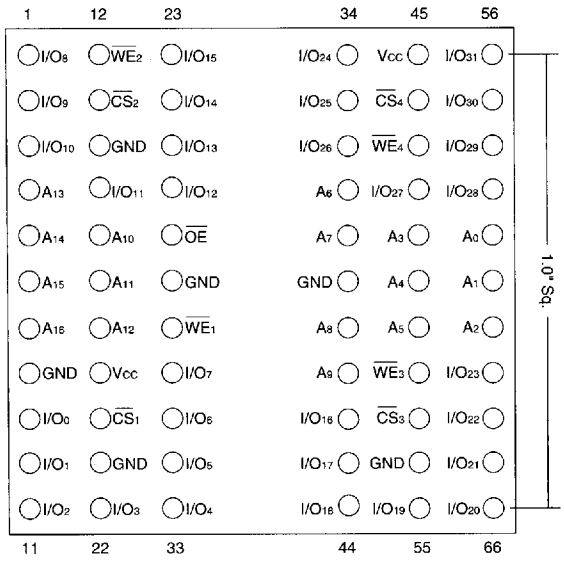

FIGURE 1 — Pin Configuration

Name	Description
I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Pin Description

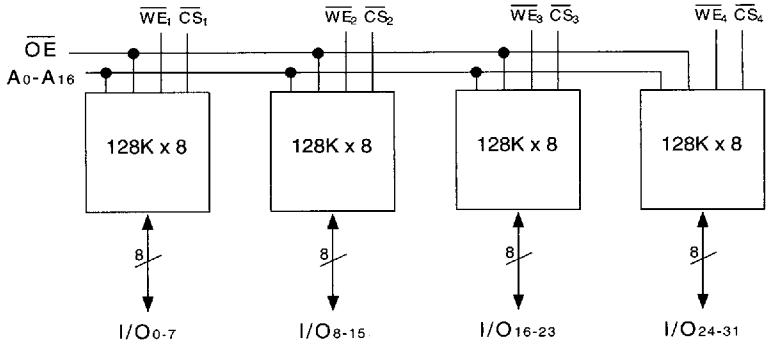

FIGURE 2 — Block Diagram

WS-128K32-XHX

PRELIMINARY
4 Megabit CMOS SRAM Module

FEATURES

- **Access Times of 25nS to 120nS**
- **66-pin, PGA Type, 1.2 inch square HIP Package**
- **Configurable as 128Kx32, 256Kx16 or 512Kx8**
- **Hermetic Ceramic Package**
- **Battery Back-Up Operation**
- **Commercial, Industrial and Military Temperature Ranges**
- **TTL Compatible Inputs and Outputs**
- **Low Power CMOS Fully Static Design**
- **5 Volt Power Supply**
- **Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation**

DESCRIPTION

The White Technology WS-128K32-XHX is a 4-megabit CMOS SRAM module organized as 128K words by 32 bits; 256K x 16 or 512K x 8. The module is constructed on a multilayer ceramic substrate, hermetically sealed, with a welded metal cover, hex-in-line package (HIP) utilizing four 128K x 8 SRAM devices.

This device is part of White Technology's "WHIP" family of memory subsystems. These modules are compatible with most 66-pin HIP packaged SRAM, EEPROM and Flash memory modules.

The WS-128K32-XHX is available with access times of 25 to 120nS over the commercial and military temperature ranges.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both low. Reading the device is accomplished by taking the chip selects low while write enable remains high. Under these conditions the contents of the memory locations specified on the address pins will appear on the data input/output pins.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Military	Unit
T_A	Operating Temperature	0 to 70	-55 to +125	°C
T_{STG}	Storage Temperature	-40 to +85	-65 to +150	°C
V_G	Signal Voltage Relative to GND	-0.5 to +7.0	-0.5 to 7.0	V

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselect)
Write	L	X	L	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

CAPACITANCE

Symbol	Parameter	Condition	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1MHz, T_A = 25°C	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1MHz, T_A = 25°C	30	pF

This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND		8	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}. V_{CC} = Max		8	µA
Operating Supply Current x 32 Mode	I_{CCx32}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		450*	mA
Operating Supply Current x 16 Mode	I_{CCx16}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		280*	mA
Operating Supply Current x 8 Mode	I_{CCx8}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		150*	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max, V_{CC} = Max		200	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA (-70 to -120 nS), I_{OL} = 8mA (-25 to -55 nS)		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA (for -70 to -125 nS)	2.4		V
		I_{OH} = -4.0mA (for -25 to -55 nS)	2.4		V

* This characteristic is frequency and configuration dependent.

AC TEST CONDITIONS

Input Pulse Levels	V_{IL} = 0V, V_{IH} = 3.0V
Input Rise and Fall Time	5 nS
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figure 3

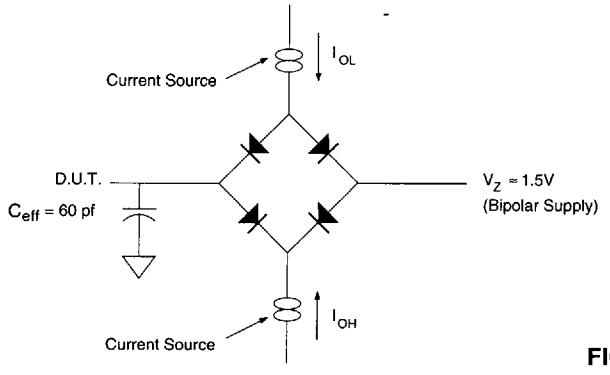

FIGURE 3

V_Z Programmable from -2V to +7V

I_{OL} & I_{OH} Programmable from 0 to 16 mA

Tester Impedance Z_O = 75 Ω

V_Z is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = ± 1.4 V)

I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

Notes: D.U.T. Device Under Test
C_{eff} Effective Capacitance
ATE Tester Includes Jig Capacitance

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C TO 125°C)

Parameter	Symbol	-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		55		nS
Address Access Time	t_{AA}		25		35		45		55	nS
Data Hold from Address Change	t_{OH}	4		4		4		4		nS
Chip Select Access	t_{ACS}		25		35		45		55	nS
Output Enable to Output Valid	t_{OE}		15		20		25		30	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		12		15		20		25	nS
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20		25	nS

1. This parameter is guaranteed by design but not tested.

Parameter	Symbol	-70		-85		-100		-120		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		nS
Address Access Time	t_{AA}		70		85		100		120	nS
Data Hold from Address Change	t_{OH}	5		5		5		5		nS
Chip Select Access	t_{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		35		40		45		50	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		30		35		40		50	nS
Output Disable to Output in High Z	t_{OHZ}[1]		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS

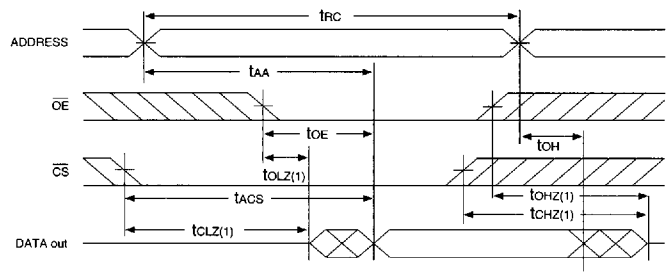

FIGURE 4 — Read Cycle Timing

1. Measured ± 200mV steady state; guaranteed by design but not tested.

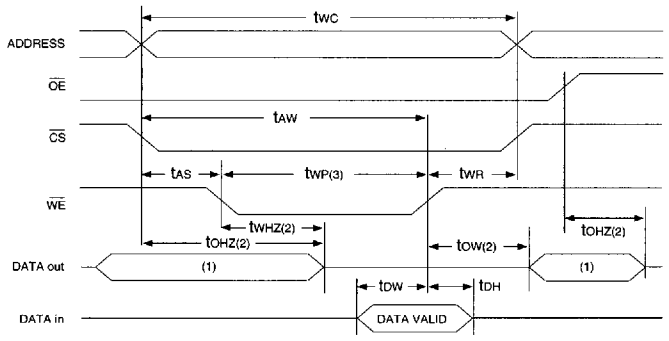

FIGURE 5 — Write Cycle Timing $\overline{WE}$ Controlled

1. I/O pins are in their output state, input signals must not be applied.
2. This parameter is guaranteed by design but not tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C TO 125°C)

Parameter Write Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		55		nS
Chip Select to End of Write	t_{CW}	20		30		40		45		nS
Address Valid to End of Write	t_{AW}	20		30		40		45		nS
Data to Write-Time Overlap	t_{DW}	15		18		20		25		nS
Data Hold from Write Time	t_{DH}	3		3		3		5		nS
Write Pulse Width	t_{WP}	20		25		35		40		nS
Address Setup Time	t_{AS}	0		0		0		0		nS
Write Recovery Time	t_{WR}	0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		10		15		15		20	nS

1. This parameter is guaranteed by design but not tested.

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		nS
Chip Select to End of Write	t_{CW}	65		80		90		110		nS
Address Valid to End of Write	t_{AW}	65		80		90		110		nS
Data to Write-Time Overlap	t_{DW}	30		35		40		55		nS
Data Hold from Write Time	t_{DH}	5		5		5		5		nS
Write Pulse Width	t_{WP}	45		50		55		65		nS
Address Setup Time	t_{AS}	5		5		5		5		nS
Write Recovery Time	t_{WR}	0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION

W S - 128K 32 - XXX H X

- **DEVICE GRADE:**
  - M = Mil, -55°C to +125°C
  - I = Industrial, -40°C to 85°C
  - C = Commercial, 0 to 70°C
- **PACKAGE TYPE:**
  - H = Hex in line package
- **ACCESS TIME IN nS**
- **BITS PER WORD:**
  - x8, x16, x32
- **NUMBER OF WORDS:**
  - 512K, 256K, 128K
- **SRAM**
- **WHITE TECHNOLOGY**

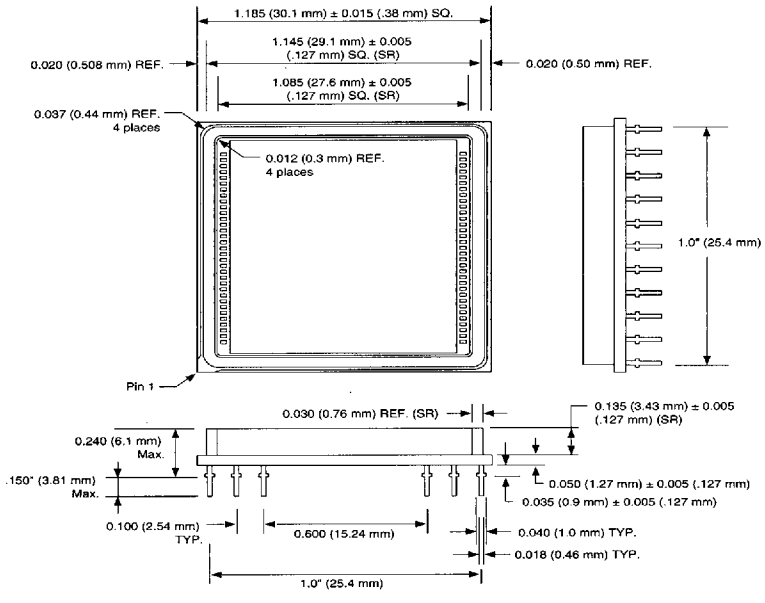

FIGURE 6 — Package Dimensions

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