4K x 8 CMOS Dual Port SRAM

FEATURES

- High-speed–35/45/55ns
- MS6134 - Standalone device
- True Dual Port Memory array
- Low Power dissipation
  - 325mW (Typ.) Operating
  - 5 mW (Typ.) Standby
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0-5.5V
- Fully asynchronous operation from either port

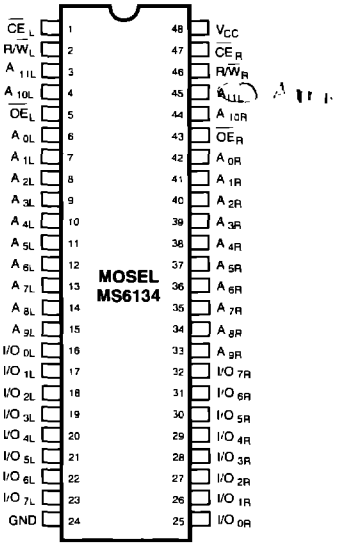
DESCRIPTION

The MOSEL MS6134 is a 32,768 bit dual port static random access memory organized as 4,096 words by 8 bits allowing each port to independently access any location in memory. The MS6134 is ideal for systems that require no on-chip arbitration.

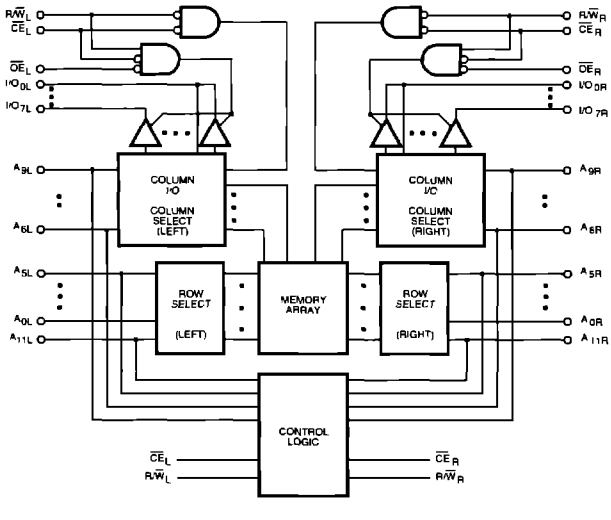
Systems using the MS6134 must be capable of supplying their own arbitration to prevent contention. Power reduction circuitry offers a battery backup data retention capability. The circuit typically consumes only 200 µW power from a 2V battery. The MS6134 is packaged in a 48-pin 600 mil-DIP.

5

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
A_{0L}-A_{11L}	A_{0R}-A_{11R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

FUNCTIONAL DESCRIPTION

The MS6134 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The MS6134 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, $\overline{OE}$ enables the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in truth table

TRUTH TABLE

LEFT PORT INPUTS			RIGHT PORT INPUT			
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	FUNCTION
X	H	X	X	X	X	Left Port in Power Down Mode
X	X	X	X	H	X	Right Port in Power Down Mode
L	L	X	X	X	X	Data on Left Port Written Into Memory
H	L	L	X	X	X	Data in Memory Output on Left Port
X	X	X	L	L	X	Data on Right Port Written Into Memory
X	X	X	H	L	L	Data in Memory Output on Right Port

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	CONDITION	UNIT
V_{TERM}	Terminal Voltage with Repect to GND	–0 5 to +7 0	V
T_{BIAS}	Temperature Under Bias	–10 to +125	°C
T_{STG}	Storage Temperature	–40 to +150	°C
P_T	Power Dissipation	1 0	W
I_{OUT}	DC Output Current	20	mA

1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to + 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MS6134 MIN.	MS6134 TYP. (1)	MS6134 MAX.	UNITS
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5 5V, V_{IN} = 0V to V_{CC}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	2	µA
V_{IH}	Input High Voltage		2 2	—	6 0	V
V_{IL}	Input Low Voltage		–0 5	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open t_{RC} = 35ns	—	—	195	mA
		t_{RC} = 45 ns	—	—	190	
		t_{RC} = 55 ns	—	—	180	
I_{SB1}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	—	25	40	mA
I_{SB2}	Standby Current (One Port Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	—	40	120	mA
I_{SB3}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0 2V $V_{IN} \geq V_{CC}$ – 0 2V or $V_{IN} \leq$ 0 2V	—	1	5	mA
I_{SB4}	Full Standby Current (One Port Full Standby)	One Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0 2V or $V_{IN} \leq$ 0 2V Active Port Outputs Open	—	—	105	mA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 8mA	—	—	0 4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2 4	—	—	V

NOTE
1. V_{CC} = 5 0V, T_A = +25°C

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	15	pF
C_{OUT}	Input Capacitance	V_{OUT} = 0V	15	pF

1 This parameter is guaranteed and not 100% tested

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to + 70°C)

SYMBOL	PARAMETER	MS6134-35 MIN.	MS6134-35 MAX.	MS6134-45 MIN.	MS6134-45 MAX.	MS6134-55 MIN.	MS6134-55 MAX.	UNITS
READ CYCLE								
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	ns
t_{ACE}	Chip Enable Access Time	—	35	—	45	—	55	ns
t_{AOE}	Output Enable Access Time	—	15	—	20	—	30	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	5	—	ns
t_{LZ}	Output Low Z Time[1,2]	3	—	3	—	5	—	ns
t_{HZ}	Output High Z Time[1,2]	—	15	—	20	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	40	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{EW}	Chip Enable to End of Write	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	40	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DS}	Input Data Setup Time	15	—	25	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z[1,2]	0	15	0	20	0	25	ns
t_{OW}	Output Active From End of Write[1,2]	3	—	3	—	3	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 & 3)
2. This parameter guaranteed but not tested

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

*Including scope and jig.

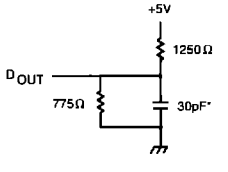


Figure 1
Output Load

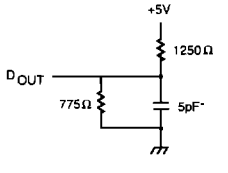
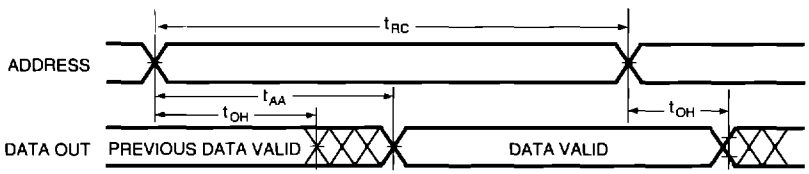


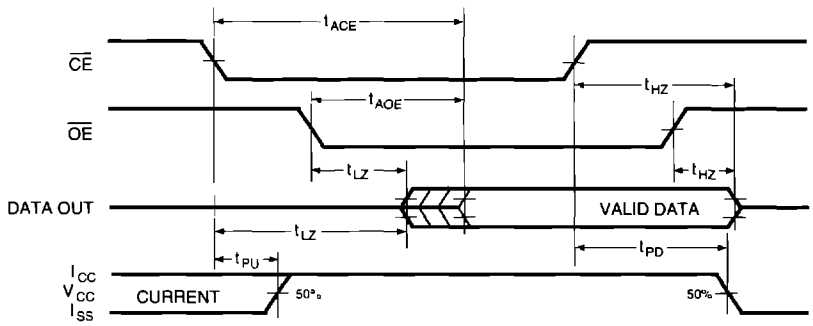
Figure 2
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

TIMING WAVEFORMS

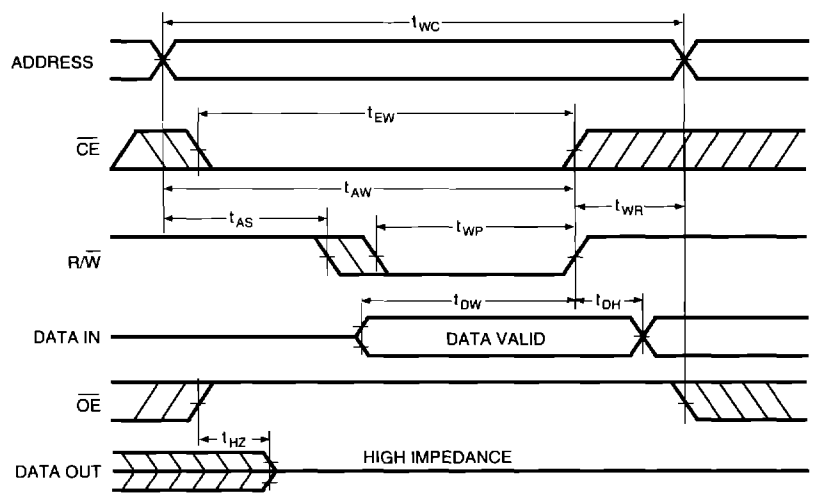
READ CYCLE NO. 1 EITHER SIDE [1,2,6]



READ CYCLE NO. 2 EITHER SIDE [1,3]

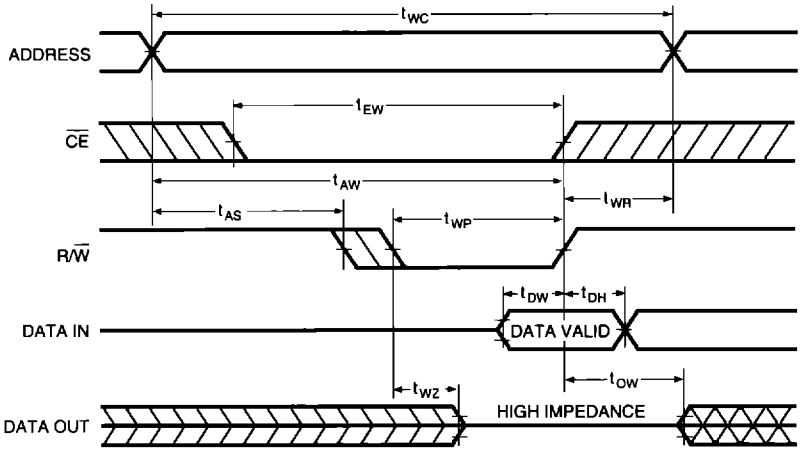


WRITE CYCLE NO. 1 EITHER SIDE [4,7]



TIMING WAVEFORMS

WRITE CYCLE NO. 2 EITHER SIDE [4,7]

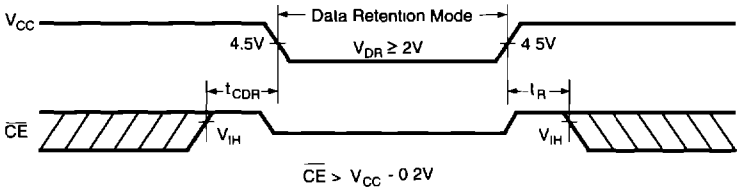


NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
6. $\overline{OE} = V_{IL}$
7. R/$\overline{W} = V_{IH}$ during address transition

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V	—	—	500	µA
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{CC} - 0.2V$	0	—	—	ns
t_R	Operation Recovery Time	$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	t_{RC}(2)	—	—	ns

NOTES:
1. T_A = 25°C
2. t_{RC} = Read Cycle Time



5

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
35	MS6134-35PC	P48-2	0°C to +70°C
45	MS6134-45PC	P48-2	0°C to +70°C
55	MS6134-55PC	P48-2	0°C to +70°C