M5M44100J, L-8, -10

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

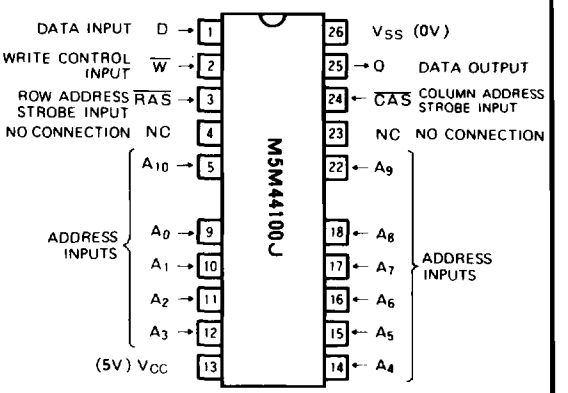
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44100$^{J}_{L}$-8	80	20	40	160	415
M5M44100$^{J}_{L}$-10	100	25	50	190	350

- Standard 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M44100J, L-8 . . . . . 522.5mW (Max)
  M5M44100J, L-10 . . . . . 467.5mW (Max)
- Fast-page mode (2048 bits random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write operation gives common I/O capability
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 512K word x 8 bit test mode capability

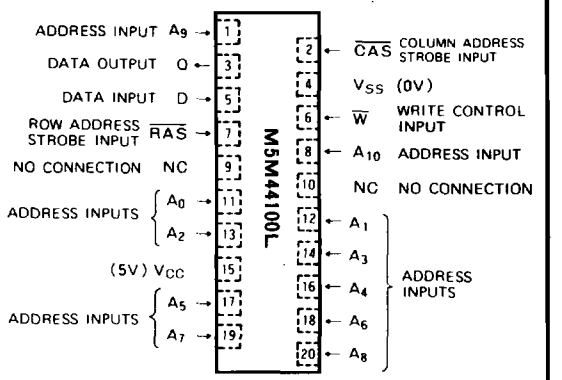
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0Z (SOJ)



Outline 20P5L-B (ZIP)

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

FUNCTION

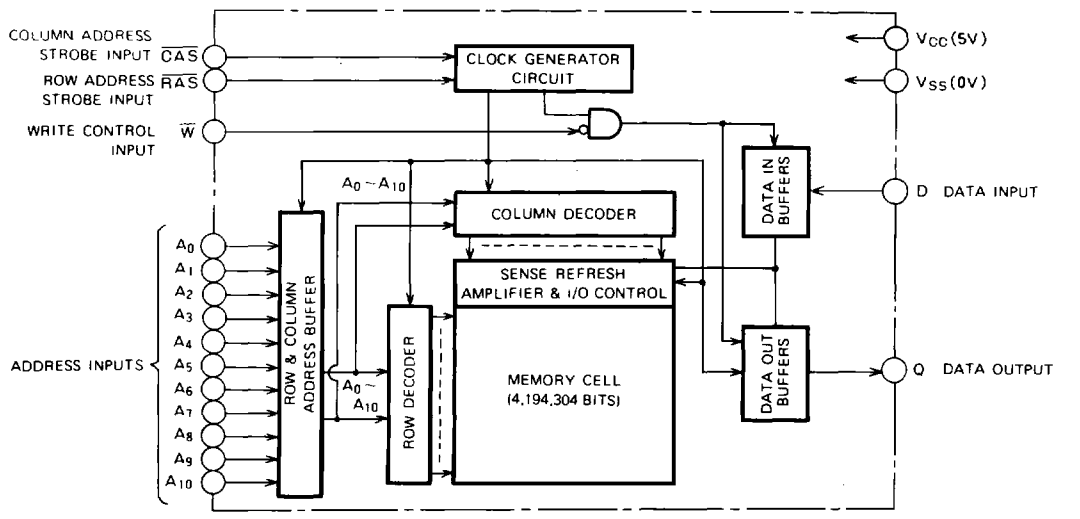
The M5M44100J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast-page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	VLD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, IVD invalid, APD: applied, OPN open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M44100-8	$\overline{RAS}$, $\overline{CAS}$ cycling			95	mA
		M5M44100-10	t_{RC}＝t_{WC}＝min, output open			85	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$＝$\overline{CAS}$＝V_{IH}, output open			2	mA
			$\overline{RAS}$＝$\overline{CAS}$＝$\overline{W}$≧V_{CC}−0.5, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M44100-8	$\overline{RAS}$ cycling, $\overline{CAS}$＝V_{IH}			95	mA
		M5M44100-10	t_{RC}＝min, output open			85	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast page mode (Note 3, 4)	M5M44100-8	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$＝cycling			95	mA
		M5M44100-10	t_{PC}＝min, output open			85	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44100-8	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling			80	mA
		M5M44100-10	t_{RC}＝min, output open			70	

Note 2 Current flowing into an IC is positive, out is negative.
3 $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4 $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open

CAPACITANCE (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M44100J	V_I＝V_{SS} f＝1MHz V_I＝25mVrms			6	pF
		M5M44100L				7	pF
$C_{I(D)}$	Input capacitance, data input					6	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
C_O	Output capacitance		V_O＝V_{SS}, f＝1MHz, V_I＝25mVrms			7	pF

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted see notes 5, 13, 14)

Symbol	Parameter		Limits (Note 6)				Unit
			M5M44100-8		M5M44100-10		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20 (25)		25 (30)	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		80 (85)		100 (105)	ns
t_{AA}	Column address access time	(Note 7, 10)		40 (45)		50 (55)	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		45 (50)		55 (60)	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	0	25	ns

Note 5 An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: The value in parentheses is specified in test mode cycle.

7: Measure with a load circuit equivalent to 2TTL loads and 100pF.

8. Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9. Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.

10 Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11 Assumes that $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \leqq t_{CP(max)}$, or $t_{ASC} \leqq t_{ASC(max)}$ and $t_{CP} - t_{ASC} \leqq 5ns$.
If $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$, access time (t_{CPA}) is controlled exclusively by t_{CAC}.
If $t_{ASC} \leqq t_{ASC(max)}$, $t_{CP} \leqq t_{CP(max)}$ and $t_{CP} - t_{ASC} \geqq 5ns$, or $t_{ASC} \leqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$, access time (t_{CPA}) is controlled exclusively by t_{AA}.

12. $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and is not reference to $V_{OH(max)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, see notes 13, 14)

Symbol	Parameter		Limits				Unit
			M5M44100-8		M5M44100-10		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			16.4		16.4	ms
t_{RP}	$\overline{RAS}$ high pulse width		70		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	22	60	25	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	17	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	15	0	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		12		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		20		ns
t_T	Transition time	(Note 18)	1	50	1	50	ns

Note 13 The timing requirements are assumed $t_T = 5ns$.

14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals

15: Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greather than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

16 Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

17 $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, column address access time(t_{AA}) is controlled exclusively by t_{CAC}.

18 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits (Note 6)				Unit
			M5M44100-8		M5M44100-10		
			Min	Max	Min	Max	
t_{RC}	Read cycle time		160 (165)		190 (195)		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80 (85)	10000	100 (105)	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20 (25)	10000	25 (30)	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		80 (85)		100 (105)		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20 (25)		25 (30)		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 19)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 19)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		40 (45)		50 (55)		ns

Note 19: Either t_{RCH} or t_{RRH} must be satisfied.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M44100-8		M5M44100-10		
			Min	Max	Min	Max	
t_{WC}	Write cycle time		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		15		20		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		20		25		ns
t_{WP}	Write pulse width		15		20		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits (Note 6)				Unit
			M5M44100-8		M5M44100-10		
			Min	Max	Min	Max	
t_{RWC}	Read write cycle time	(Note 20)	185 (190)		220 (225)		ns
t_{RMWC}	Read modify write cycle time	(Note 21)	185 (190)		220 (225)		ns
t_{RAS}	$\overline{RAS}$ low pulse width		105 (110)	10000	130 (135)	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		45 (50)	10000	55 (60)	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105 (110)		130 (135)		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		45 (50)		55 (60)		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	20 (25)		25 (30)		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	80 (85)		100 (105)		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 22)	40 (45)		50 (55)		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		20		25		ns
t_{WP}	Write pulse width		15		20		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		15		20		ns

Note 20: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
21: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
22: t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} do not define the limits of operation, but are included as electrical characteristics only.
When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geqq t_{RwD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition (delayed write) is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read-Write Read-Modify-Write Cycles) (Note 23)

Symbol	Parameter		Limits (Note 6)				Unit
			M5M44100-8		M5M44100-10		
			Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		50 (55)		60 (65)		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		75 (80)		90 (95)		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 24)	130 (135)	200000	160 (165)	200000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 25)	10	20	10	25	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		45 (50)		55 (60)		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 22)	45 (50)		55 (60)		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
25: Operation within the $t_{CP(max)}$ limit insures that $t_{CPA(max)}$ can be met. $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M44100-8		M5M44100-10		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		20		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	15		20		ns

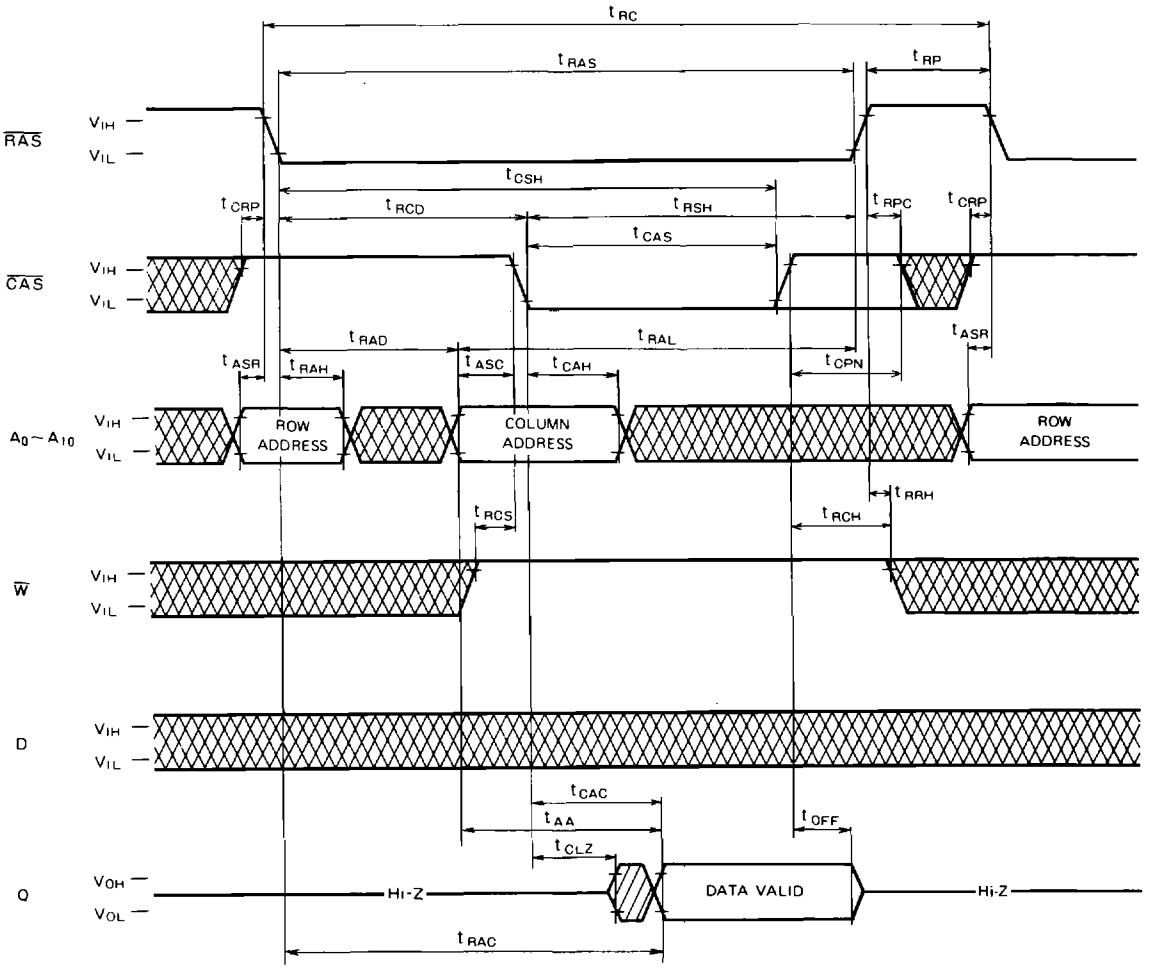
Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Tes Mode Set Cycle

Symbol	Parameter	Limits				Unit
		M5M44100-8		M5M44100-10		
		Min	Max	Min	Max	
t_{WSR}	Write setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	Write hold time after $\overline{RAS}$ low	15		20		ns

Timing Diagrams (Note 27)

Read Cycle

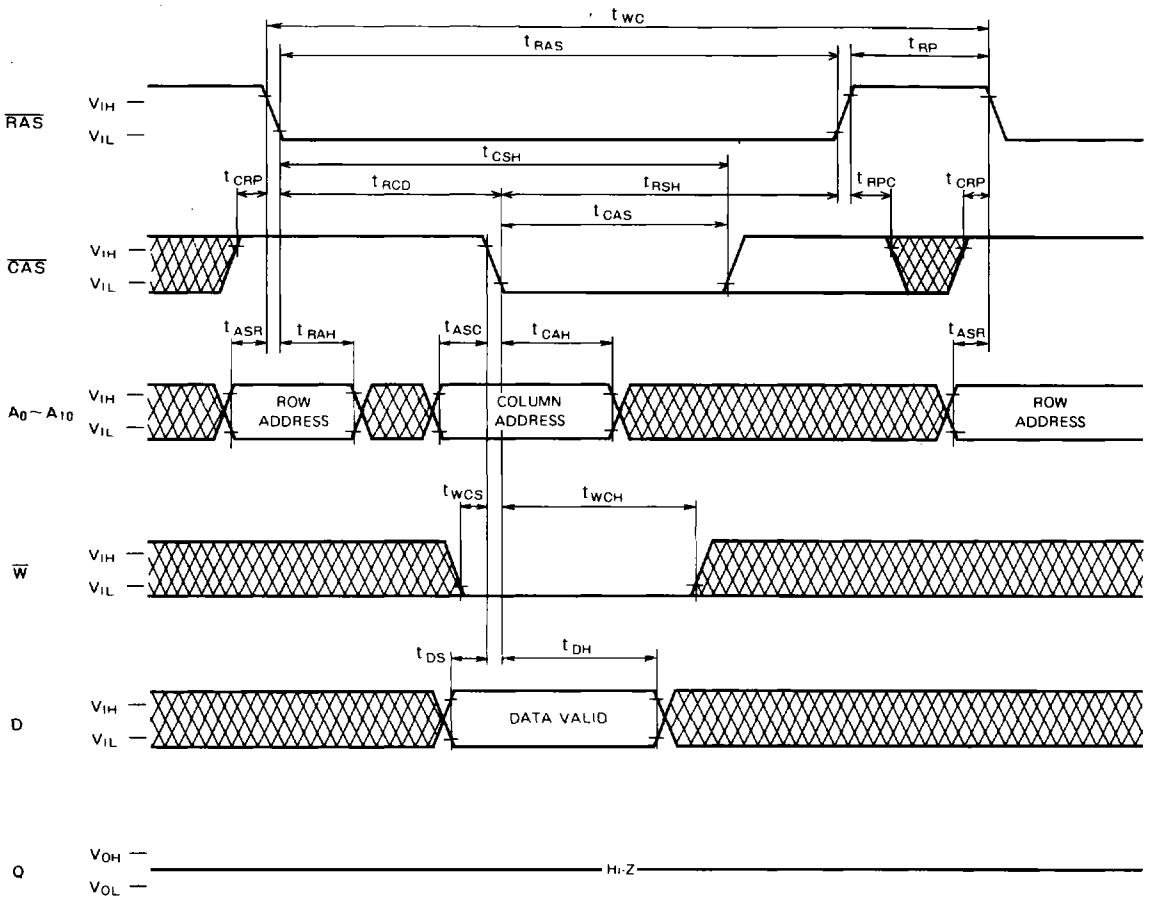


Note 27

Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

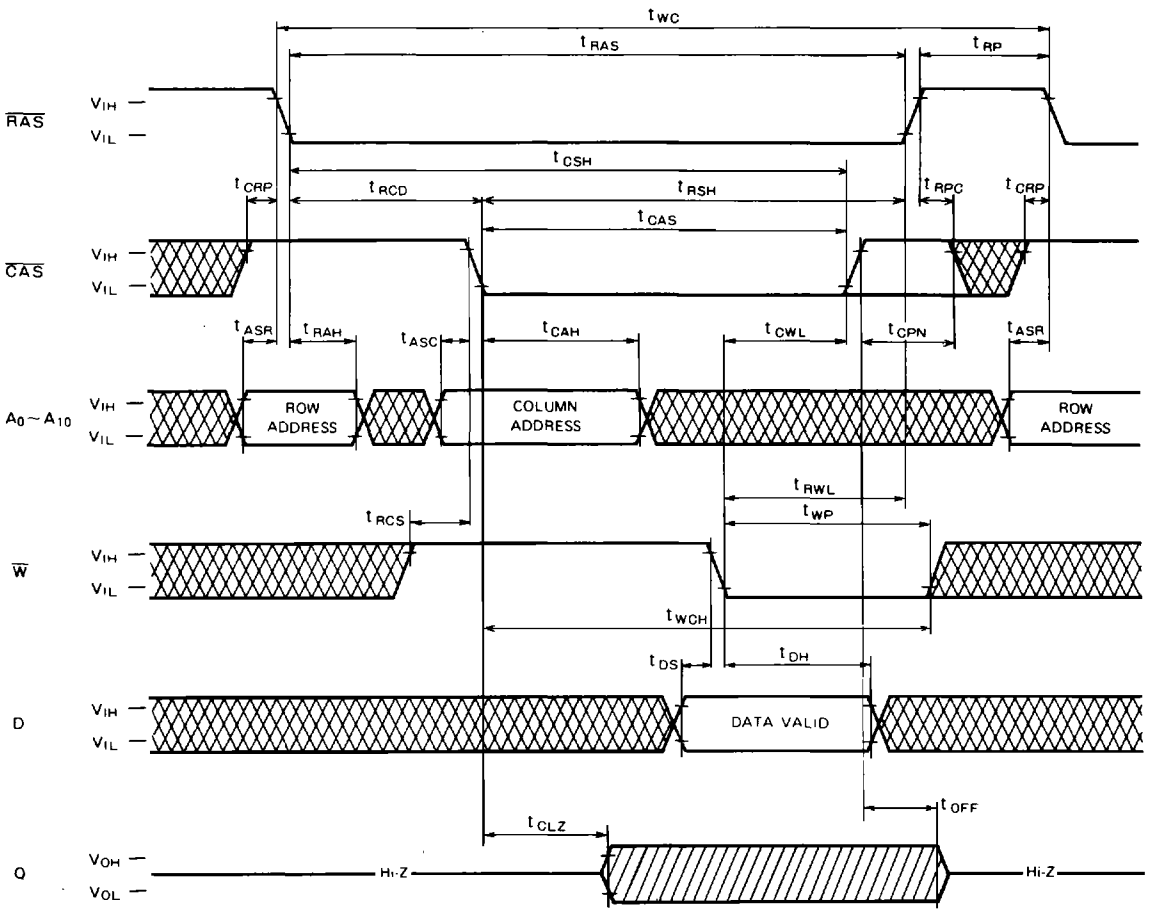
Indicates the invalid output.

Write Cycle (Early Write)

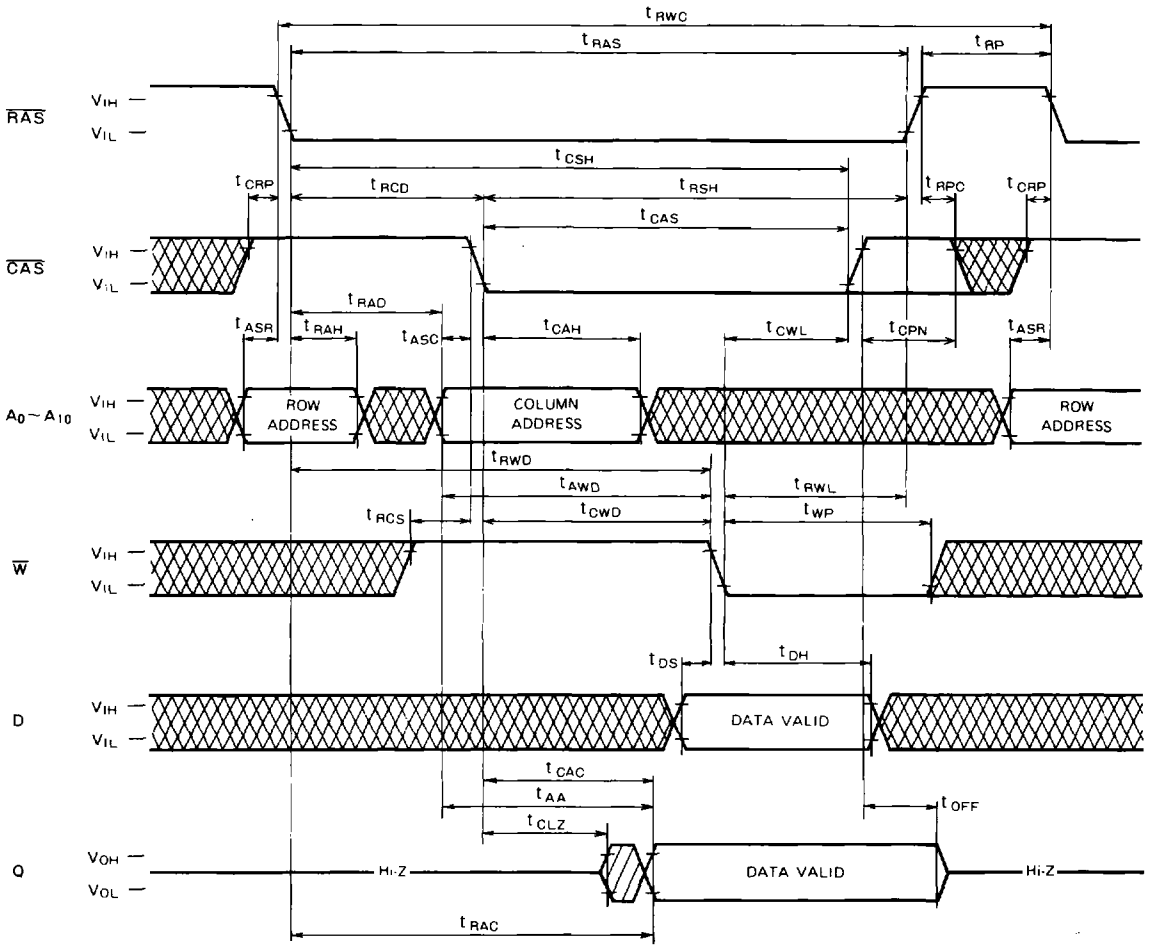


MITSUBISHI ELECTRIC

Write Cycle (Delayed Write)



Read-Write, Read-Modify-Write Cycle



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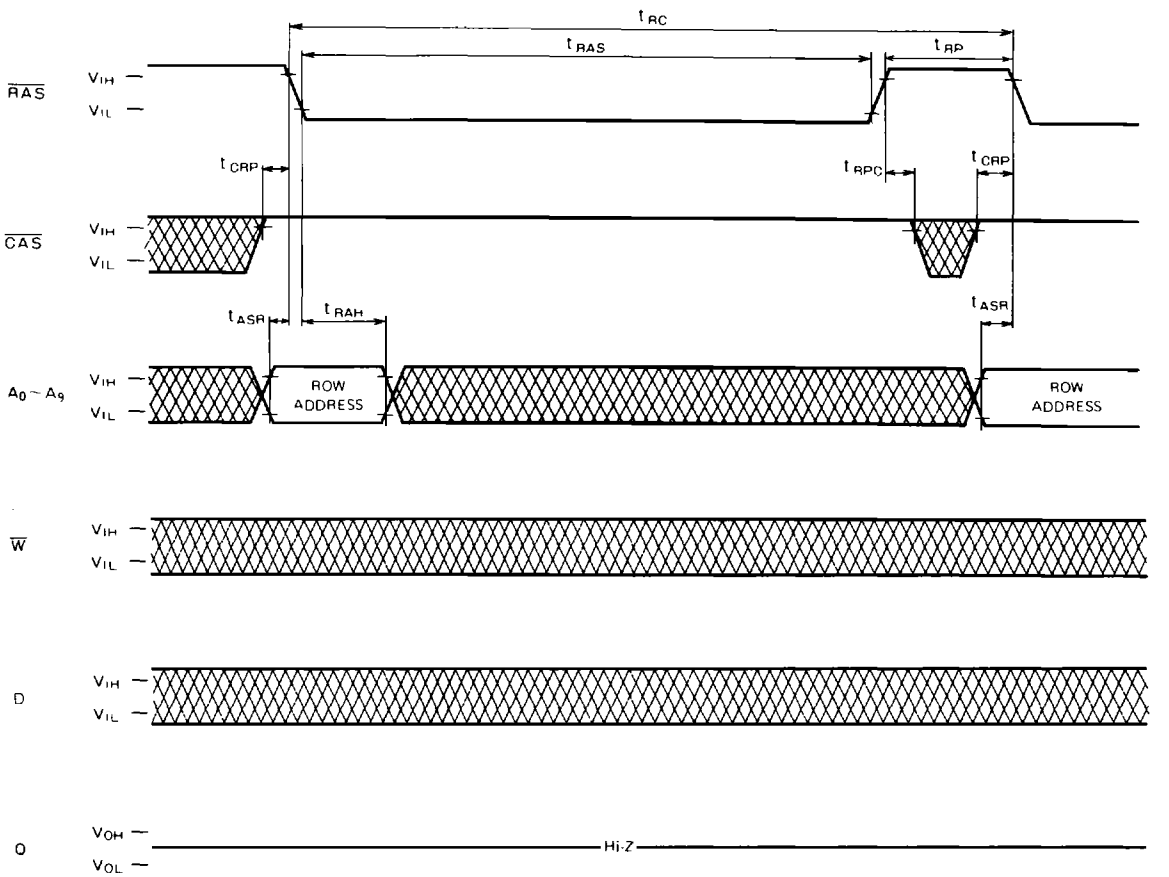
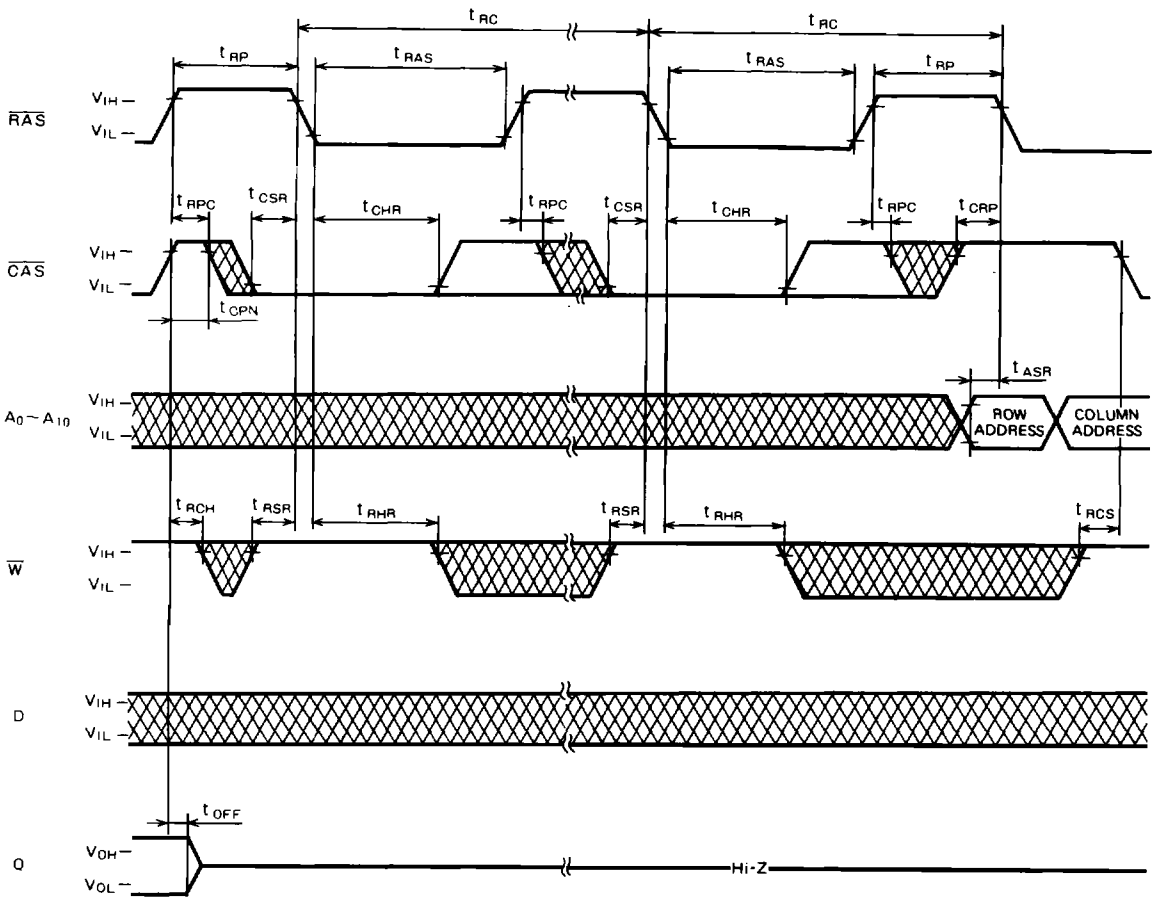
$\overline{RAS}$-only-Refresh Cycle (Note 28)

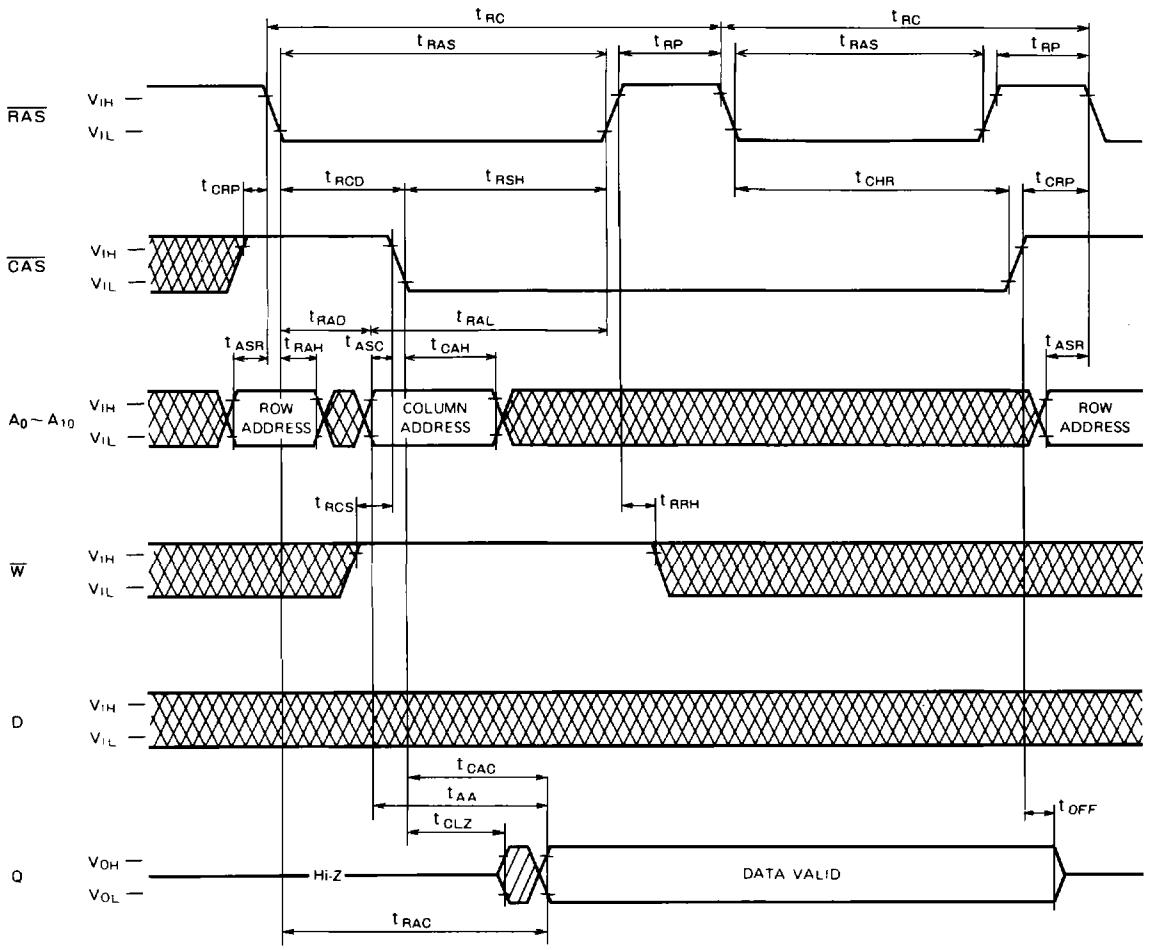


Note 28 A_{10} may be V_{IH} or V_{IL}. Refresh address: A_0 (ROW) ~ A_9 (ROW).

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

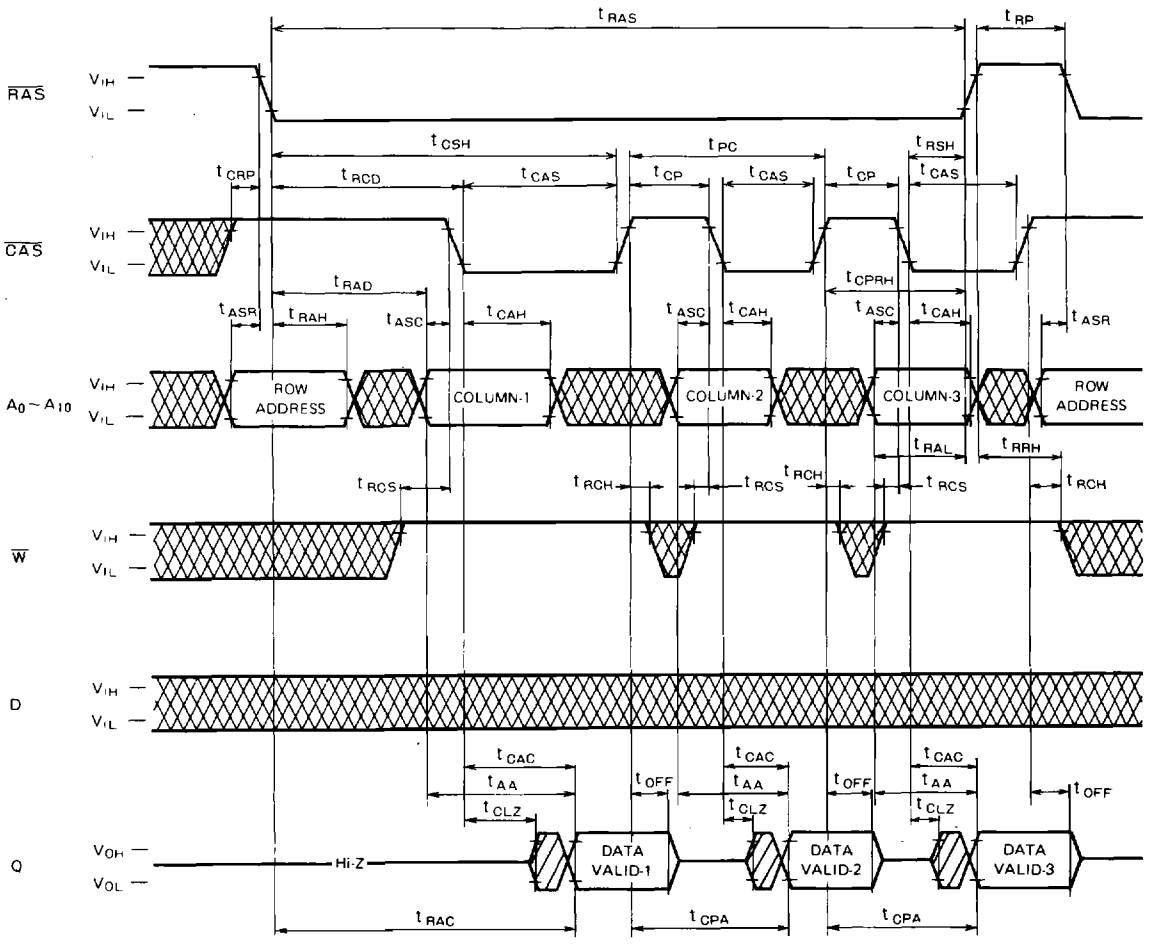


Hidden Refresh Cycle (Read) (Note 29)



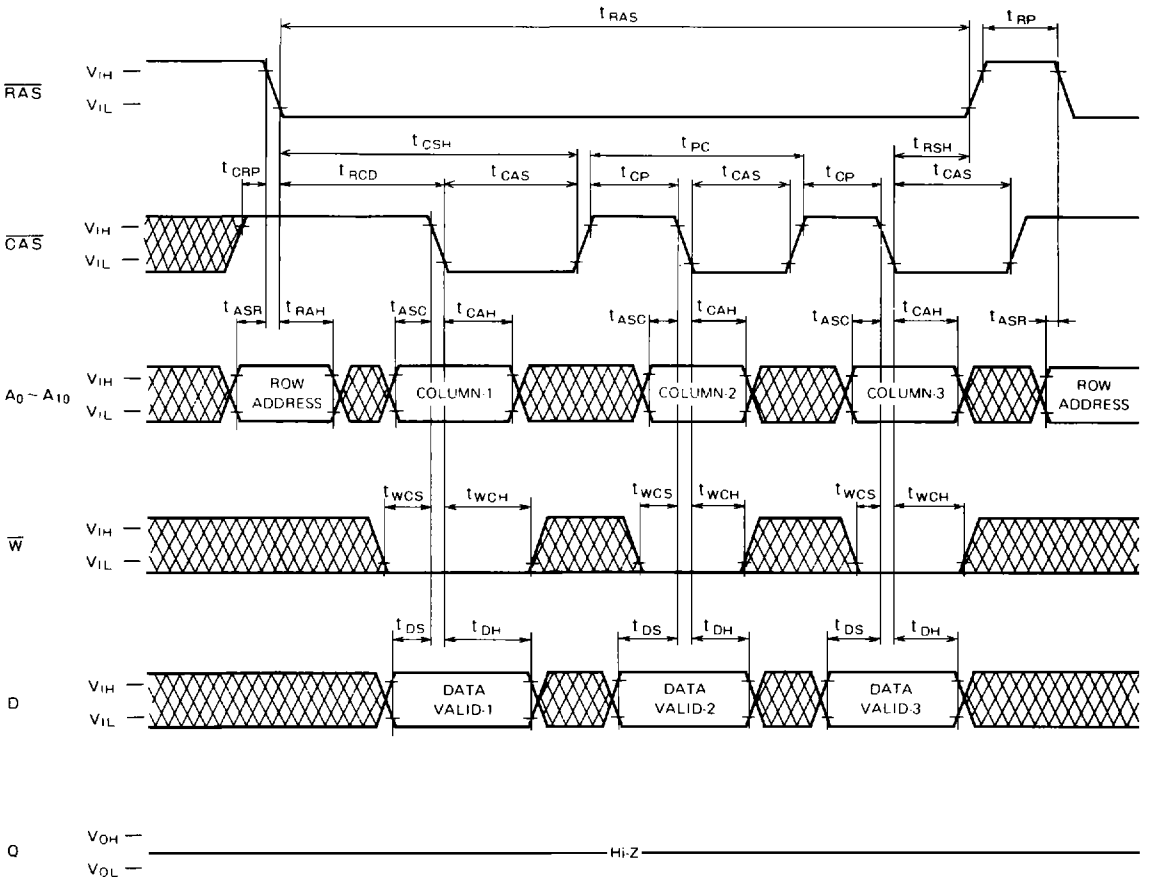
Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Fast-Page-Mode Read Cycle

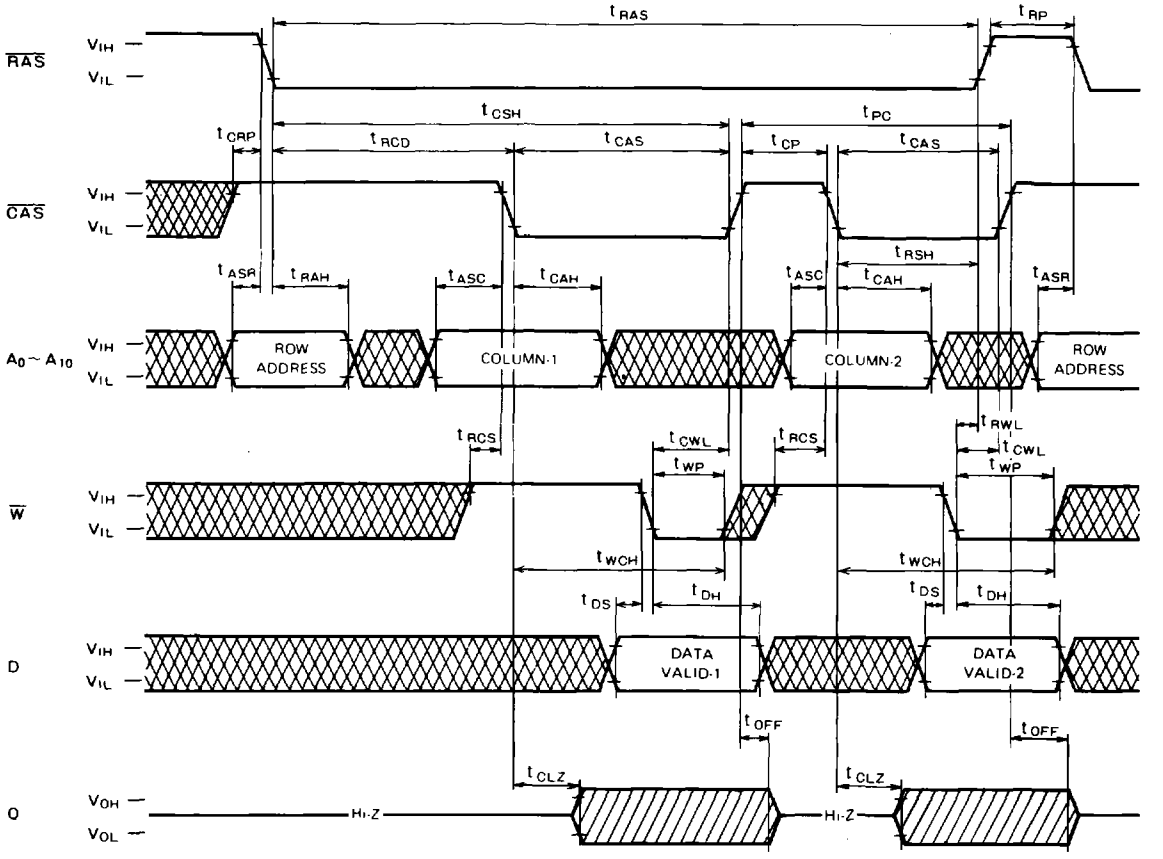


MITSUBISHI ELECTRIC

Fast-Page-Mode Write Cycle (Early Write)

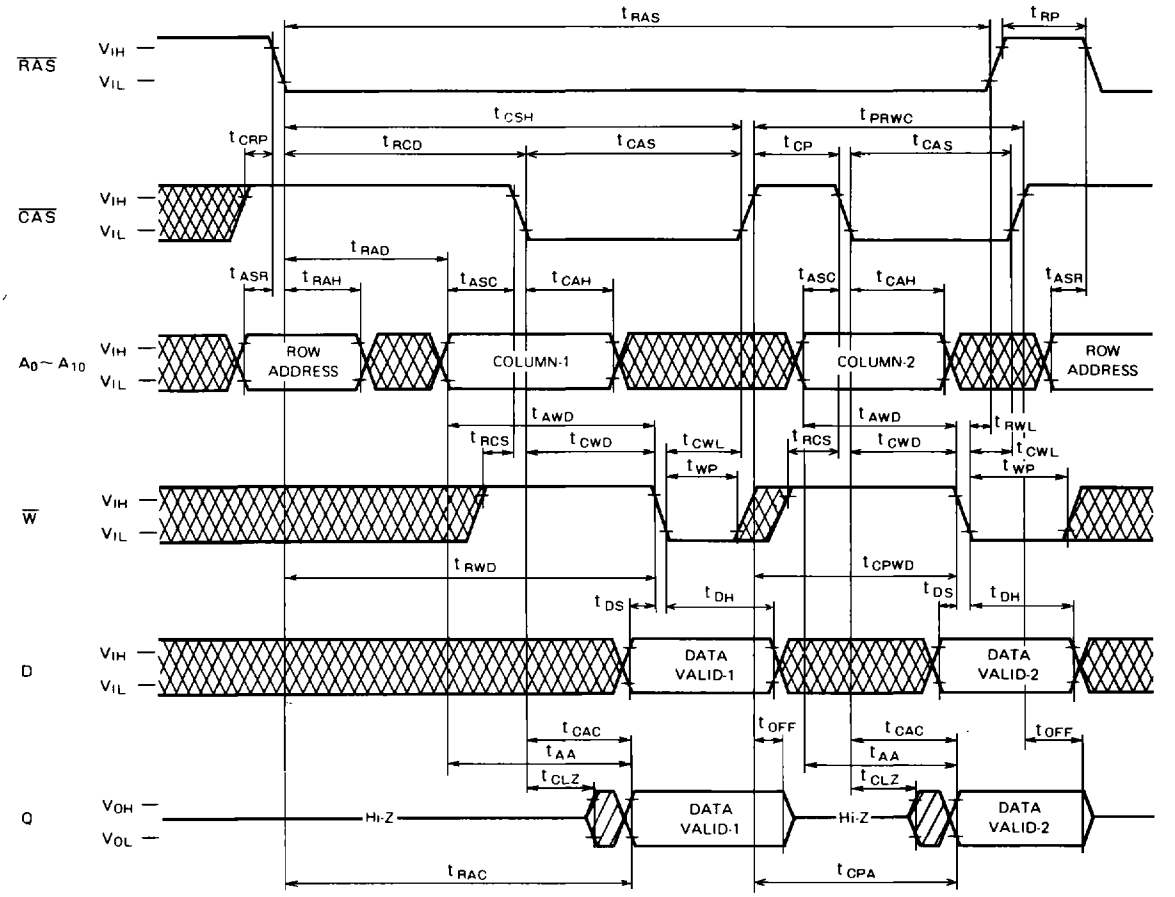


Fast-Page-Mode Write Cycle (Delayed Write)

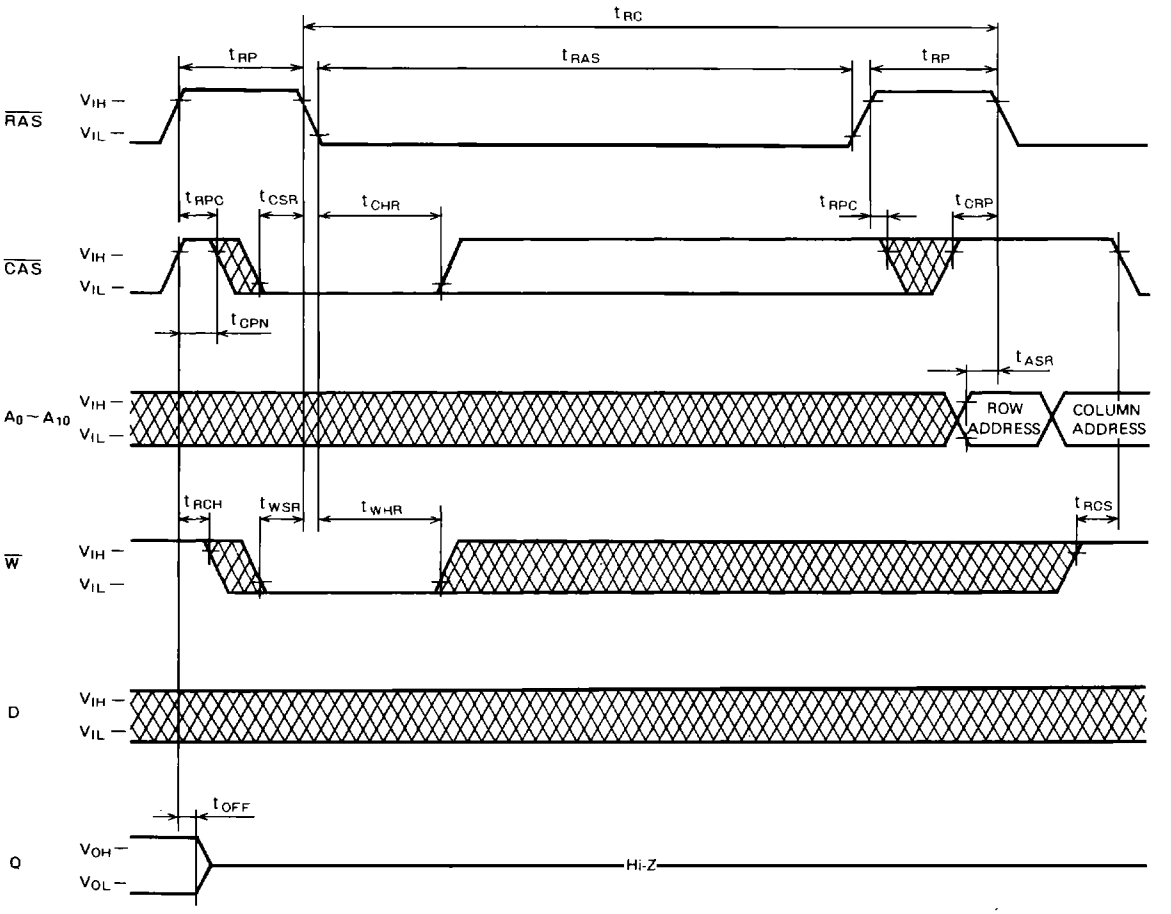


MITSUBISHI ELECTRIC

Fast-Page-Mode Read-Write, Read-Modify-Write Cycle



Test Mode Set Cycle (Note 30)



Note 30: This cycle is also available for the initialization cycle, but in this case device enters test mode. Test mode is reset by $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.