

DDR2 Unbuffered SODIMM

**200pin Unbuffered SODIMM based on 1Gb R-die
64-bit Non-ECC**

**60FBGA with Lead-Free and Halogen-Free
(RoHS compliant)**

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Revision History

Revision	Month	Year	History
1.0	March	2008	- Initial Release
1.1	April	2008	- Added new product
1.2	July	2008	- Applied JEDEC update(JESD79-2E) on AC timing table

1.0 DDR2 Unbuffered SODIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
M470T5663RZ3-CF7/E6	2GB	256Mx64	128Mx8(K4T1G084QR-HCF7/E6)*16	2	30mm
M470T2863RZ3-CF7/E6	1GB	128Mx64	128Mx8(K4T1G084QR-HCF7/E6)*8	1	30mm

Note :

1. "Z" of Part number(12th digit) stand for Lead-free products.
2. "H" of Part number(12th digit) stand for Lead-free, Halogen-free and RoHS compliant products.
3. "3" of Part number(13th digit) stand for Dummy Pad PCB products.

2.0 Features

- Performance range

	F7 (DDR2-800)	E6 (DDR2-667)	Unit
Speed@CL3	-	400	Mbps
Speed@CL4	533	533	Mbps
Speed@CL5	667	667	Mbps
Speed@CL6	800	-	Mbps
CL-tRCD-tRP	6-6-6	5-5-5	CK

- JEDEC standard 1.8V $\pm$ 0.1V Power Supply
- $V_{DDQ} = 1.8V \pm 0.1V$
- 333MHz f_{CK} for 667Mb/sec/pin, 400MHz f_{CK} for 800Mb/sec/pin
- 8 Banks
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- PASR(Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq 95^\circ C$
- support High Temperature Self-Refresh rate enable feature
- Package: 60ball FBGA - 128Mx8
- All of base components are Lead-free, Halogen-free and RoHS compliant

Note : For detailed DDR2 SDRAM operation, please refer to Samsung's Device operation & Timing diagram.

3.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx8(1Gb) based Module	A0-A13	A0-A9	BA0-BA2	A10

4.0 Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REF}	2	V _{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V _{SS}	4	DQ4	53	V _{SS}	54	V _{SS}	103	V _{DD}	104	V _{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V _{SS}	156	V _{SS}
7	DQ1	8	V _{SS}	57	DQ19	58	DQ23	107	BA0	108	RAS	157	DQ48	158	DQ52
9	V _{SS}	10	DM0	59	V _{SS}	60	V _{SS}	109	WE	110	$\overline{S}0$	159	DQ49	160	DQ53
11	$\overline{DQS}0$	12	V _{SS}	61	DQ24	62	DQ28	111	V _{DD}	112	V _{DD}	161	V _{SS}	162	V _{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	CAS	114	ODT0	163	NC, TEST	164	CK1
15	V _{SS}	16	DQ7	65	V _{SS}	66	V _{SS}	115	NC/ $\overline{S}1$	116	A13	165	V _{SS}	166	$\overline{CK}1$
17	DQ2	18	V _{SS}	67	DM3	68	$\overline{DQS}3$	117	VDD	118	V _{DD}	167	$\overline{DQS}6$	168	V _{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	NC/ODT1	120	NC	169	DQS6	170	DM6
21	V _{SS}	22	DQ13	71	V _{SS}	72	V _{SS}	121	V _{SS}	122	V _{SS}	171	V _{SS}	172	V _{SS}
23	DQ8	24	V _{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V _{SS}	28	V _{SS}	77	V _{SS}	78	V _{SS}	127	V _{SS}	128	V _{SS}	177	V _{SS}	178	V _{SS}
29	$\overline{DQS}1$	30	CK0	79	CKE0	80	NC/CKE1	129	$\overline{DQS}4$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK}0$	81	V _{DD}	82	V _{DD}	131	DQS4	132	V _{SS}	181	DQ57	182	DQ61
33	V _{SS}	34	V _{SS}	83	NC	84	NC	133	V _{SS}	134	DQ38	183	V _{SS}	184	V _{SS}
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS}7$
37	DQ11	38	DQ15	87	V _{DD}	88	V _{DD}	137	DQ35	138	V _{SS}	187	V _{SS}	188	DQS7
39	V _{SS}	40	V _{SS}	89	A12	90	A11	139	V _{SS}	140	DQ44	189	DQ58	190	V _{SS}
41	V _{SS}	42	V _{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V _{SS}	193	V _{SS}	194	DQ63
45	DQ17	46	DQ21	95	V _{DD}	96	V _{DD}	145	V _{SS}	146	$\overline{DQS}5$	195	SDA	196	V _{SS}
47	V _{SS}	48	V _{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS}2$	50	NC	99	A3	100	A2	149	V _{SS}	150	V _{SS}	199	V _{DD} SPD	200	SA1

Note : NC = No Connect; NC, TEST(pin 163)is for bus analysis tool and is not connected on normal memory modules.

5.0 Pin Description

Pin Name	Description	Pin Name	Description
CK0,CK1	Clock Inputs, positive line	SDA	SPD Data Input/Output
$\overline{CK}0,\overline{CK}1$	Clock Inputs, negative line	SA1,SA0	SPD address
CKE0,CKE1	Clock Enables	DQ0~DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe	DM0~DM7	Data Masks
$\overline{CAS}$	Column Address Strobe	DQS0~DQS7	Data strobes
$\overline{WE}$	Write Enable	$\overline{DQS}0\sim\overline{DQS}7$	Data strobes complement
$\overline{S}0,\overline{S}1$	Chip Selects	TEST	Logic Analyzer specific test pin (No connect on So-DIMM)
A0~A9, A11~A13	Address Inputs	V _{DD}	Core and I/O Power
A10/AP	Address Input/Autoprecharge	V _{SS}	Ground
BA0~BA2	SDRAM Bank Address	V _{REF}	Input/Output Reference
ODT0,ODT1	On-die termination control	V _{DD} SPD	SPD Power
SCL	Serial Presence Detect (SPD) Clock Input	NC	Spare pins, No connect
CK0,CK1	Clock Inputs, positive line	SDA	SPD Data Input/Output

*The VDD and VDDQ pins are tied to the single power-plane on PCB.

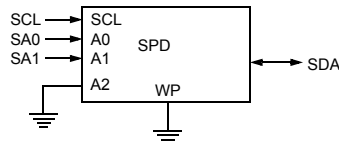
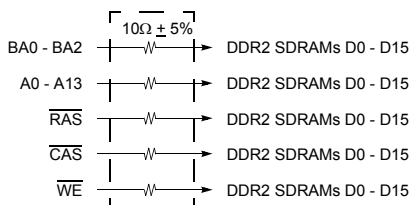
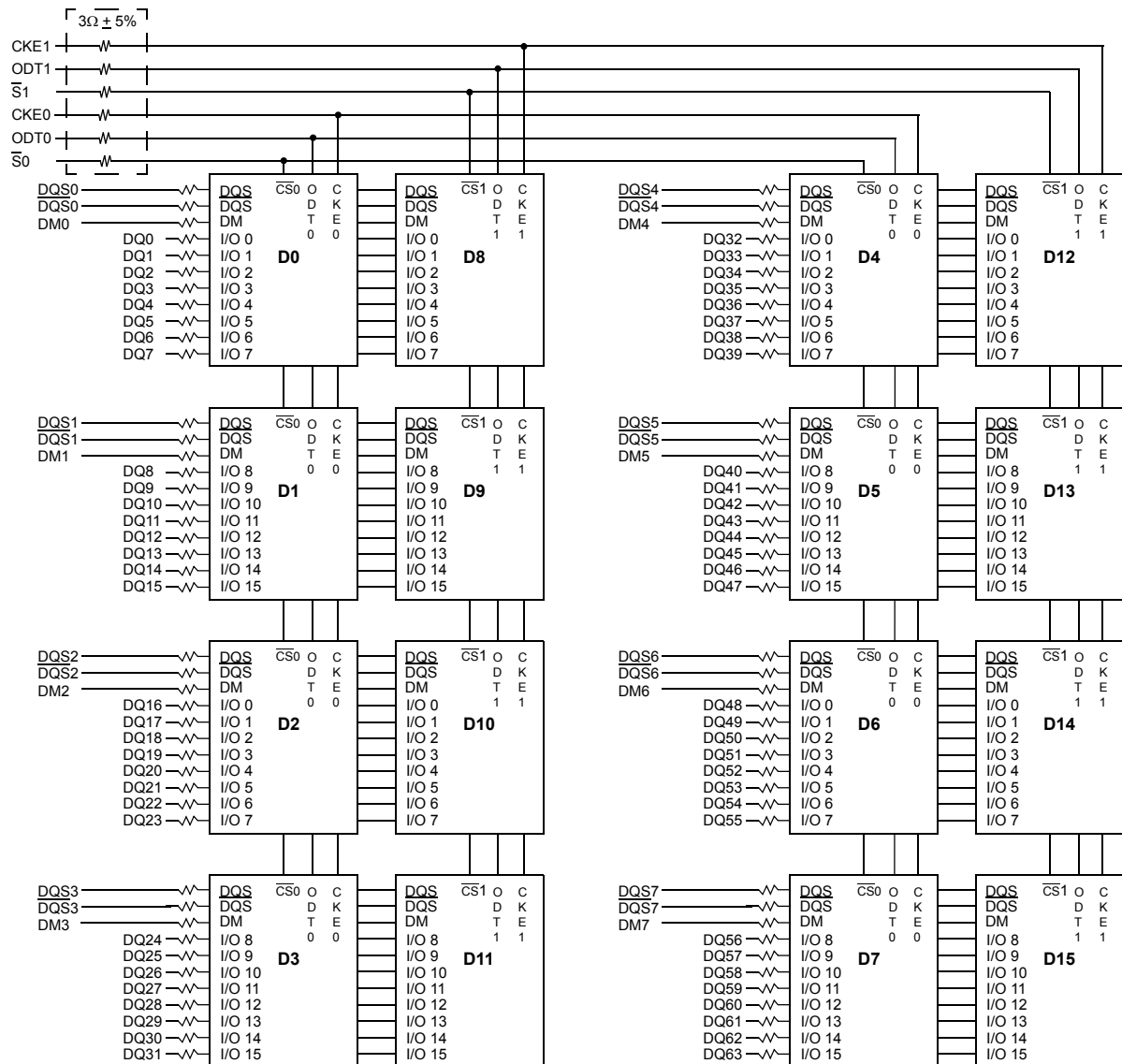
6.0 Input/Output Function Description

Symbol	Type	Description
$\overline{CK0-CK1}$ $\overline{CK0-CK1}$	Input	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock input and output timing for read operations is synchronized to the input clock.
CKE0-CKE1	Input	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0-S1}$	Input	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$, Rank 1 is selected by $\overline{S1}$. Ranks are also called "Physical banks".
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0~BA2	Input	Selects which DDR2 SDRAM internal bank is activated.
ODT0~ODT1	Input	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM Extended Mode Register Set (EMRS).
A0~A9, A10/AP, A11~A13	Input	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autprecharge operation at the end of the burst read or write cycle. If AP is high, autprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0~DQ63	In/Out	Data Input/Output pins.
DM0~DM7	Input	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
$\overline{DQS0-DQS7}$ $\overline{DQS0-DQS7}$	In/Out	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
V_{DD} , V_{DD} SPD, V_{SS}	Supply	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	In/Out	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.
SA0~SA1	Input	Address pins used to select the Serial Presence Detect base address.
TEST	In/Out	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules(SO-DIMMs).

7.0 Functional Block Diagram :

7.1 2GB, 256Mx64 Module - M470T5663RZ3

(Populated as 2 rank of x8 DDR2 SDRAMs)

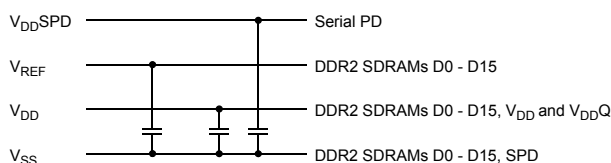


* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	8 DDR2 SDRAMs
*CK1/CK1	8 DDR2 SDRAMs

* Wire per Clock Loading
Table/Wiring Diagrams

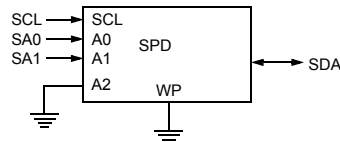
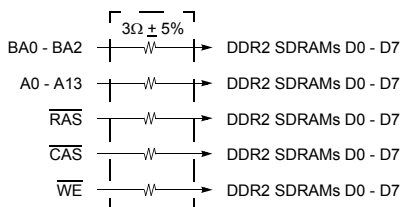
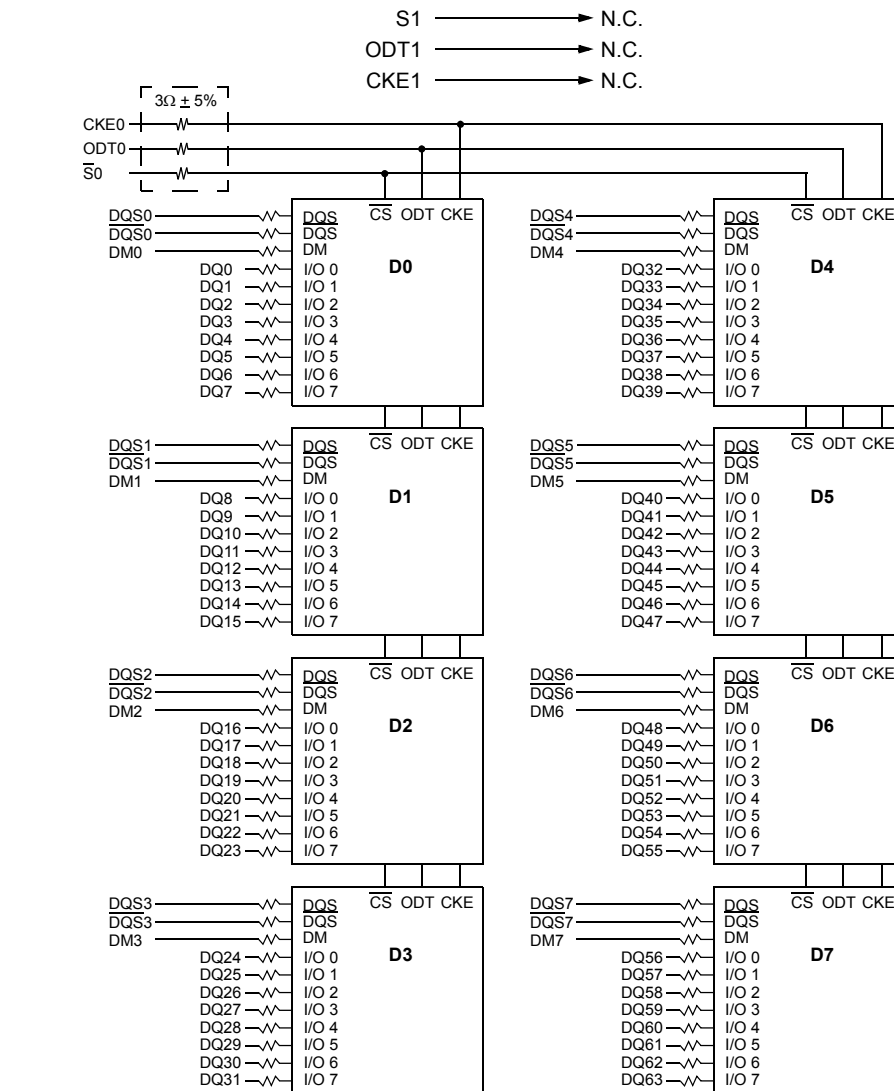
Note :

1. DQ, DM, DQS/DQS resistors : 22 Ohms $\pm$ 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 10.0 Ohms $\pm$ 5%.



7.2 1GB, 128Mx64 Module - M470T2863RZ3

(Populated as 1 rank of x8 DDR2 SDRAMs)

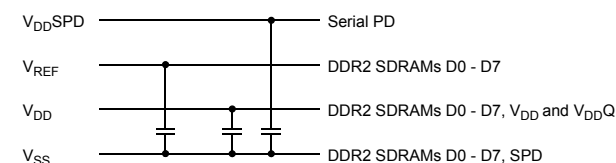


* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	4 DDR2 SDRAMs
*CK1/CK1	4 DDR2 SDRAMs

* Wire per Clock Loading
Table/Wiring Diagrams

Note :

1. DQ, DM, DQS/DQS resistors : 22 Ohms $\pm$ 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 3.0 Ohms $\pm$ 5%.



8.0 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	- 1.0 V ~ 2.3 V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.

9.0 AC & DC Operating Conditions

9.1 Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	mV	1,2
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	3

Symbol	Parameter	Rating		Units	Notes
		Min.	Max.		
V_{DDSPD}	Core Supply Voltage	1.7	3.6	V	5

Note : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD} .

- The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
- Peak to peak AC noise on V_{REF} may not exceed $\pm 2\% V_{REF}(DC)$.
- V_{TT} of transmitting device must track V_{REF} of receiving device.
- AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDL} tied together.
- SODIMMs that include an optional temperature sensor may require a restricted V_{DDSPD} operating voltage range for proper operation of the temperature sensor. Refer to the thermal sensor specification for details regarding the supported voltage range. All other functions of the SODIMM SPD are supported across the full V_{DDSPD} range.

9.2 Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature	0 to 95	°C	1, 2

Note :

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period ($t_{REFI}=3.9\text{ us}$) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

9.3 Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH}(DC)$	DC input logic high	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V	
$V_{IL}(DC)$	DC input logic low	- 0.3	$V_{REF} - 0.125$	V	

9.4 Input AC Logic Level

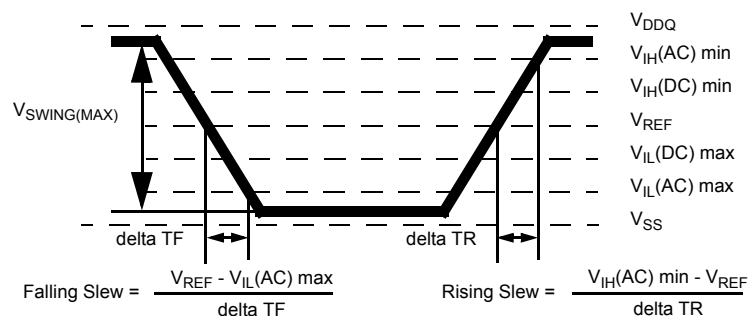
Symbol	Parameter	DDR2-667, DDR2-800		Units
		Min.	Max.	
$V_{IH}(AC)$	AC input logic high	$V_{REF} + 0.200$		V
$V_{IL}(AC)$	AC input logic low		$V_{REF} - 0.200$	V

9.5 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	$0.5 * V_{DDQ}$	V	1
$V_{SWING}(MAX)$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Note:

1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}(AC)$ level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH}(AC)$ min for rising edges and the range from V_{REF} to $V_{IL}(AC)$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from $V_{IL}(AC)$ to $V_{IH}(AC)$ on the positive transitions and $V_{IH}(AC)$ to $V_{IL}(AC)$ on the negative transitions.



< AC Input Test Signal Waveform >

10.0 IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Units	Note
IDD0	Operating one bank active-precharge current; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RASmin}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD1	Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RASmin}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD2P	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2Q	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2N	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD3P	Active power-down current; All banks open; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	mA
		Slow PDN Exit MRS(12) = 1	mA
IDD3N	Active standby current; All banks open; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4W	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4R	Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD5B	Burst auto refresh current; $t_{CK} = t_{CK}(IDD)$; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD6	Self refresh current; CK and CK\ at 0V; CKE $\leq 0.2V$; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA
		Low Power	mA
IDD7	Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD}(IDD) - 1 \cdot t_{CK}(IDD)$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RRD} = t_{RRD}(IDD)$, $t_{FAW} = t_{FAW}(IDD)$, $t_{RCD} = 1 \cdot t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	mA	

11.0 Operating Current Table

11.1 M470T5663RZ3 : 2GB(128Mx8 *16) Module

(TA=0°C, VDD= 1.9V)

Symbol	800@CL=6	667@CL=5	Unit	Notes
	CF7	CE6		
IDD0	920	880	mA	
IDD1	1,000	960	mA	
IDD2P	240	240	mA	
IDD2Q	480	480	mA	
IDD2N	560	560	mA	
IDD3P-F	560	560	mA	
IDD3P-S	288	288	mA	
IDD3N	800	760	mA	
IDD4W	1,280	1,160	mA	
IDD4R	1,520	1,360	mA	
IDD5	1,720	1,680	mA	
IDD6	240	240	mA	
IDD7	2,560	2,400	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

11.2 M470T2863RZ3 : 1GB(128Mx8 *8) Module

(TA=0°C, VDD= 1.9V)

Symbol	800@CL=6	667@CL=5	Unit	Notes
	CF7	CE6		
IDD0	640	600	mA	
IDD1	720	680	mA	
IDD2P	120	120	mA	
IDD2Q	240	240	mA	
IDD2N	280	280	mA	
IDD3P-F	280	280	mA	
IDD3P-S	144	144	mA	
IDD3N	520	480	mA	
IDD4W	1,000	880	mA	
IDD4R	1,240	1,080	mA	
IDD5	1,440	1,400	mA	
IDD6	120	120	mA	
IDD7	2,280	2,120	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

12.0 Input/Output Capacitance

(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A=25°C)

Parameter	Symbol	Min	Max	Min	Max	Units
Non-ECC		M470T5663RZ3		M470T2863RZ3		
Input capacitance, CK and $\overline{\text{CK}}$	CCK	-	48	-	32	pF
Input capacitance, CKE , $\overline{\text{CS}}$, Addr , $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	CI	-	42	-	42	
Input/output capacitance, DQ , DM , DQS , $\overline{\text{DQS}}$	CIO	-	9	-	5.5	

* DM is internally loaded to match DQ and DQS identically.

13.0 Electrical Characteristics & AC Timing for DDR2-800/667

(0 °C ≤ T_{OPER} ≤ 95 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

13.1 Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	0 °C ≤ T _{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	μs
		85 °C < T _{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	μs

13.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR2-800(F7)		DDR2-667(E6)		Units
Bin(CL - tRCD - tRP)	6 - 6- 6		5 - 5 - 5		
Parameter	min	max	min	max	
tCK, CL=3	-	-	5	8	ns
tCK, CL=4	3.75	8	3.75	8	ns
tCK, CL=5	3	8	3	8	ns
tCK, CL=6	2.5	8	-	-	ns
tRCD	15	-	15	-	ns
tRP	15	-	15	-	ns
tRC	60	-	60	-	ns
tRAS	45	70000	45	70000	ns

13.3 Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

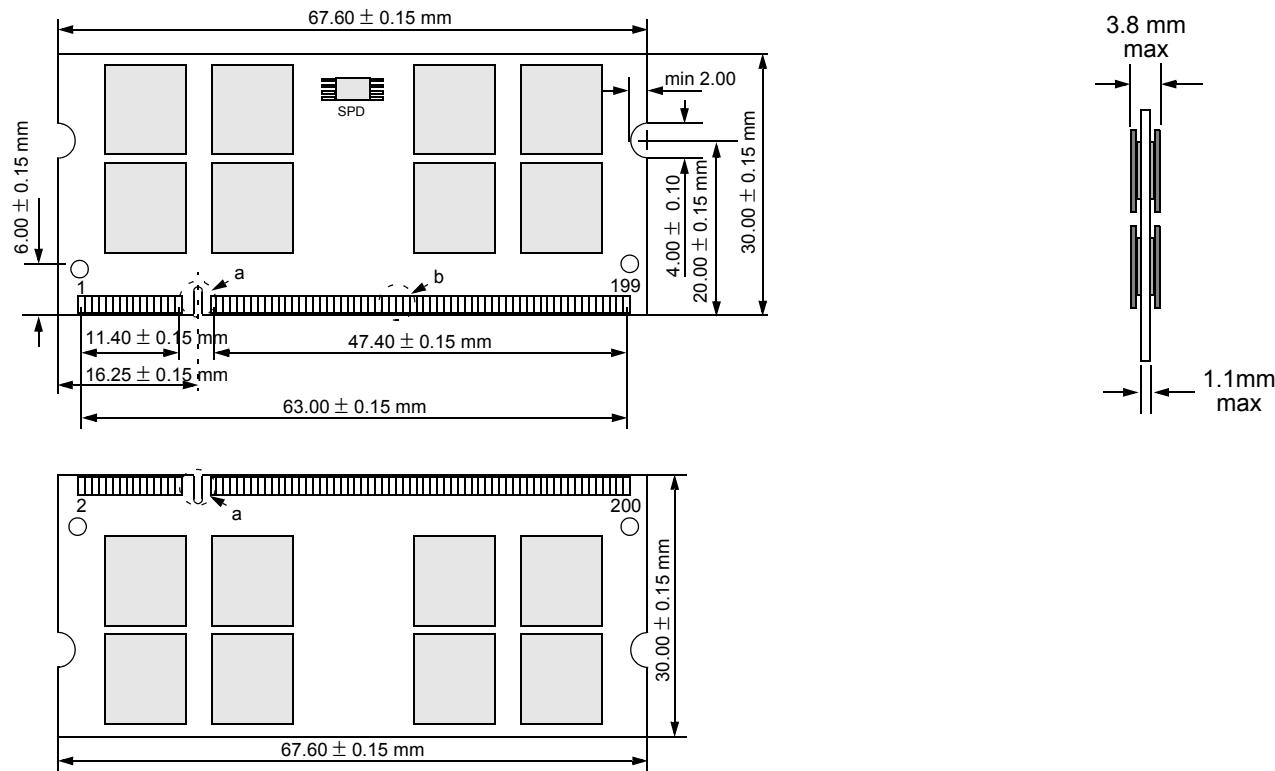
Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
DQ output access time from $\overline{\text{CK}}/\overline{\text{CK}}$	tAC	-400	400	-450	450	ps	40
DQS output access time from $\overline{\text{CK}}/\overline{\text{CK}}$	tDQSCK	-350	350	-400	400	ps	40
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
CK half pulse period	tHP	Min(tCL(abs), tCH(abs))	x	Min(tCL(abs), tCH(abs))	x	ps	37
Average clock period	tCK(avg)	2500	8000	3000	8000	ps	35,36
DQ and DM input hold time	tDH(base)	125	x	175	x	ps	6,7,8,21,28,31
DQ and DM input setup time	tDS(base)	50	x	100	x	ps	6,7,8,20,28,31
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK(avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK(avg)	
Data-out high-impedance time from $\overline{\text{CK}}/\overline{\text{CK}}$	tHZ	x	tAC(max)	x	tAC(max)	ps	18,40
DQS/ $\overline{\text{DQS}}$ low-impedance time from $\overline{\text{CK}}/\overline{\text{CK}}$	tLZ(DQS)	tAC(min)	tAC(max)	tAC(min)	tAC(max)	ps	18,40
DQ low-impedance time from $\overline{\text{CK}}/\overline{\text{CK}}$	tLZ(DQ)	2* tAC(min)	tAC(max)	2* tAC(min)	tAC(max)	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	ps	13
DQ hold skew factor	tQHS	x	300	x	340	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	39
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	-0.25	0.25	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30
Mode register set command cycle time	tMRD	2	x	2	x	nCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Write preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	
Address and control input hold time	tIH(base)	250	x	275	x	ps	5,7,9,23,29
Address and control input setup time	tIS(base)	175	x	200	x	ps	5,7,9,22,29
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4,32
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4,32

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	35	x	37.5	x	ns	32
Four Activate Window for 2KB page size products	tFAW	45	x	50	x	ns	32
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2	x	2	x	nCK	
Write recovery time	tWR	15	x	15	x	ns	32
Auto precharge write recovery + precharge time	tDAL	WR + tnRP	x	WR + tnRP	x	nCK	33
Internal write to read command delay	tWTR	7.5	x	7.5	x	ns	24,32
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3,32
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	32
Exit self refresh to a read command	tXSRD	200	x	200	x	nCK	
Exit precharge power down to any command	tXP	2	x	2	x	nCK	
Exit active power down to read command	tXARD	2	x	2	x	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL	x	7 - AL	x	nCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	nCK	27
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2*tCK(avg) +tAC(max)+1	tAC(min)+2	2*tCK(avg) +tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5*tCK(avg) +tAC(max)+1	tAC(min)+2	2.5*tCK(avg) +tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	nCK	
ODT power down exit latency	tAXPD	8	x	8	x	nCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(avg) +tIH	x	tIS+tCK(avg) +tIH	x	ns	15

14.0 Physical Dimensions :

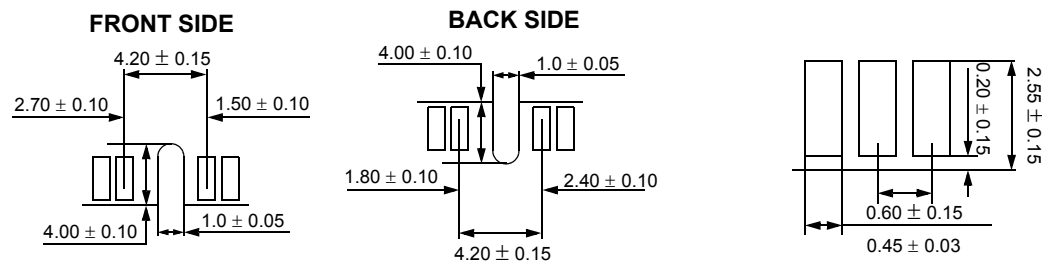
14.1 128Mbx8 based 256Mx64 Module (2 Rank) - M470T5663RZ3

Units : Millimeters



DETAIL a

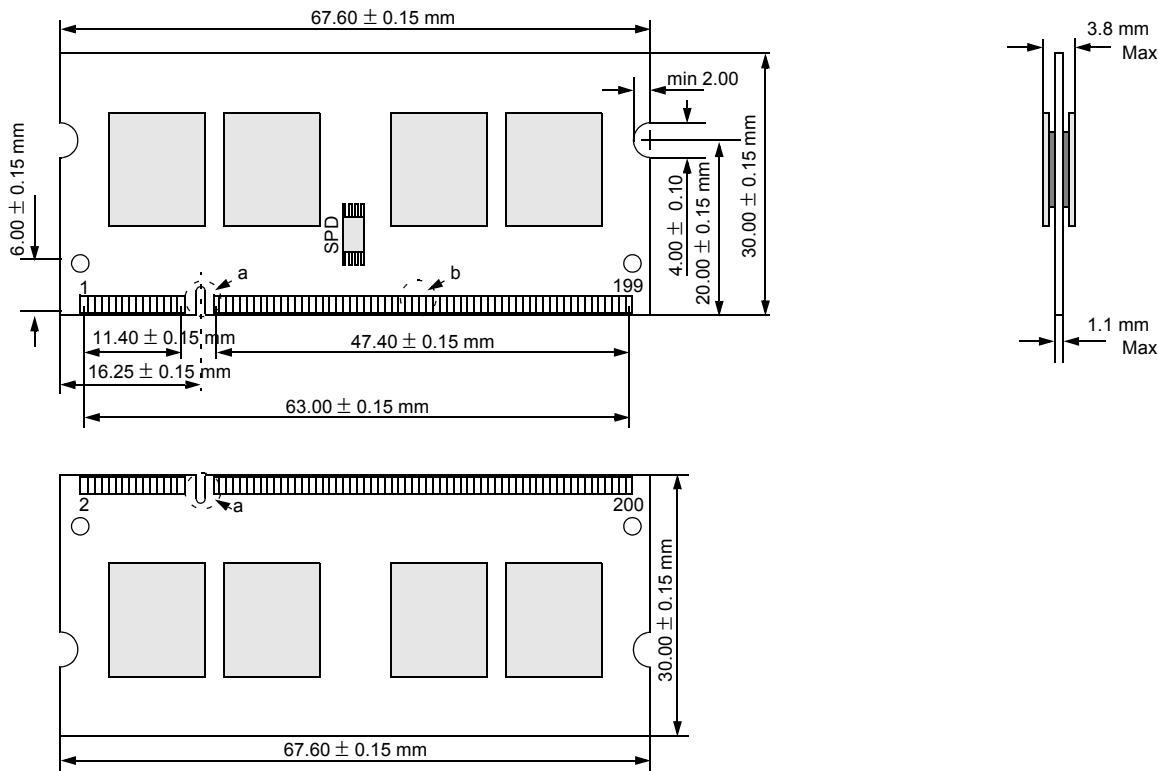
DETAIL b



The used device is 128M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T1G084QR

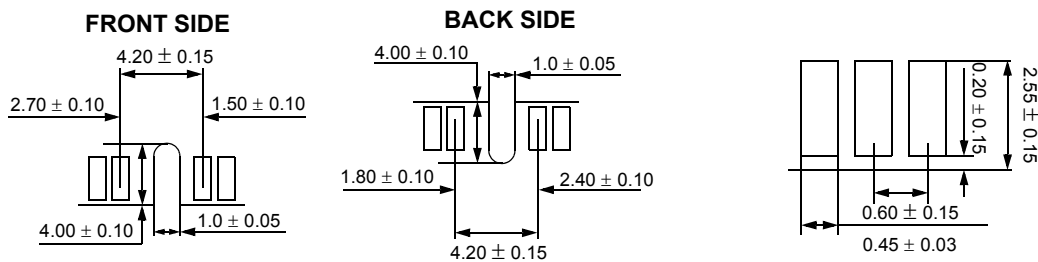
14.2 128Mbx8 based 128Mx64 Module (1 Rank) - M470T2863RZ3

Units : Millimeters



DETAIL a

DETAIL b



The used device is 128M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T1G084QR