Features

- **Fast Read Access Time - 70ns**
- **Automatic Page Write Operation**
  Internal Address and Data Latches for 64 Bytes
  Internal Control Timer
- **Fast Write Cycle Times**
  Page Write Cycle Time: 10ms or 3ms maximum
  1 to 64 Byte Page Write Operation
- **Low Power Dissipation**
  80mA Active Current
  3mA Standby Current (AT28HC256L)
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- **High Reliability CMOS Technology**
  Endurance: 10^4 or 10^5 Cycles
  Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

256 (32K x 8) High Speed CMOS E²PROM

2

Description

The AT28HC256/L is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the AT28HC256 offers access times to 70ns with power dissipation of just 440mW. When the AT28HC256L is deselected, the standby current is less than 5mA.
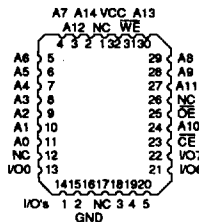
The AT28HC256/L is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC256/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E²PROM for device identification or tracking.

Pin Configurations

Pin Name	Function
A0 - A14	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP package pinout:

A14	1	28	VCC
A12	2	27	WE
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19	I/O7
I/O0	11	18	I/O6
I/O1	12	17	I/O5
I/O2	13	16	I/O4
GND	14	15	I/O3

PLCC package:

Top pins: A7 A14 VCC A13 A12 NC WE

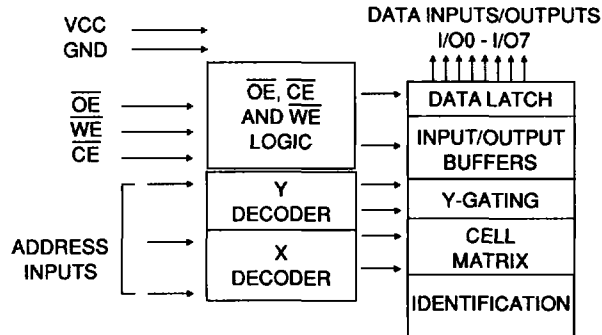|			
A6	5	29	A8
A5	6	28	A9
A4	7	27	A11
A3	8	26	NC
A2	9	25	OE
A1	10	24	A10
A0	11	23	CE
NC	12	22	I/O7
I/O0	13	21	I/O6

Bottom pins: I/O's 1 2 NC 3 4 5 GND

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram

Device Operation

READ: The AT28HC256/L is accessed like a Static RAM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the WE or CE input with CE or WE low (respectively) and OE high initiates a write cycle. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28HC256/L allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on WE (or CE) within 150μs of the low to high transition of WE (or CE) of the preceding byte. If a high to low transition is not detected within 150μs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of WE (or CE). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28HC256/L features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to DATA Polling the AT28HC256/L provides another method for determining the

end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256/L in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of OE low, CE high or WE high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the WE or CE inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28HC256/L. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 bytes of E²PROM memory are available to the user for device identification. By raising A9 to 12±0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

AT28HC256/L

Absolute Maximum Ratings*

Temperature Under Bias................-55°C to +125°C	
Storage Temperature......................-65°C to +150°C	
All Input Voltages (including N.C. Pins) with Respect to Ground ....-0.6V to +6.25V	
All Output Voltages with Respect to Ground ....-0.6V to V_{CC} +0.6V	
Voltage on $\overline{OE}$ and A9 with Respect to Ground ....-0.6V to +13.5V	

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28HC256-70	AT28HC256L-90	AT28HC256-90	AT28HC256L-12 AT28HC256-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	μA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	μA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V	AT28HC256L		3	mA
			AT28HC256		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE}$=-3.0V to V_{CC} + 1V	AT28HC256L		300	μA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=6.0mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-4mA		2.4		V

A.C. Read Characteristics

| Symbol	Parameter	AT28HC256-70 Min	AT28HC256-70 Max	AT28C256-90 AT28HC256L-90 Min	AT28C256-90 AT28HC256L-90 Max	AT28HC256-12 AT28HC256L-12 Min	AT28HC256-12 AT28HC256L-12 Max	Units
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE} [1]	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE} [2]	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF} [3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms
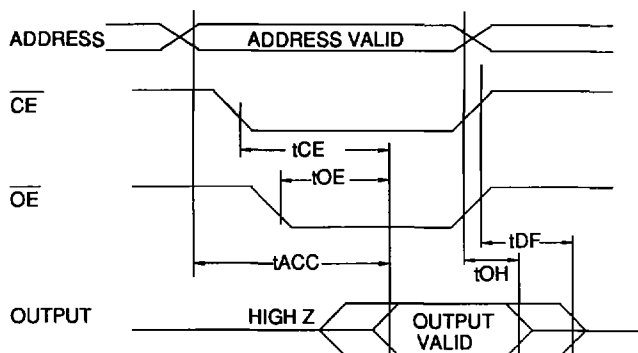
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L = 5pF$).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level

t_R, t_F < 5ns
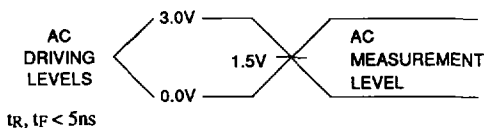
Output Test Load
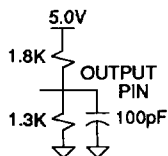
Pin Capacitance   (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

AT28HC256/L

A.C. Write Characteristics

Symbol	Parameter		Min	Max	Units
tAS, tOES	Address, $\overline{OE}$ Set-up Time		0		ns
tAH	Address Hold Time		50		ns
tCS	Chip Select Set-up Time		0		ns
tCH	Chip Select Hold Time		0		ns
tWP	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		ns
tDS	Data Set-up Time		50		ns
tDH, tOEH	Data, $\overline{OE}$ Hold Time		0		ns
tDV	Time to Data Valid		NR[1]		
twc	Write Cycle Time	AT28HC256		10	ms
		AT28HC256F		3.0	ms

Note: 1. NR = No Restiction

A.C. Write Waveforms- $\overline{WE}$ Controlled
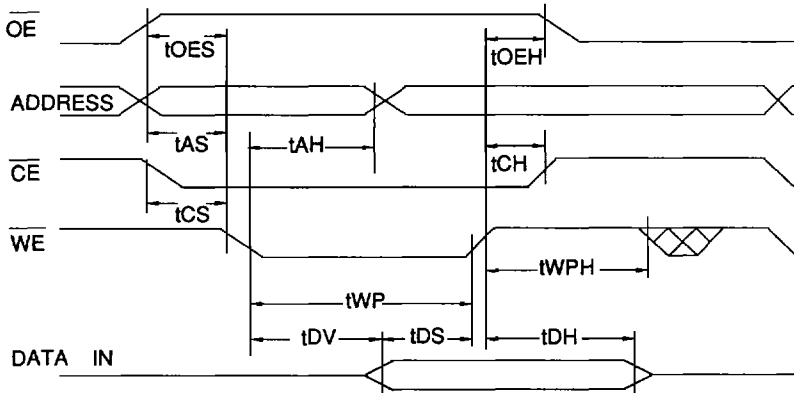
## A.C. Write Load Waveforms- $\overline{CE}$ Controlled
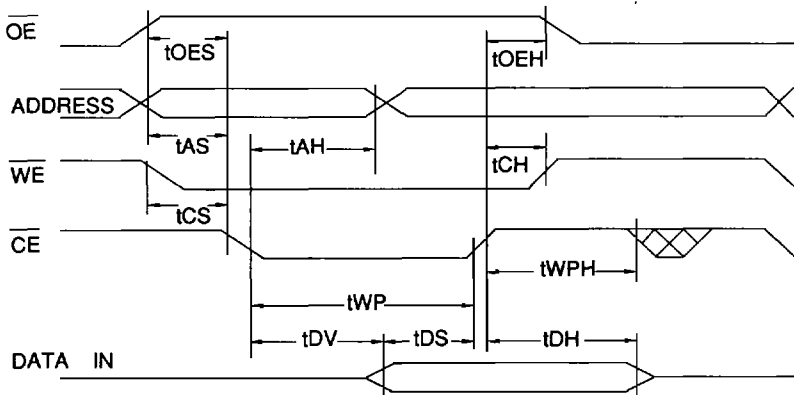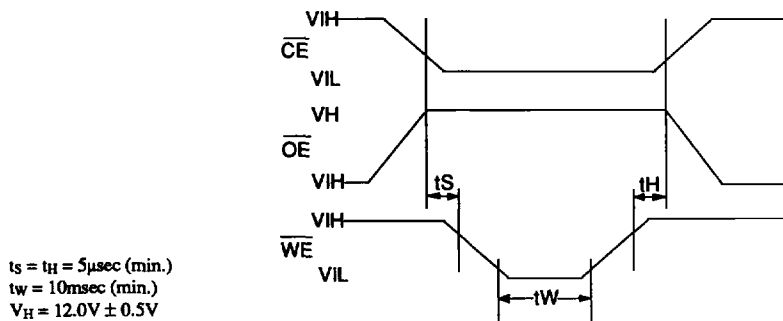
Page Mode Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
twc	Write Cycle Time	AT28HC256		5	10	ms
		AT28HC256F		2	3.0	ms
tAS	Address Set-up Time		0			ns
tAH	Address Hold Time		50			ns
tDS	Data Set-up Time		50			ns
tDH	Data Hold Time		0			ns
tWP	Write Pulse Width		100			ns
tBLC	Byte Load Cycle Time				150	μs
tWPH	Write Pulse Width High		50			ns

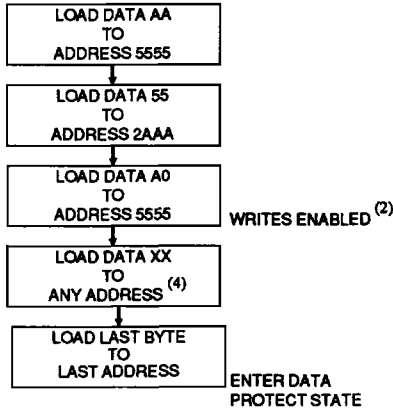## Page Mode Write Waveforms
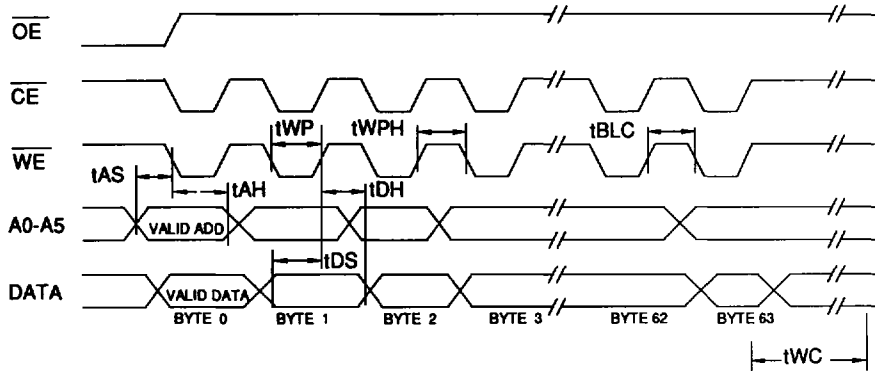
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).

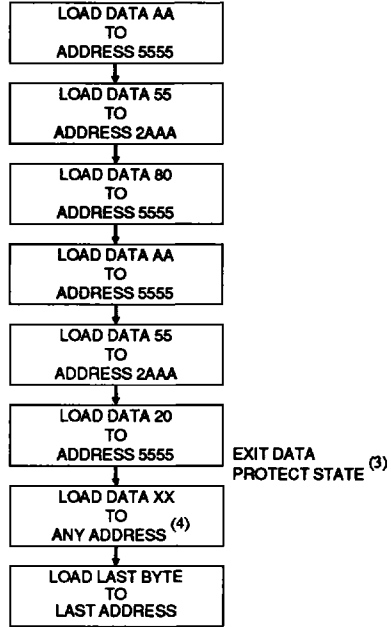$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

$t_S = t_H = 5\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

AT28HC256/L

Software Data Protection Enable Algorithm [1]

```
LOAD DATA AA
TO
ADDRESS 5555
        ↓
LOAD DATA 55
TO
ADDRESS 2AAA
        ↓
LOAD DATA A0
TO
ADDRESS 5555        WRITES ENABLED [2]
        ↓
LOAD DATA XX
TO
ANY ADDRESS [4]
        ↓
LOAD LAST BYTE
TO
LAST ADDRESS        ENTER DATA
                    PROTECT STATE
```
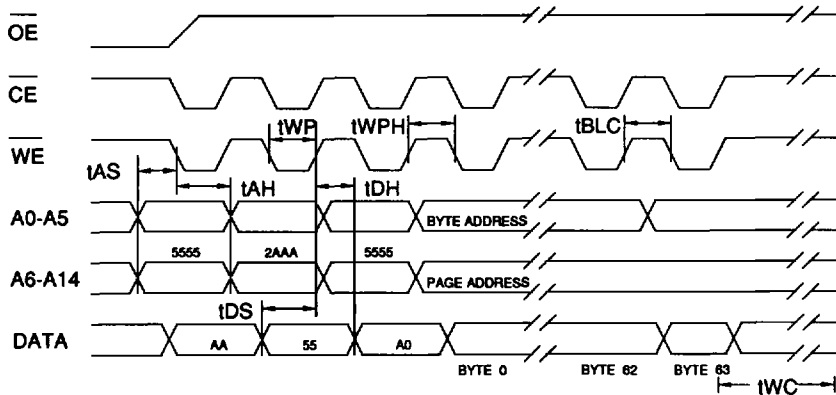
Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Data Protection Disable Algorithm [1]

```
LOAD DATA AA
TO
ADDRESS 5555
        ↓
LOAD DATA 55
TO
ADDRESS 2AAA
        ↓
LOAD DATA 80
TO
ADDRESS 5555
        ↓
LOAD DATA AA
TO
ADDRESS 5555
        ↓
LOAD DATA 55
TO
ADDRESS 2AAA
        ↓
LOAD DATA 20
TO
ADDRESS 5555        EXIT DATA
                    PROTECT STATE [3]
        ↓
LOAD DATA XX
TO
ANY ADDRESS [4]
        ↓
LOAD LAST BYTE
TO
LAST ADDRESS
```

Software Protected Write Cycle Waveforms

Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
tDH	Data Hold Time	0			ns
tOEH	$\overline{OE}$ Hold Time	0			ns
tOE	$\overline{OE}$ to Output Delay			100	ns
tWR	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms
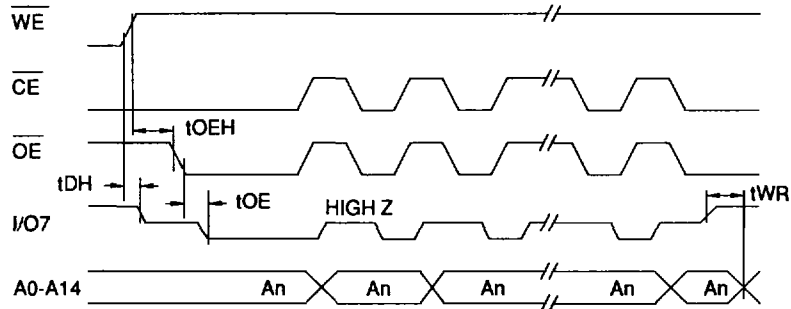
Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
tDH	Data Hold Time	10			ns
tOEH	$\overline{OE}$ Hold Time	10			ns
tOE	$\overline{OE}$ to Output Delay			100	ns
tOEHP	$\overline{OE}$ High Pulse	150			ns
tWR	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.
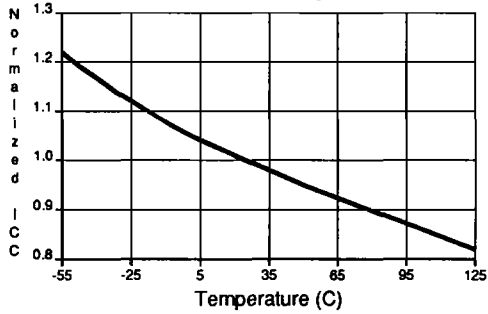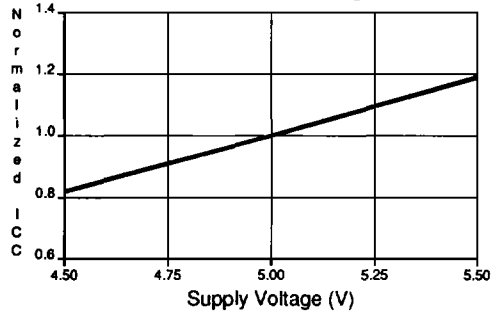
Toggle Bit Waveforms
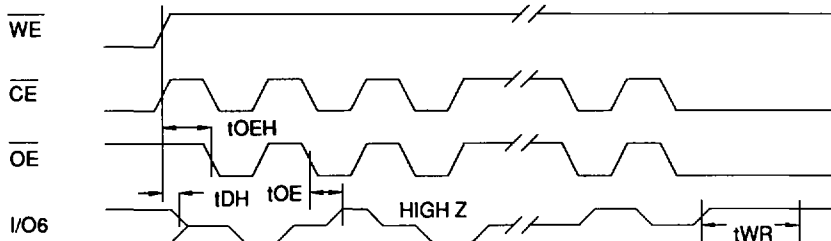
Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

2

NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

Normalized ICC

1.3
1.2
1.1
1.0
0.9
0.8

-55   -25   5   35   65   95   125

Temperature (C)

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

Normalized ICC

1.4
1.2
1.0
0.8
0.6

4.50   4.75   5.00   5.25   5.50

Supply Voltage (V)

NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY

Normalized ICC

1.1
1.0
0.9
0.8
0.7
0.6

Vcc = 5V
T = 25C

0   2   4   6   8   10

Frequency (MHz)

Ordering Information

tACC (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70DC AT28HC256(E,F)-70JC AT28HC256(E,F)-70LC AT28HC256(E,F)-70PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC256(E,F)-70DI AT28HC256(E,F)-70JI AT28HC256(E,F)-70LI AT28HC256(E,F)-70PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
90	80	60	AT28HC256(E,F)-90DC AT28HC256(E,F)-90FC AT28HC256(E,F)-90JC AT28HC256(E,F)-90LC AT28HC256(E,F)-90PC AT28HC256(E,F)-90UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-90DI AT28HC256(E,F)-90FI AT28HC256(E,F)-90JI AT28HC256(E,F)-90LI AT28HC256(E,F)-90PI AT28HC256(E,F)-90UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-90DM AT28HC256(E,F)-90FM AT28HC256(E,F)-90LM AT28HC256(E,F)-90UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC256(E,F)-12DC AT28HC256(E,F)-12FC AT28HC256(E,F)-12JC AT28HC256(E,F)-12LC AT28HC256(E,F)-12PC AT28HC256(E,F)-12UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-12DI AT28HC256(E,F)-12FI AT28HC256(E,F)-12JI AT28HC256(E,F)-12LI AT28HC256(E,F)-12PI AT28HC256(E,F)-12UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-12DM AT28HC256(E,F)-12FM AT28HC256(E,F)-12LM AT28HC256(E,F)-12UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

AT28HC256/L

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Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	60	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information

tACC (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256L(E,F)-90DC AT28HC256L(E,F)-90FC AT28HC256L(E,F)-90JC AT28HC256L(E,F)-90LC AT28HC256L(E,F)-90PC AT28HC256L(E,F)-90UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-90DI AT28HC256L(E,F)-90FI AT28HC256L(E,F)-90JI AT28HC256L(E,F)-90LI AT28HC256L(E,F)-90PI AT28HC256L(E,F)-90UI AT28HC256L(E,F)-W	28D6 28F 32J 32L 28P6 28U DIE	Industrial (-40°C to 85°C)
120	80	0.3	AT28HC256L(E,F)-12DC AT28HC256L(E,F)-12FC AT28HC256L(E,F)-12JC AT28HC256L(E,F)-12LC AT28HC256L(E,F)-12PC AT28HC256L(E,F)-12UC AT28HC256L-W	28D6 28F 32J 32L 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-12DI AT28HC256L(E,F)-12FI AT28HC256L(E,F)-12JI AT28HC256L(E,F)-12LI AT28HC256L(E,F)-12PI AT28HC256L(E,F)-12UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256L(E,F)-12DM AT28HC256L(E,F)-12FM AT28HC256L(E,F)-12LM AT28HC256L(E,F)-12UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256L(E,F)-12DM/883 AT28HC256L(E,F)-12FM/883 AT28HC256L(E,F)-12LM/883 AT28HC256L(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

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