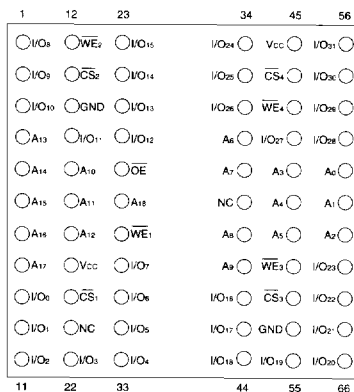
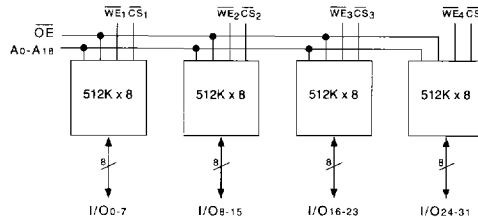


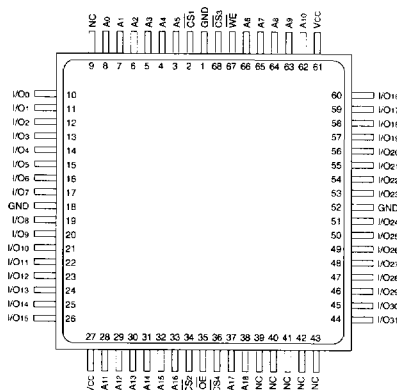
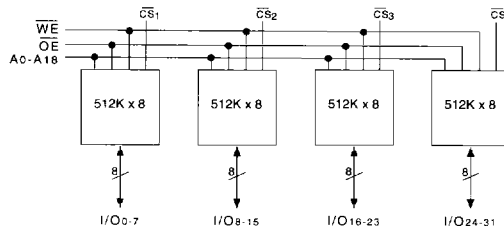
**512Kx32 SRAM MODULE** *PRELIMINARY****FEATURES**

- Access Times of 55nS to 120nS
 - Packaging
 - 66-pin, PGA Type, 1.38 inch square HIP, Hermetic Ceramic Package
 - 68 lead, 40 mm Hermetic CQFP
 - Organized as 512Kx32; User Configurable as 1024Kx16 or 2Mx8.
 - Battery Back-Up Operation
 - Commercial, Industrial and Military Temperature Ranges
 - TTL Compatible Inputs and Outputs
 - 2.7V to 5.5 Volt Supply Voltage Range
 - Low Power CMOS
 - Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
 - Weight
 - WS512K32-XHX - 13 grams typical
 - WS512K32-XG4X - 20 grams typical
- * This data sheet describes a product under development and is subject to change without notice.*

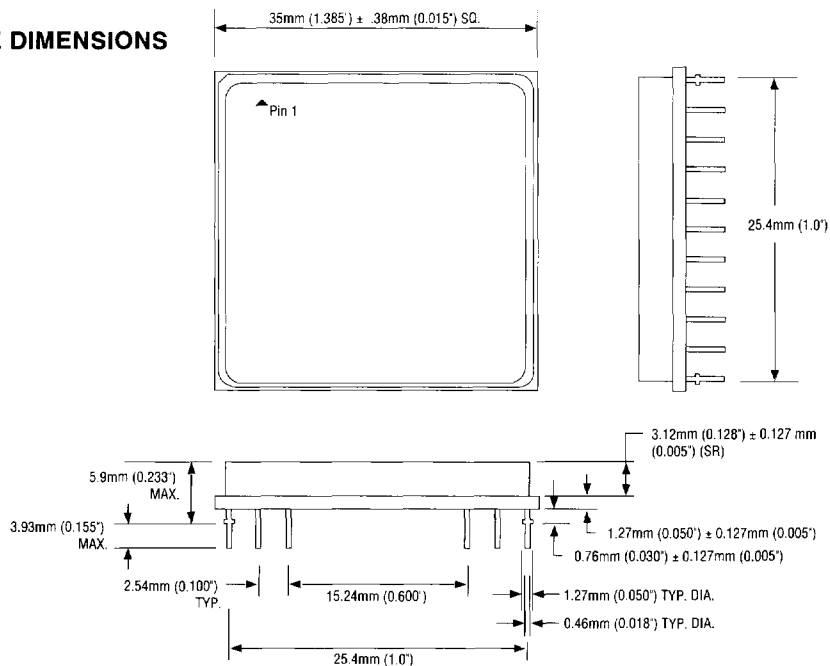
2**SRAM MODULES****FIG. 1 PIN CONFIGURATION FOR WS512K32N-XHX****TOP VIEW****BLOCK DIAGRAM****PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

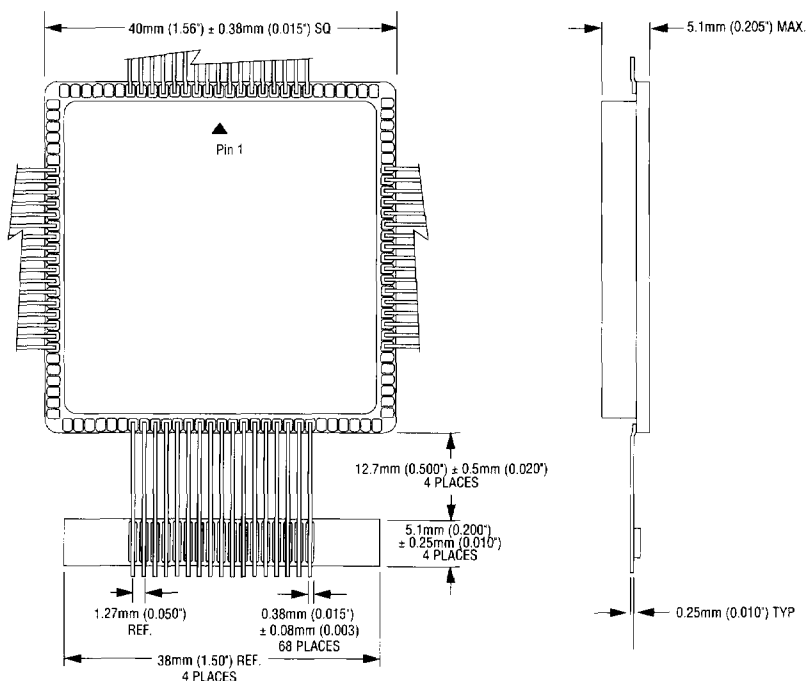
S3D2101

FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4X**TOP VIEW****BLOCK DIAGRAM****PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE	Write Enable
CS1-4	Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

**FIG. 3**
PACKAGE DIMENSIONS
(16A07)

This package is also available without shoulders on the corner pins.

FIG. 4
PACKAGE DIMENSIONS
(14A15)

**ORDERING INFORMATION****W S 512K 32 X - XXX X X****DEVICE GRADE:**

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to 85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H = Ceramic hex-in-line package
- HS = Ceramic hex-in-line package,
no shoulders
- G4 = 40 mm Ceramic Quad Flat Pack

ACCESS TIME IN nS**IMPROVEMENT MARK:**

- N = No Connect at pin 21, and 39
- Blank = GND at 21, and 39

ORGANIZATION, 512Kx32

User configurable as 1024Kx16 or 2Mx8

SRAM**WHITE MICROELECTRONICS**



NOTES:

**512Kx32 SRAM MODULE** PRELIMINARY***FEATURES**

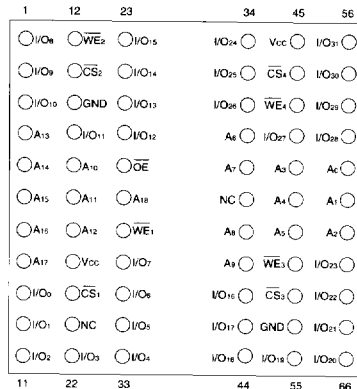
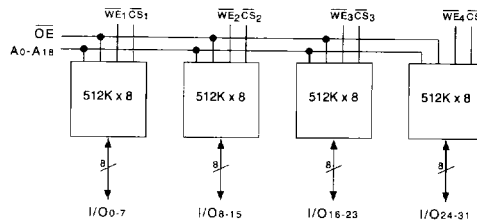
- Access Times of 25nS to 45nS
- Packaging
 - 66-pin, PGA Type, 1.38 inch square HIP, Hermetic Ceramic Package
 - 68 lead, 40 mm Hermetic CQFP Package
- Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8.
- Battery Back-Up Operation

- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 3.3 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
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 - WS512K32-XG4X - 20 grams typical

* This data sheet describes a product under development and is subject to change, without notice.

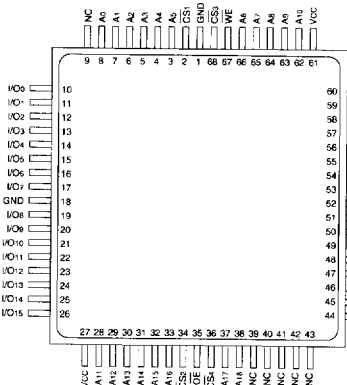
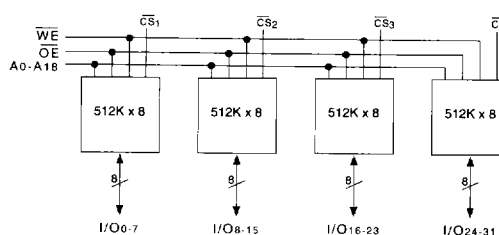
2

SRAM MODULES

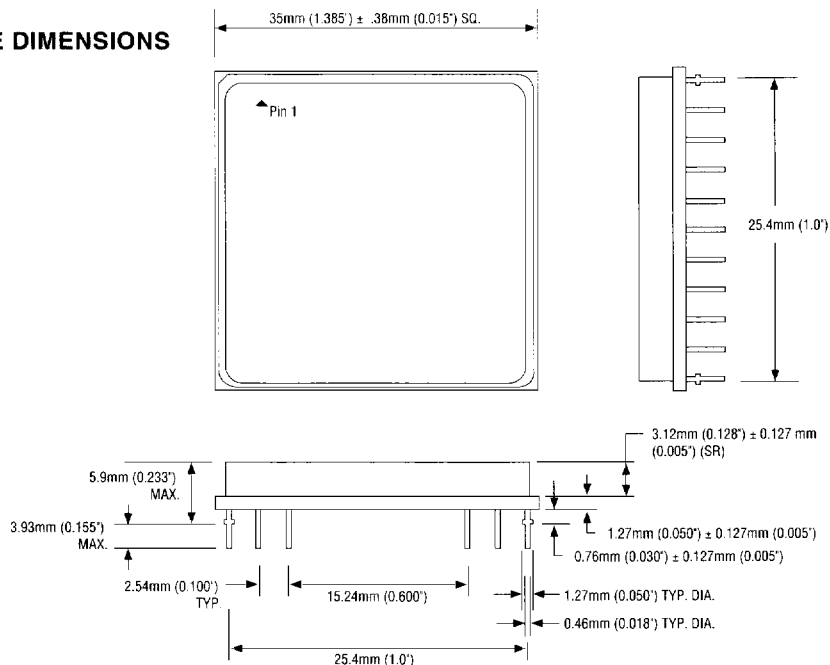
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TOP VIEW**BLOCK DIAGRAM****PIN DESCRIPTION**

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GND	Ground
NC	Not Connected

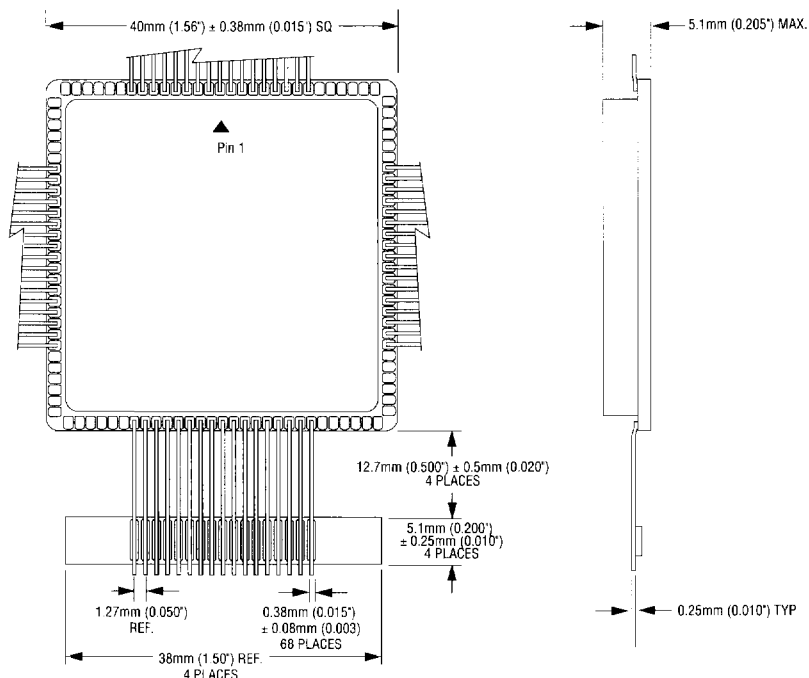
S3D2101

FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4X
TOP VIEW**BLOCK DIAGRAM****PIN DESCRIPTION**

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ORGANIZATION, 512Kx32

User configurable as 1024Kx16 or 2Mx8

SRAM**WHITE MICROELECTRONICS****2****SRAM MODULES**