NEC

MOS INTEGRATED CIRCUIT

μPD178004A, 178006A, 178016A, 178018A

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD178004A, 178006A, 178016A and 178018A are 8-bit single-chip CMOS microcontrollers that incorporate hardware for digital tuning systems.

The CPU uses the 78K/0 architecture, which makes it easy to implement high-speed access to internal memory and control of peripheral hardware. Also, the instructions used are the high-speed 78K/0 instructions, suitable for system control.

The rich assortment of peripheral hardware includes an input/output port, 8-bit timer, A/D converter, serial interface, power-ON clear circuits, as well as a pre-scaler for digital tuning, a PLL frequency synthesizer and a frequency counter.

The μPD178P018A, one-time PROM or EPROM versions which can be operated in the same supply voltage range as for the mask ROM versions, and various development tools, are also available.

For more information on functions, refer to the following User's Manuals. Be sure to read them when designing.

μPD178018A Subseries User's Manual: to be prepared
78K/0 Series User's Manual Instruction: U12326E

FEATURES

- Internal high-capacity ROM and RAM

Product Name \ Items	Program Memory	Data Memory		
	ROM	Internal High-Speed RAM	Buffer RAM	Internal Expanded RAM
μPD178004A	32 Kbytes	1 024 bytes	32 bytes	Not provided
μPD178006A	48 Kbytes			
μPD178016A				2 048 bytes
μPD178018A	60 Kbytes			

- Instruction Cycle: 0.44 μs (4.5-MHz crystal oscillator used)
- Large array of on-chip peripheral hardware
  General-purpose input/output port, A/D converter, serial interface, timer, frequency counter, power-ON clear circuits.
- On-chip hardware for a PLL frequency synthesizer.
  Dual modulus pre-scaler, programmable divider, phase comparator, charge pump.
- Vector interrupt sources: 17
- Supply Voltage: V_{DD} = 4.5 to 5.5 V (during PLL operation)
  V_{DD} = 3.5 to 5.5 V (during CPU operation, when the system clock is fx/2 or lower)
  V_{DD} = 4.5 to 5.5 V (during CPU operation, when the system clock is fx)

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APPLICATIONS

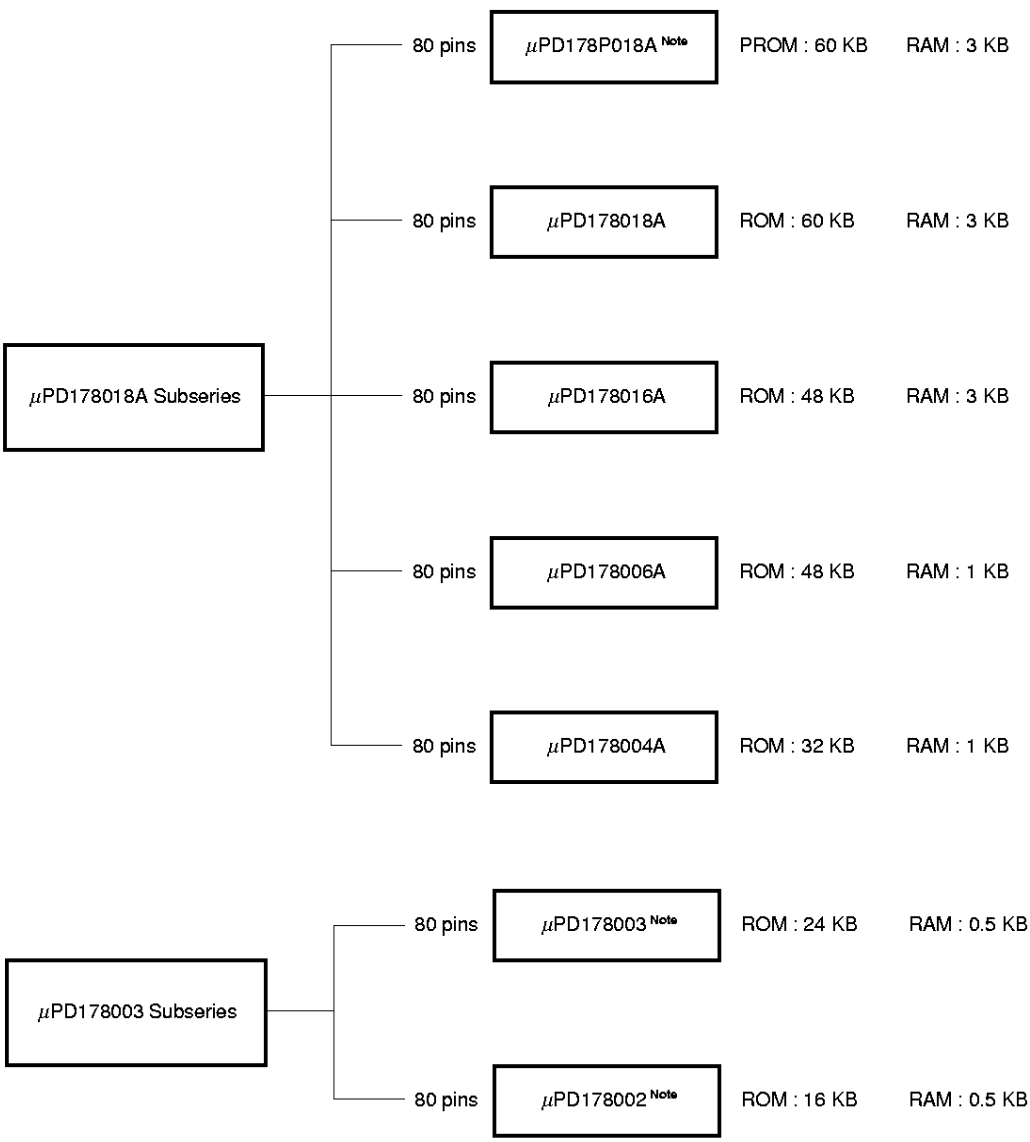
Car stereo, home stereo systems.

ORDERING INFORMATION

Part Number	Package
μPD178004AGC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178006AGC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178016AGC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178018AGC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)

Remark xxx denotes the ROM code number. Also, the ROM code number becomes Exx when the I^2C bus is used.

μPD178018A SUBSERIES AND μPD178003 SUBSERIES EXPANSION



Note Under development

OUTLINE OF FUNCTION

(1/2)

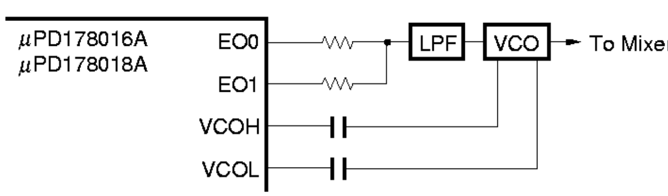
Item		μPD178004A	μPD178006A	μPD178016A	μPD178018A
Internal memory	ROM (ROM configuration)	32 Kbytes (mask ROM)	48 Kbytes (mask ROM)		60 Kbytes (mask ROM)
	High-speed RAM	1 024 bytes			
	Buffer RAM	32 bytes			
	Expansion RAM	Not provided		2 048 bytes	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		With variable instruction execution time function 0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (with 4.5-MHz crystal resonator)			
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc.			
I/O port		Total : 62 pins CMOS input : 1 pin CMOS I/O : 54 pins N-ch open-drain I/O : 4 pins N-ch open-drain output : 3 pins			
A/D converter		8-bit resolution × 6 channels			
Serial interface		• 3-wire/SBI/2-wire/I²C bus **Note** mode selectable : 1 channel • 3-wire serial I/O mode (with automatic transfer/receive function of up to 32 byte) : 1 channel			
Timer		• Basic timer (timer carry FF (10 Hz)) : 1 channel • 8-bit timer/event counter : 2 channels • 8-bit timer (D/A converter: PWM output) : 1 channel • Watchdog timer : 1 channel			
Buzzer (BEEP) output		1.5 kHz, 3 kHz, 6 kHz			
Vectored interrupt Source	Maskable	Internal: 8, external: 7			
	Non-maskable	Internal: 1			
	Software	Internal: 1			
Test input		Internal: 1			

Note When using the I²C bus mode (including when this mode is implemented by program without using the peripheral hardware), consult your local NEC sales representative when you place an order for mask.

(2/2)

Item \ Product name		μPD178004A	μPD178006A	μPD178016A	μPD178018A
PLL frequency synthesizer	Division mode	Two types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOH and VCOL pins)			
	Reference frequency	7 types selectable by program (1, 3, 5, 9, 10, 25, 50 kHz)			
	Charge pump	Error out output: 2 (EO0 and EO1 pins Note 1)			
	Phase comparator	Unlock detectable by program			
Frequency counter		• Frequency measurement • AMIFC pin: for 450-kHz count • FMIFC pin: for 450-kHz/10.7-MHz count			
D/A converter (PWM output)		8-/9-bit resolution × 3 channels (shared by 8-bit timer)			
Standby function		• HALT mode • STOP mode			
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Reset by power-ON clear circuit (3-value detection) • Detection of less than 4.5 V Note 2 (CPU clock: fx) • Detection of less than 3.5 V Note 2 (CPU clock: fx/2 or less and on power application) • Detection of less than 2.5 V Note 2 (in STOP mode)			
Power supply voltage		• V_{DD} = 4.5 to 5.5 V (with PLL operating) • V_{DD} = 3.5 to 5.5 V (with CPU operating, CPU clock: fx/2 or less) • V_{DD} = 4.5 to 5.5 V (with CPU operating, CPU clock: fx)			
Package		• 80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)			

Notes 1. The EO1 pin can be set to high impedance for the μPD178016A and 178018A.
The following shows an application example.



LPF : Low path filter
VCO : Voltage controlled oscillator

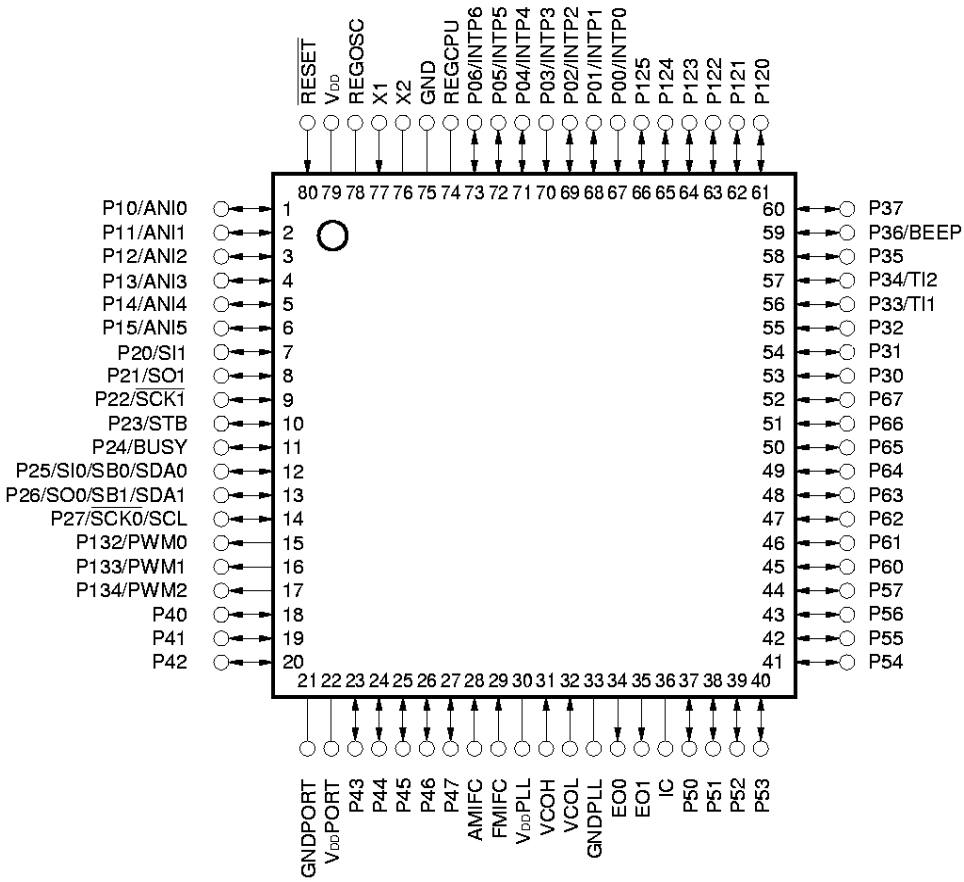
- To lock to a target frequency at high speed
  Setting the EO0 and EO1 pins to error out output improves the output current potential and LPF voltage control potential.
- Normal state
  Setting only the EO0 pin to error out output maintains the LPF stable.

2. These voltage values are maximum values. Reset is actually executed at a voltage lower than these values.

TABLE OF CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-PIN PLASTIC QFP (14 × 14 mm, 0.65 mm pitch)**
  μPD178004AGC-xxx-3B9, 178006AGC-xxx-3B9
  μPD178016AGC-xxx-3B9, 178018AGC-xxx-3B9



Cautions 1. Connect the Internally Connected (IC) pin to GND directly.

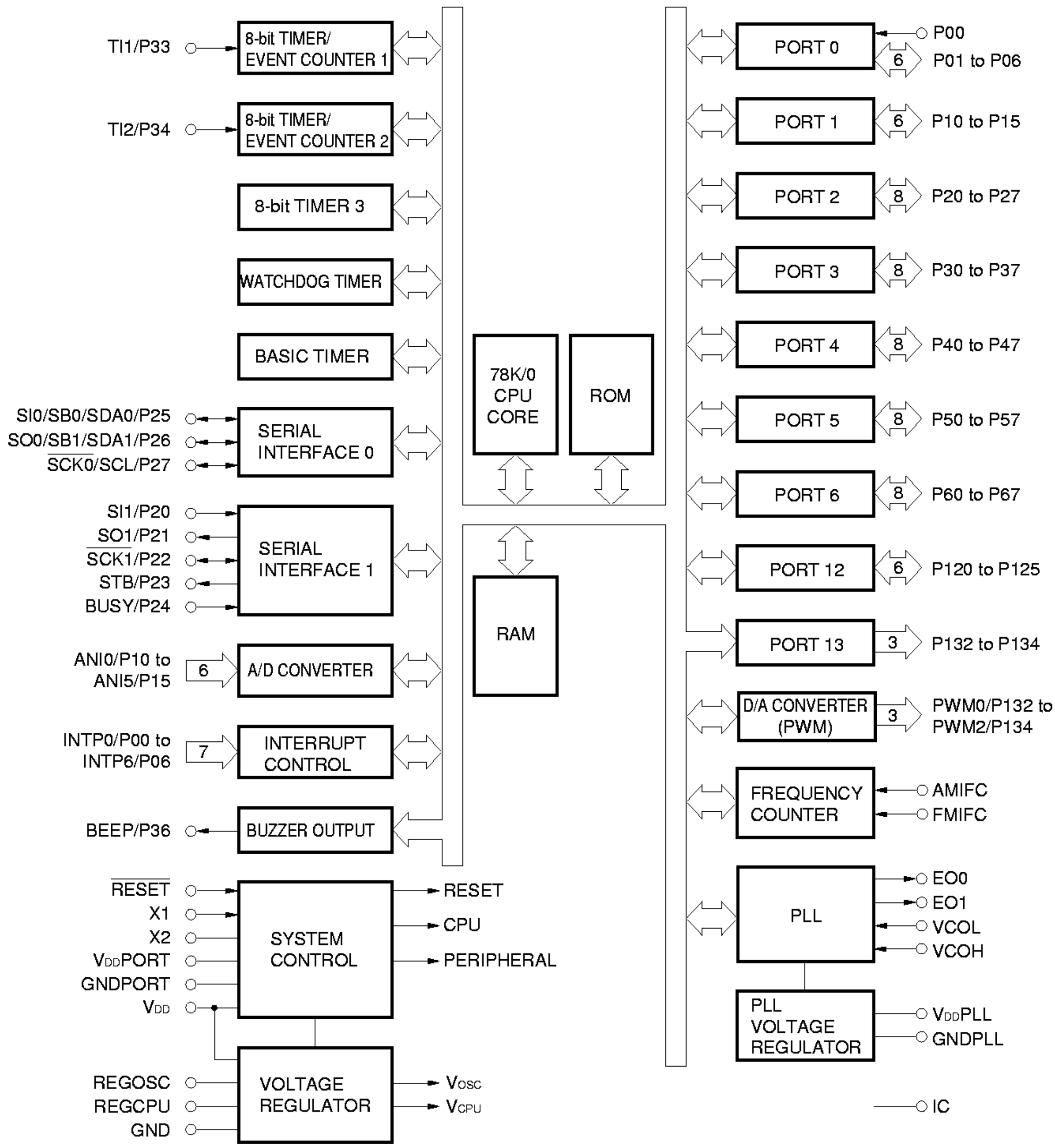
2. Connect V_{DD}PORT and V_{DD}PLL pins to V_{DD}.

3. Connect the GNDPORT and GNDPLL pins to GND.

4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1-μF capacitor.

AMIFC	: AM Intermediate Frequency Counter Input
AN10 to AN15	: A/D Converter Input
BEEP	: Buzzer Output
BUSY	: Busy Output
EO0, EO1	: Error Out Output
FMIFC	: FM Intermediate Frequency Counter Input
GND	: Ground
GNDPLL	: PLL Ground
GNDPORT	: Port Ground
IC	: Internally Connected
INTP0 to INTP6	: Interrupt Inputs
P00 to P06	: Port 0
P10 to P15	: Port 1
P20 to P27	: Port 2
P30 to P37	: Port 3
P40 to P47	: Port 4
P50 to P57	: Port 5
P60 to P67	: Port 6
P120 to P125	: Port 12
P132 to P134	: Port 13
PWM0 to PWM2	: PWM Output
REGCPU	: Regulator for CPU Power Supply
REGOSC	: Regulator for Oscillator Circuit
$\overline{\text{RESET}}$	: Reset Input
SB0, SB1	: Serial Data Bus Input/Output
$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$	: Serial Clock Input/Output
SCL	: Serial Clock Input/Output
SDA0, SDA1	: Serial Data Input/Output
SI0, SI1	: Serial Data Input
SO0, SO1	: Serial Data Output
STB	: Strobe Output
TI1, TI2	: Timer Clock Input
VCOL, VCOH	: Local Oscillator Input
V_{DD}	: Power Supply
V_{DD}PLL	: PLL Power Supply
V_{DD}PORT	: Port Power Supply
X1, X2	: Crystal Oscillator Connection

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities depend on the version.

3. PIN FUNCTION LIST

3.1 PORT PINS

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0. 7-bit input/output port.	Input only	Input	INTP0
P01 to P06	I/O		Input/output mode can be specified bit-wise.	Input	INTP1 to INTP6
P10 to P15	I/O	Port 1. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	ANI0 to ANI5
P20	I/O	Port 2. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30 to P32	I/O	Port 3. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P33					TI1
P34					TI2
P35					—
P36					BEEP
P37					—
P40 to P47	I/O	Port 4. 8-bit input/output port. Input/output mode can be specified in 8-bit units. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50 to P57	I/O	Port 5. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P60 to P63	I/O	Port 6. 8-bit input/output port. Input/output mode can be specified bit-wise.	Middle voltage N-ch open drain input/output port. LEDs can be driven directly.	Input	—
P64 to P67					
P120 to P125	I/O	Port 12. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P132 to P134	Output	Port 13. 3-bit output port. N-ch open-drain output port.		—	PWM0 to PWM2

3.2 PINS OTHER THAN PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP6	Input	External maskable interrupt inputs with specifiable valid edges (rising edge, falling edge, both rising and falling edges).	Input	P00 to P06
SI0	Input	Serial interface serial data input	Input	P25/SB0/SDA0
SI1				P20
SO0	Output	Serial interface serial data output	Input	P26/SB1/SDA1
SO1				P21
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{\text{SCK0}}$	I/O	Serial interface serial clock input/output	Input	P27/SCL
$\overline{\text{SCK1}}$				P22
SCL				P27/$\overline{\text{SCK0}}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
TI1	Input	External count clock input to 8-bit timer (TM1)	Input	P33
TI2		External count clock input to 8-bit timer (TM2)		P34
BEEP	Output	Buzzer output	Input	P36
ANI0 to ANI5	Input	A/D converter analog input	Input	P10 to P15
PWM0 to PWM2	Output	PWM output	—	P132 to P134
EO0, EO1	Output	Error out output from charge pump of the PLL frequency synthesizer	—	—
VCOL	Input	Inputs PLL local band frequency (In HF, MF mode)	—	—
VCOH	Input	Inputs PLL local band frequency (In VHF mode)	—	—
AMIFC	Input	Inputs AM intermediate frequency counter	—	—
FMIFC	Input	Inputs FM intermediate frequency counter	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	System clock oscillation resonator connection	—	—
X2	—		—	—
REGOSC	—	Oscillation regulator. Connected to GND via a 0.1-μF capacitor.	—	—
REGCPU	—	CPU power supply regulator. Connected to GND via a 0.1-μF capacitor.	—	—
V_{DD}	—	Positive power supply	—	—
GND	—	Ground	—	—
V_{DD}PORT	—	Positive power supply for port block	—	—
GNDPORT	—	Ground for port block	—	—
V_{DD}PLL Note	—	Positive power supply for PLL	—	—
GNDPLL Note	—	Ground for PLL	—	—
IC	—	Internally connected. Connected to GND or GNDPORT.	—	—

Note Connect a capacitor of approximately 1 000 pF between the V_{DD}PLL pin and GNDPLL pin.

3.3 INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

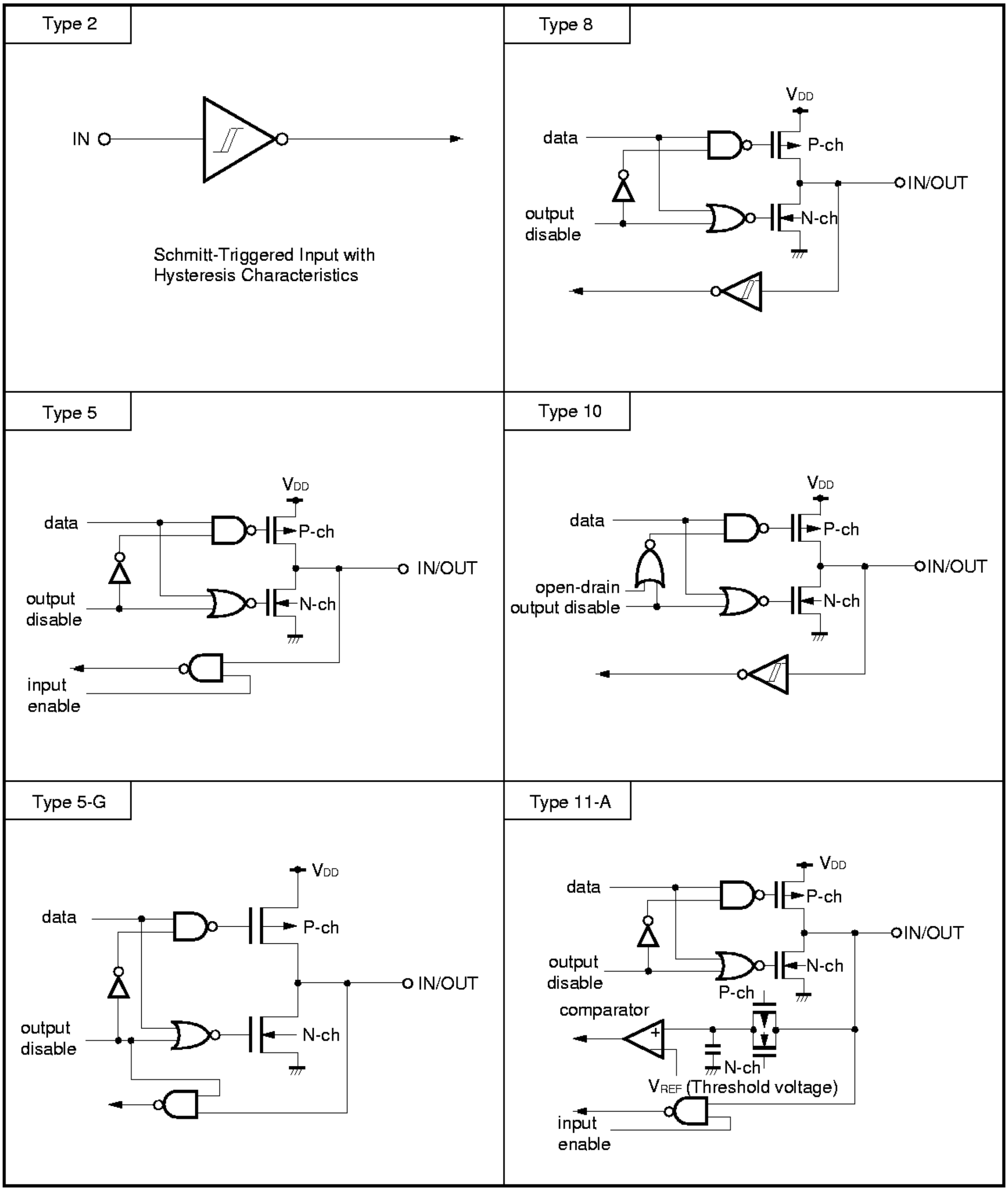
Table 3-1 shows the input/output circuit types of pins and the recommended conditions for unused pins.
Refer to Figure 3-1 for the configuration of the input/output circuit of each type.

Table 3-1. I/O Circuit Type of Each Circuit

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	2	Input	Connected to GND or GNDPORT
P01/INTP1 to P06/INTP6	8	I/O	Set in general-purpose input port mode by software and individually connected to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
P10/ANI0 to P15/ANI5	11-A		
P20/SI1	8		
P21/SO1	5		
P22/$\overline{\text{SCK1}}$	8		
P23/STB	5		
P24/BUSY	8		
P25/SI0/SB0/SDA0 P26/SO0/SB1/SDA1 P27/$\overline{\text{SCK0}}$/SCL	10		
P30 to P32	5		
P33/TI1, P34/TI2	8		
P35 P36/BEEP P37	5		
P40 to P47	5-G		
P50 to P57	5		
P60 to P63	13-D		
P64 to P67	5		
P120 to P125			
P132/PWM0 to P134/PWM2	19	Output	Set to low-level output by software and open
EO0	DTS-EO1		Open
EO1	DTS-EO3 Note		
VCOL, VCOH	DTS-AMP	Input	Set to disabled status by software and open
AMIFC, FMIFC			
IC	—	—	Connected to GND or GNDPORT directly

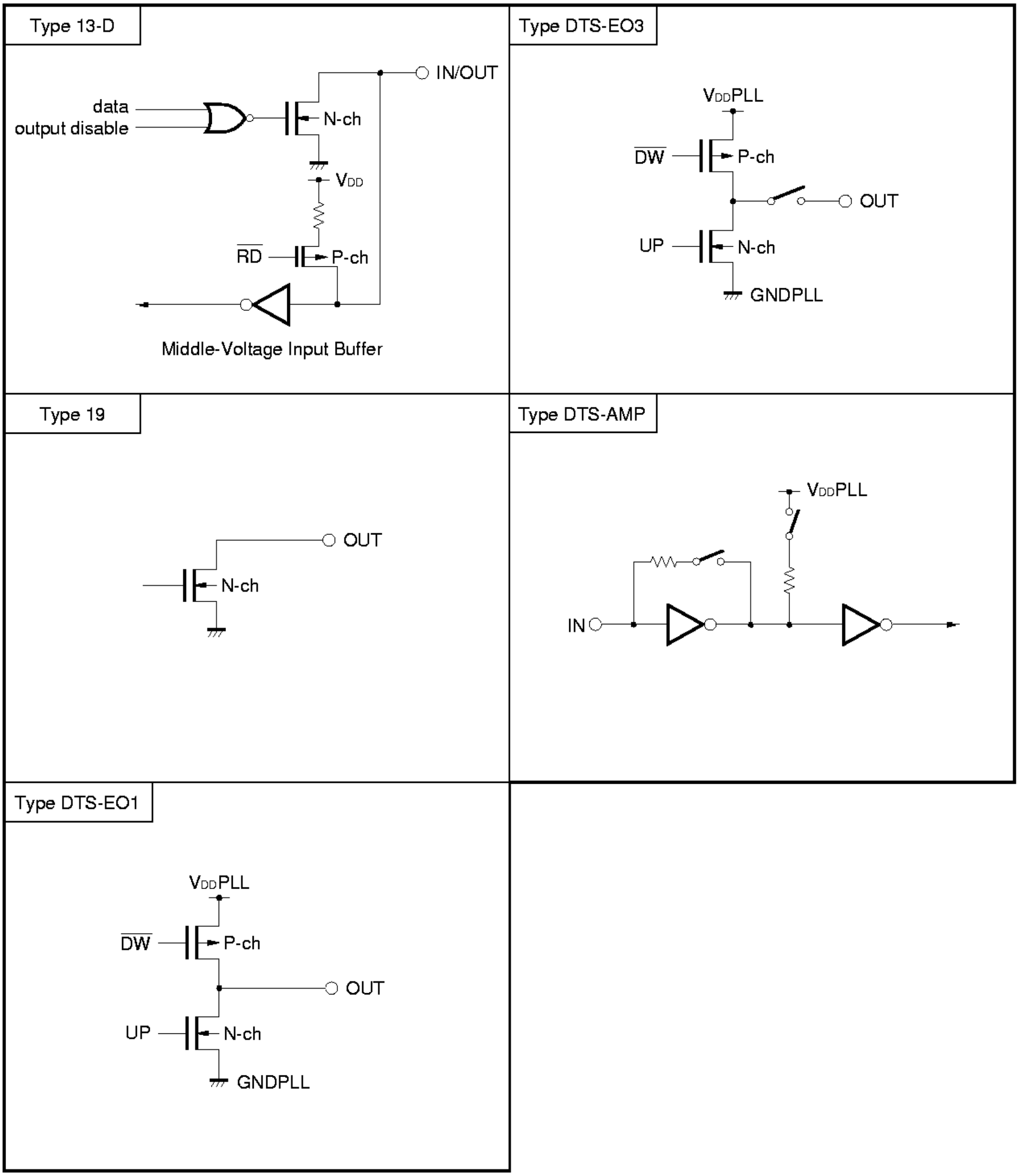
Note For the μPD178004A and 178006A, the I/O circuit type is DTS-EO1.

Figure 3-1. Pin Input/Output Circuit of List (1/2)



Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

Figure 3-1. Pin Input/Output Circuit of List (2/2)

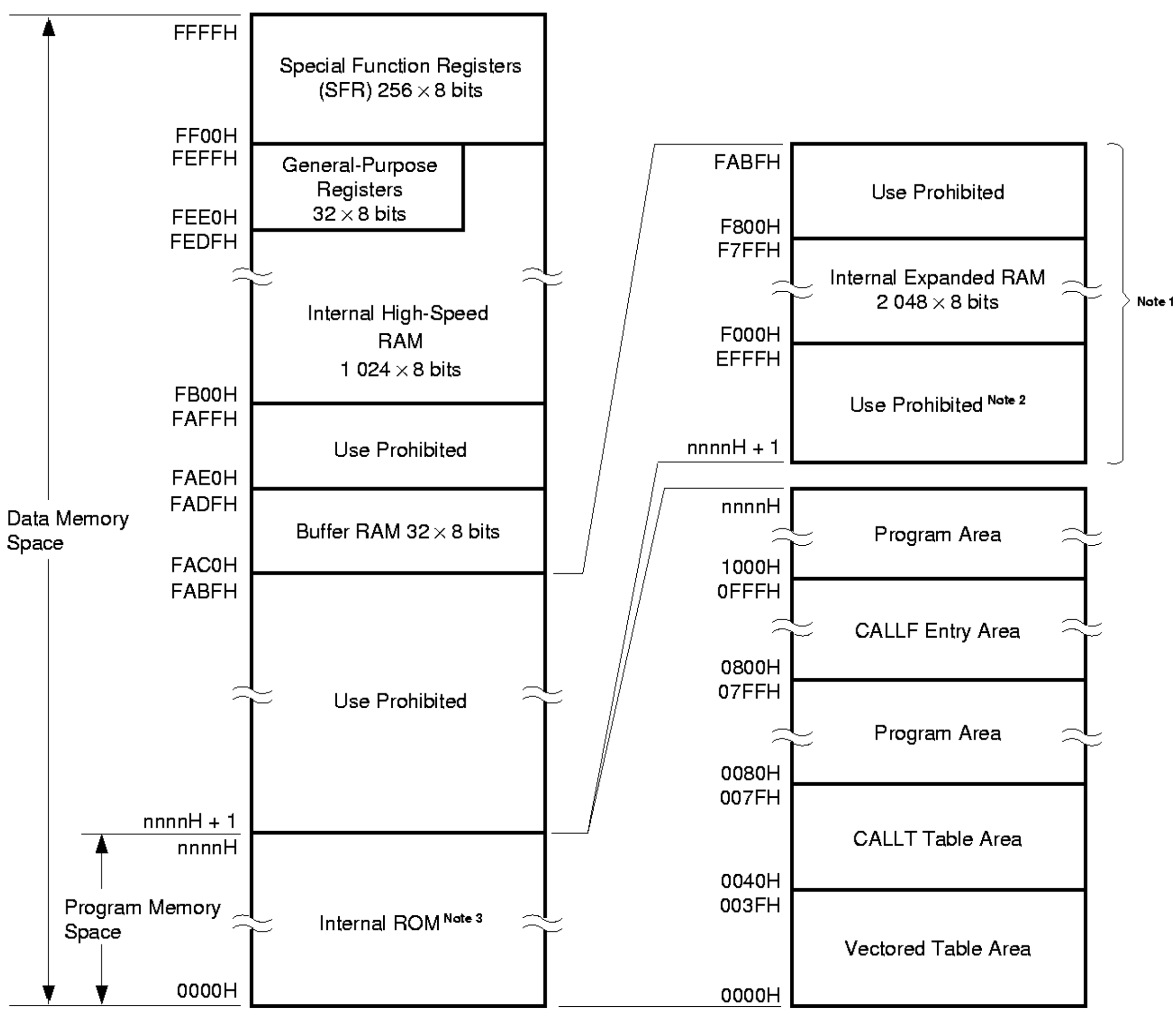


Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

4. MEMORY SPACE

Figure 4-1 shows the μPD178004A, 178006A, 178016A, and 178018A memory map.

Figure 4-1. Memory Map



Notes 1. Available only for μPD178016A and 178018A

2. The μPD178018A does not contain this use prohibited area.

3. The internal ROM capacity depends on the version (see the table below).

Corresponding Product Name	Internal ROM Last Address nnnnH
μPD178004A	7FFFH
μPD178006A, 178016A	BFFFH
μPD178018A	EFFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The following 3 types of I/O ports are available.

• CMOS input (P00)	: 1
• CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 12)	: 54
• N-channel open-drain input/output (P60 to P63)	: 4
• N-ch open drain output (Port 13)	: 3
Total	: 62

Table 5-1. Port Functions

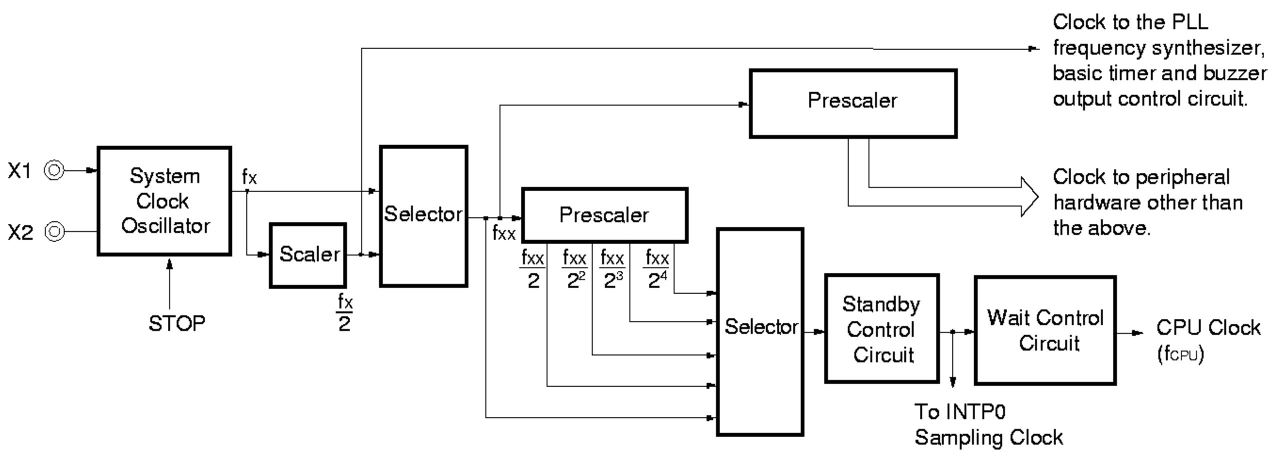
Name	Pin Name	Function
Port 0	P00	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise.
Port 1	P10 to P15	Input/output port pins. Input/output specifiable bit-wise.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. LED direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise.
Port 12	P120 to P125	Input/output port pins. Input/output specifiable bit-wise.
Port 13	P132 to P134	N-ch open drain output port.

5.2 CLOCK GENERATOR

The instruction execution time can be changed as follows.

0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (@ 4.5-MHz crystal oscillator with system clock.)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER

The μPD178004A, 178006A, 178016A, and 178018A incorporate 5 channels of the timer.

- Basic timer : 1 channel
- 8-bit timer/event counter : 2 channels
- 8-bit timer (D/A converter) Note : 1 channel
- Watchdog timer : 1 channel

Note Used is shared with the 8/9-bit resolution × 3-channel D/A converter (PWM output).

Figure 5-2. Basic Timer Block Diagram

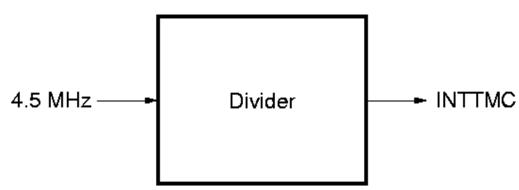


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

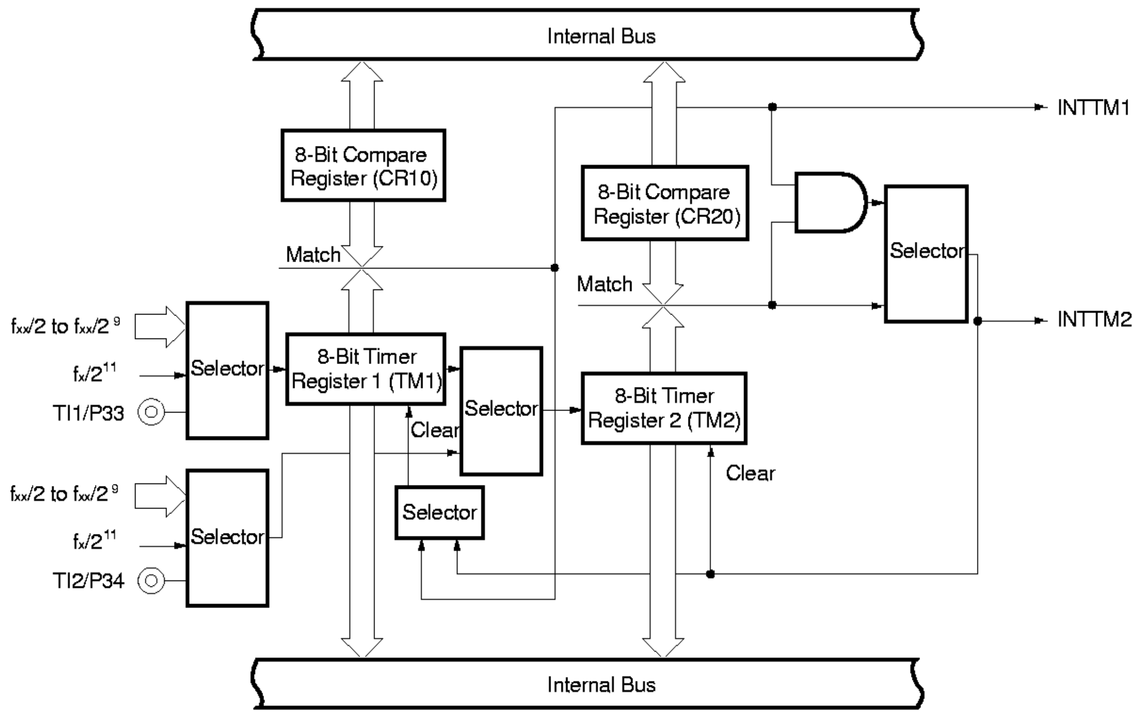
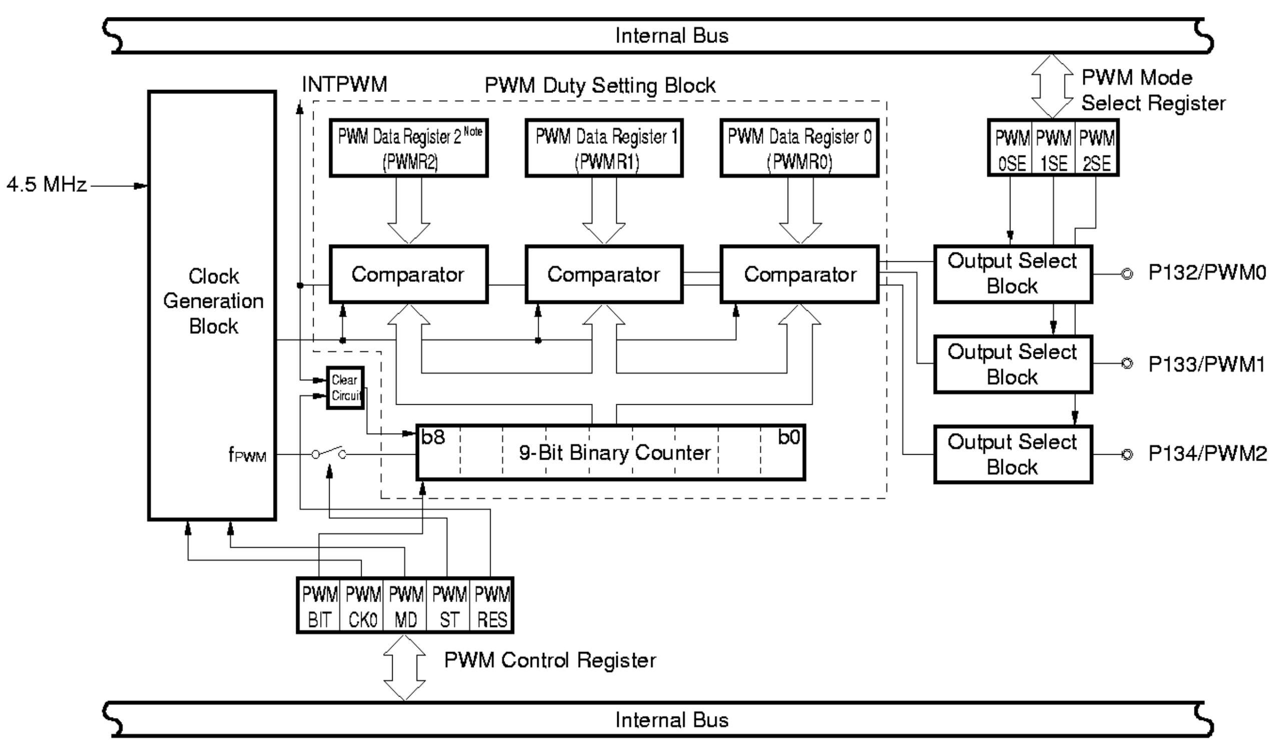
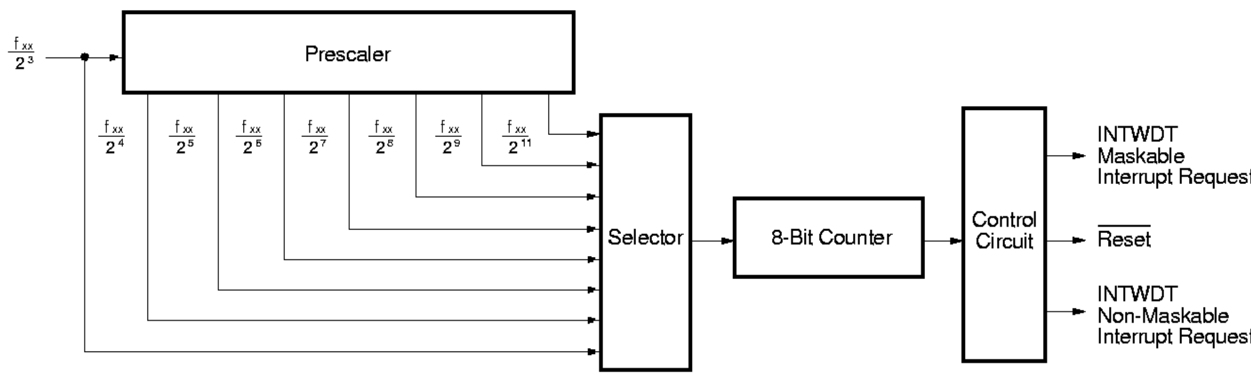


Figure 5-4. 8-Bit Timer (D/A Converter) Block Diagram



Note The PWM data register 2 (PWMR2) is multiplexed with the PWM timer register (PWMTMR).

Figure 5-5. Watchdog Timer Block Diagram

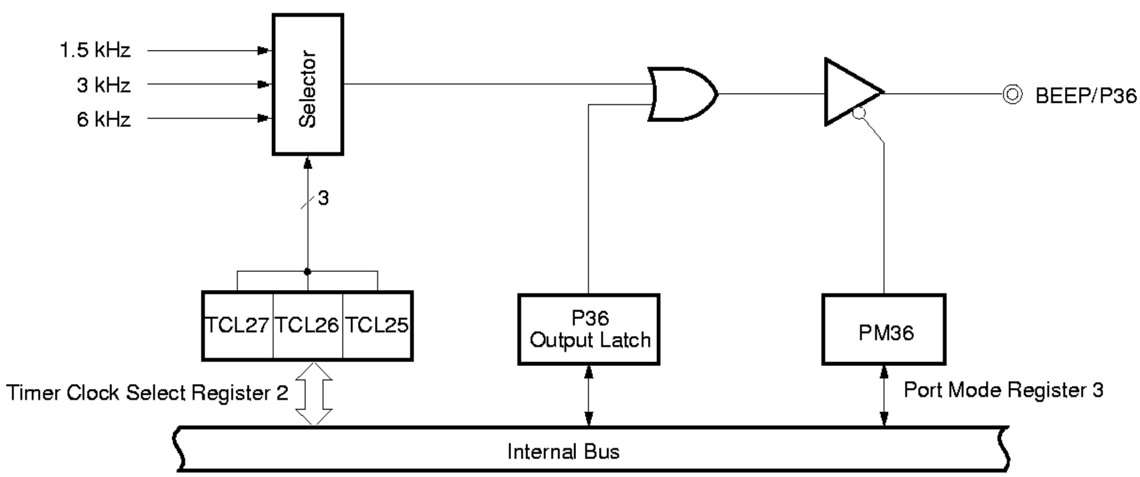


5.4 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a buzzer output.

- 1.5 kHz/3 kHz/6 kHz (@ 4.5-MHz crystal oscillator with system clock)

Figure 5-6. Buzzer Output Control Circuit Block Diagram



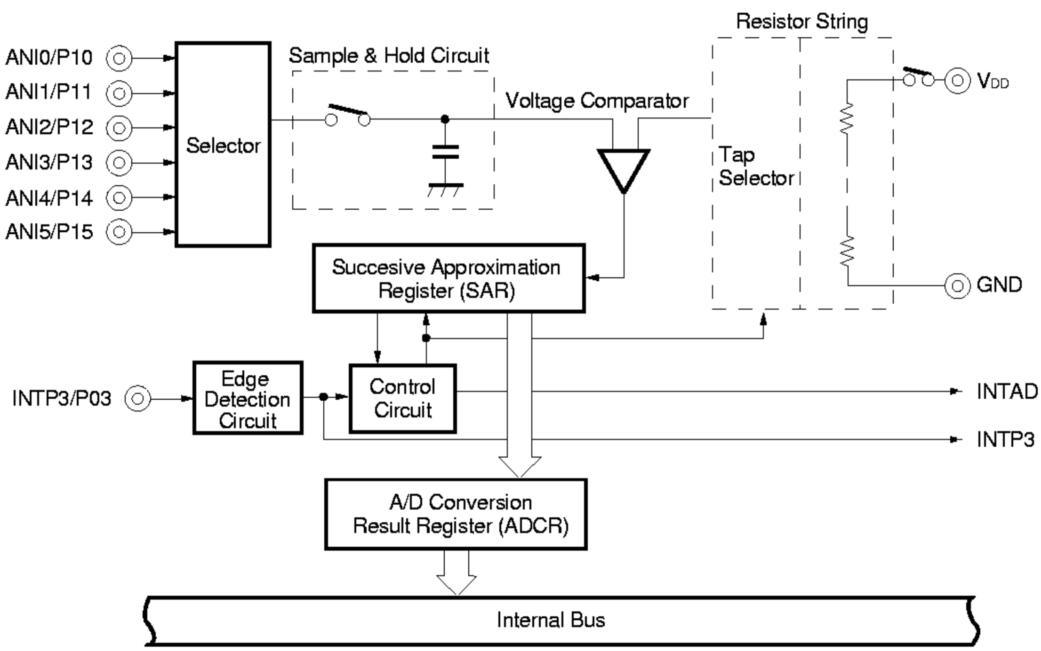
5.5 A/D CONVERTER

An A/D converter of 8-bit resolution × 6 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-7. A/D Converter Block Diagram



5.6 SERIAL INTERFACES

2 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1

Table 5-2. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	O (MSB/LSB first switchable)	O (MSB/LSB first switchable)
3-wire serial I/O mode with automatic transmission/ reception function	—	O (MSB/LSB first switchable)
SBI (serial bus interface) mode	O (MSB first)	—
2-wire serial I/O mode	O (MSB first)	—
I²C Bus Mode	O (MSB first)	—

Figure 5-8. Serial Interface Channel 0 Block Diagram

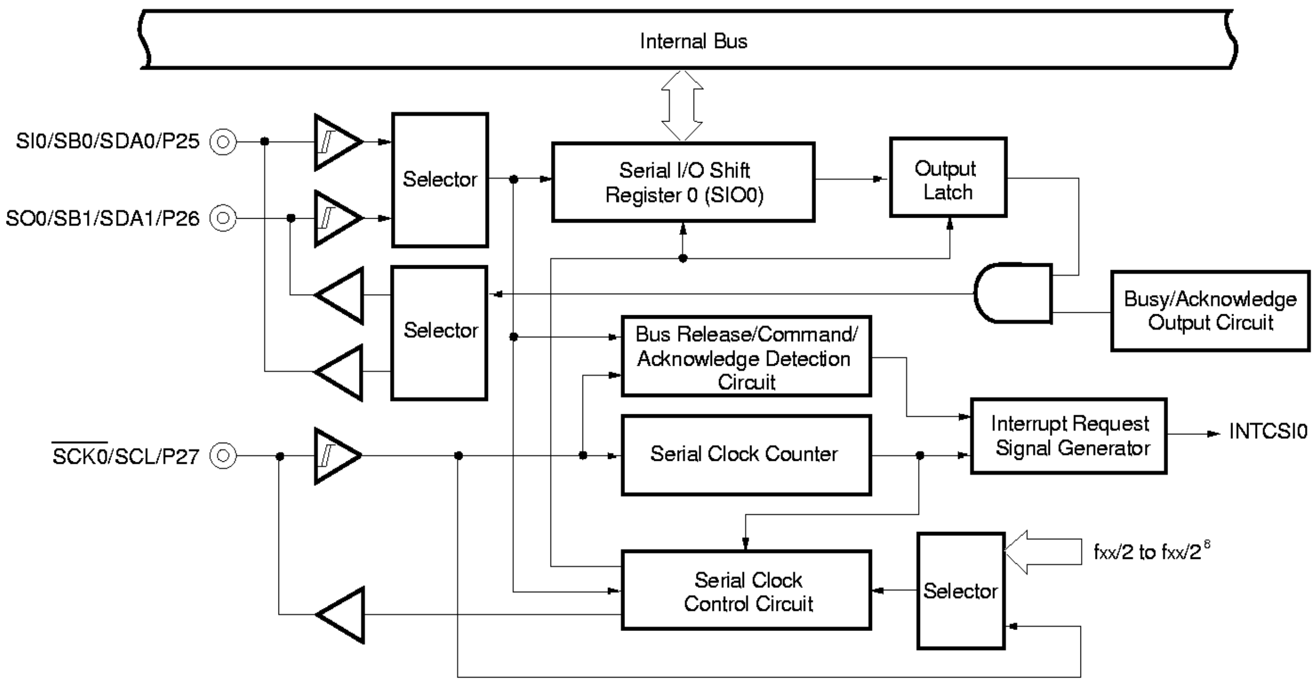
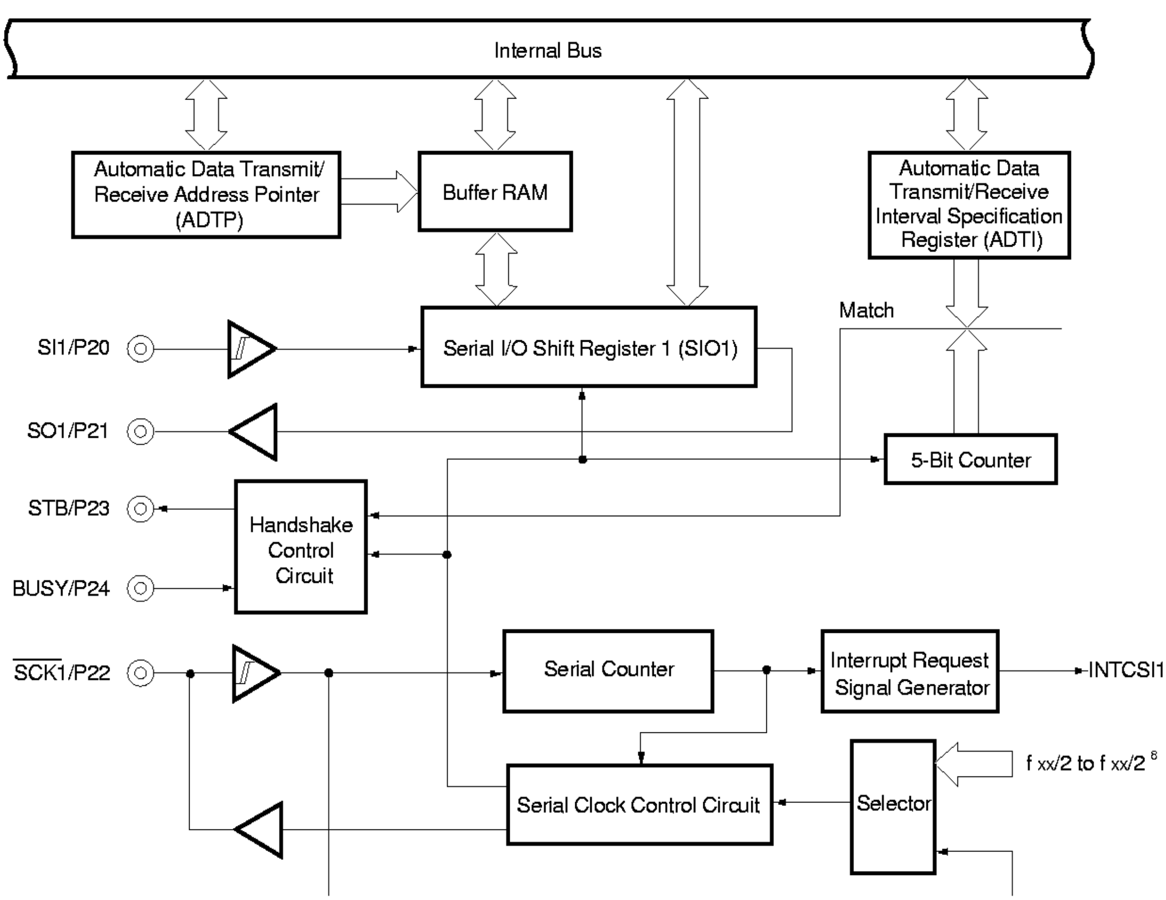
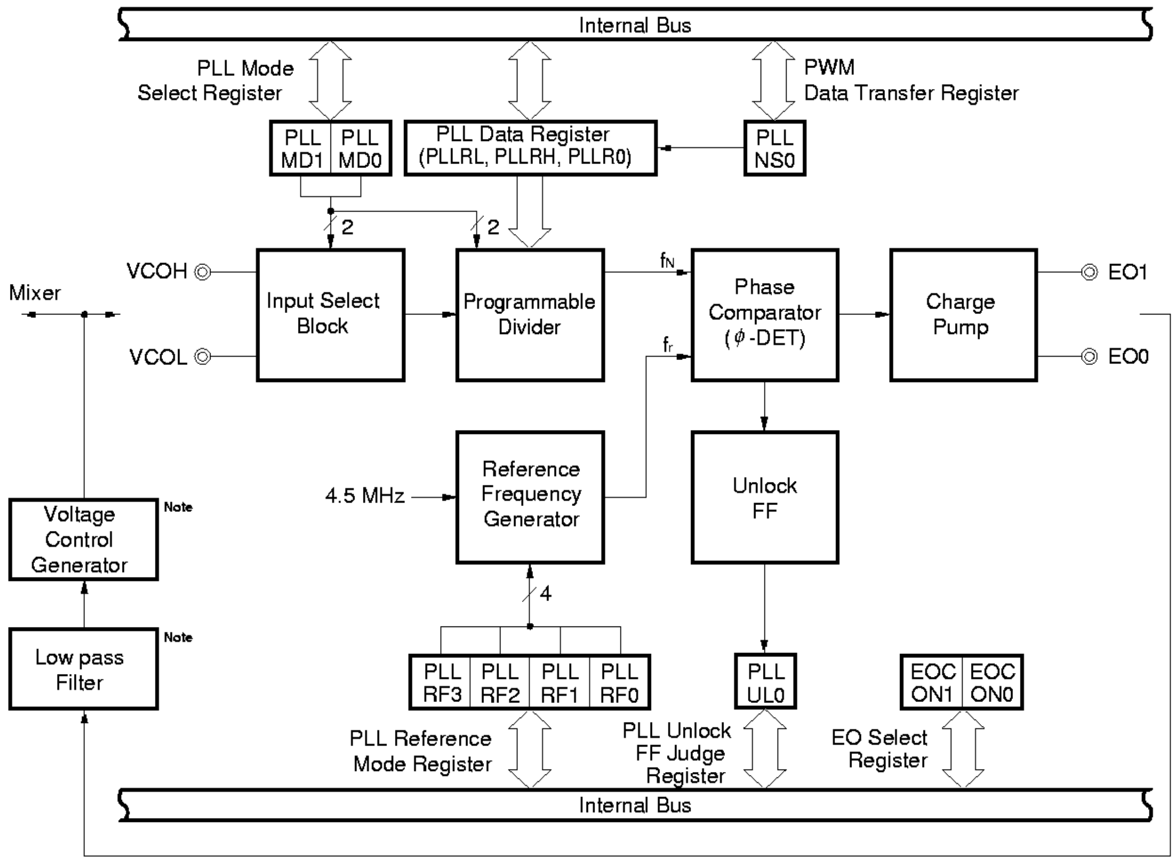


Figure 5-9. Serial Interface Channel 1 Block Diagram



5.7 PLL FREQUENCY SYNTHESIZER

Figure 5-10. PLL Frequency Synthesizer Block Diagram



Note External circuit

Cautions 1. Be sure to set EOCON0 to 0.

2. For the μPD178004A and 178006A, do not set EOCON1 to 1.

5.8 FREQUENCY COUNTER

Figure 5-11. Frequency Counter Block Diagram