

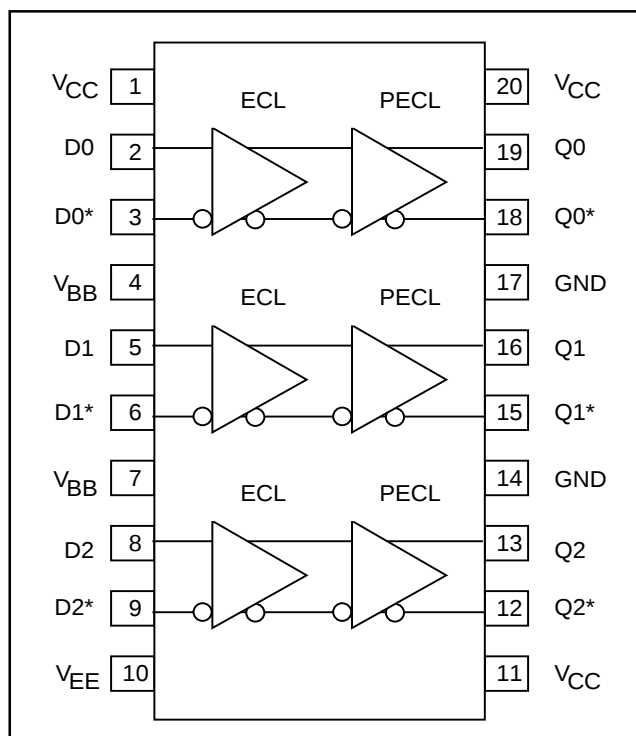
Description

The SK10/100EL90W is a triple ECL to PECL/LVPECL and LVECL to PECL/LVPECL translator. It is fully compatible with MC100EL90 and MC100LVEL90. The SK10/100EL90W provides a V_{BB} output for single-ended use or DC bias for AC coupling to the device. V_{BB} is an output pin and should be used as a bias for the EL90W as its current source/sink capability is limited. Whenever used, the V_{BB} output pin should be bypassed to V_{CC} via a 0.01 μ F capacitor.

To accomplish levels of translation, the EL90W requires three power rails, V_{CC} , V_{EE} and GND. Please refer to the Function Table below for more details. V_{CC} supply should be connected to the positive supply, and V_{EE} should be connected to the negative supply.

The GND pins are connected to the system ground plane. Both V_{CC} and V_{EE} pins should be bypassed to ground via a 0.01 μ F capacitor. Under open input conditions, the D* input will be biased at $V_{EE}/2$, and the D input will be pulled to V_{EE} . This condition will force the Q output to low, ensuring stability.

Functional Block Diagram



Features

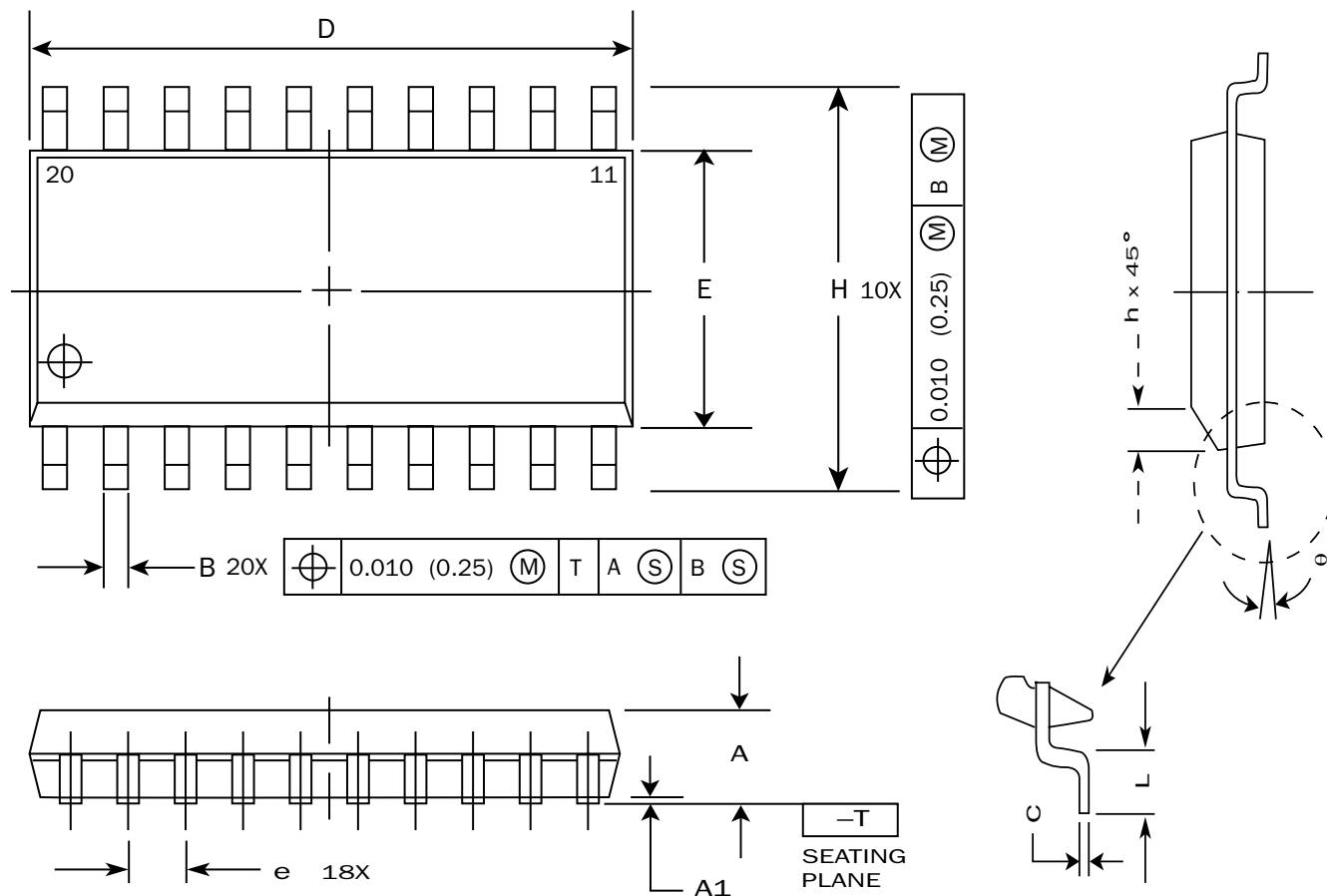
- Extended Supply Voltage Range ($V_{EE} = -5.5V$ to $-3.0V$ and $V_{CC} = 3.0V$ to $5.5V$)
- High Bandwidth Output Transition
- 500 ps Propagation Delay
- V_{BB} Output
- Internal Input Pulldown Resistors
- New Differential Input Common Mode Range
- Fully Compatible with MC100EL90 and MC100LVEL90
- ESD Protection of $>4000V$
- Industrial Temperature Range: $-40^{\circ}C$ to $+85^{\circ}C$
- Available in 20-lead SOIC Package

Pin Names

Pin	Function
Dn, Dn*	Differential ECL/LVECL Inputs
Qn, Qn*	Differential PECL/LVPECL Outputs
V_{BB}	ECL/LVECL Reference Voltage Output

Function	V_{EE}	V_{CC}
LVECL-to-PECL	-3.3V	+5.0V
LVECL-to-LVPECL	-3.3V	+3.3V
ECL-to-PECL	-5.0V	+5.0V
ECL-to-LVPECL	-5.0V	+3.3V

Function Table

Package Information
20 Pin SOIC Package


DIM	Millimeters	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

NOTES:

1. Dimensions and tolerances per ASME Y14.5M, 1994.
2. Controlling dimension: millimeters.
3. Dimensions D and E do not include mold protrusion.
4. Maximum mold protrusion 0.15 per side.
5. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 total in excess of B dimension at maximum material condition.

DC Characteristics

SK10/100EL90W ECL/LVECL Input DC Electrical Characteristics (Notes 1, 2, 6)

($V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = +3.0V$ to $+5.5V$; V_{OUT} loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = -40°C		TA = 0°C		TA = +25°C		TA = +85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	Input HIGH Voltage	-1230	-890	-1170	-840	-1130	-810	-1060	-720	mV
	10 EL 100 EL	-1165	-880	-1165	-880	-1165	-880	-1165	-880	mV
V _{IL}	Input LOW Voltage	-1950	-1500	-1950	-1480	-1950	-1480	-1950	-1445	mV
	10 EL 100 EL	-1810	-1475	-1810	-1475	-1810	-1475	-1810	-1475	mV
V _{BB}	Input Reference Voltage	-1430	-1300	-1380	-1270	-1350	-1250	-1310	-1190	mV
	10 EL 100 EL	-1380	-1260	-1380	-1260	-1380	-1260	-1380	-1260	mV
I _{IN}	Input Current (Diff)	-150	150	-150	150	-150	150	-150	150	μA
I _{EE}	Power Supply Current	2	6	2	6	2	6	2	6	mA

SK10/100EL90W PECL/LVPECL Output DC Electrical Characteristics (Notes 1, 2)

($V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = +3.0V$ to $+5.5V$; V_{OUT} loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit	Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
V _{OH}	Output HIGH Voltage	3.92	4.11	3.98	4.16	4.02	4.19	4.09	4.28	V	V _{CC} = 5V
	10 EL	2.22	2.41	2.28	2.46	2.32	2.49	2.39	2.58	V	V _{CC} = 3.3V
V _{OH}	Output HIGH Voltage	3.915	4.12	3.975	4.12	3.975	4.12	3.975	4.12	V	V _{CC} = 5V
	100 EL	2.215	2.42	2.275	2.42	2.275	2.42	2.275	2.42	V	V _{CC} = 3.3V
V _{OL}	Output LOW Voltage	3.05	3.35	3.05	3.37	3.05	3.37	3.05	3.405	V	V _{CC} = 5V
	10 EL	1.35	1.65	1.35	1.67	1.35	1.67	1.35	1.705	V	V _{CC} = 3.3V
V _{OL}	Output LOW Voltage	3.17	3.445	3.19	3.38	3.19	3.38	3.19	3.38	V	V _{CC} = 5V
	100 EL	1.47	1.745	1.49	1.68	1.49	1.68	1.49	1.68	V	V _{CC} = 3.3V
I _{GND}	Power Supply Current	17	32	17	32	17	32	17	32	mA	
	10 EL 100 EL	17	35	17	35	17	35	17	35	mA	

AC Characteristics
SK10/100EL90W AC Electrical Characteristics

($V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = +3.0V$ to $+5.5V$; V_{OUT} loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = -40 °C		TA = 0 °C		TA = +25 °C		TA = +85 °C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{skew}	Output to Output Skew		100		100		100		100	ps
t _{PHL} t _{PLH}	Propagation Delay (Diff) ³	420	530	435	550	440	560	460	585	ps
t _{PLH} t _{PH}	Propagation Delay (SE) ³	435	545	450	565	460	580	470	605	ps
t _r , t _f	Output Rise/Fall Times (20% to 80%)	275	470	275	470	275	470	275	470	ps
V _{CMR}	Common Mode Range ⁵	VEE + 1.2	GND	VEE + 1.2	GND	VEE + 1.2	GND	VEE + 1.2	GND	V
V _{PP}	Minimum Input Swing ⁴	150	1000	150	1000	150	1000	150	1000	mV

Notes:

- 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to $V_{CC}-2.0V$.
- 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
- Duty cycle skew is the difference between T_{PLH} and T_{PHL} propagation delay through a device.
- Minimum input swing for which parameters guaranteed.
- CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $V_{PP(min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to $VEE + 1.2V$.
- For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
- For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID
SK10EL90WD	20-SOIC
SK10EL90WDT	20-SOIC
SK100EL90WD	20-SOIC
SK100EL90WDT	20-SOIC
SK10EL90WU	Die
SK100EL90WU	Die

Application Notes

AN1002 - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTTL / CMOS / LVCMOS

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

AN1005 - Using ECL / LVECL Devices as PECL / LVPECL

AN1006 - Designing with 10K and 100K ECL / PECL Devices

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