DESCRIPTION

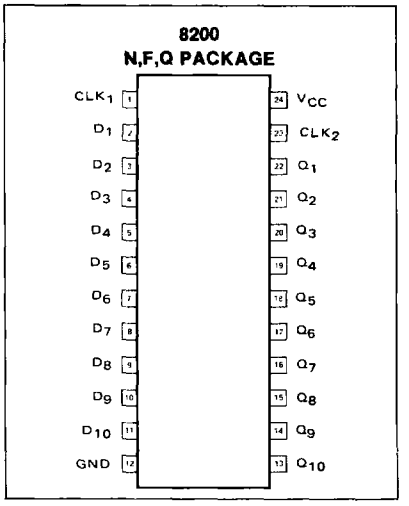
The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel-in parallel-out register applications. They are also suitable for general purpose applications as parallel-in serial-out, serial-in parallel-out registers.

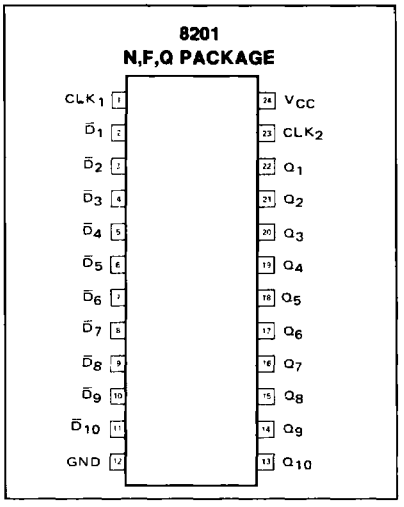
The flip-flops are arranged as dual 5 arrays, (8200 & 8201) and single 10 arrays with reset, (8202 & 8203). The true output of each bit is made available to the user.

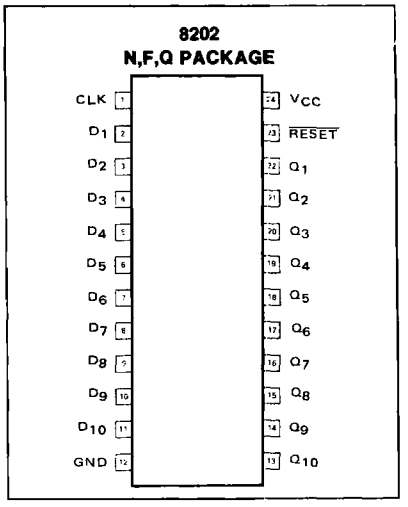
The 8200 and 8202 feature true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock.

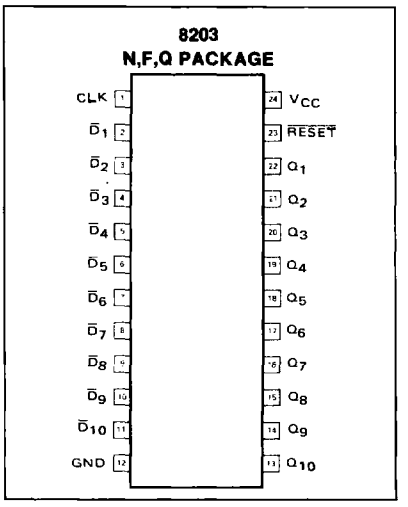
The 8201 and 8203 feature complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative going transition of the clock. This complementing input feature ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

PIN CONFIGURATION









LOGIC

TRUTH TABLE

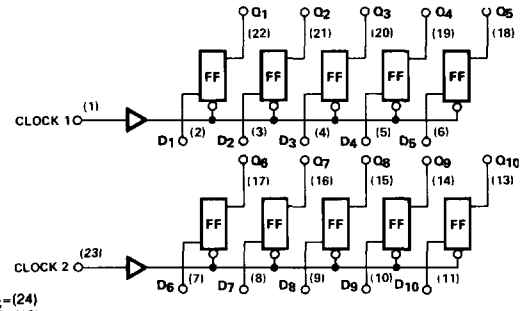
	D_n	$\overline{D}_n$	$\overline{RESET}$	Q_{n+1}
8200	1	—	—	1
	0	—	—	0
8201	—	1	—	0
	—	0	—	1
8202	1	—	1	1
	0	—	1	0
8203	0	—	1	1
	1	—	1	0

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

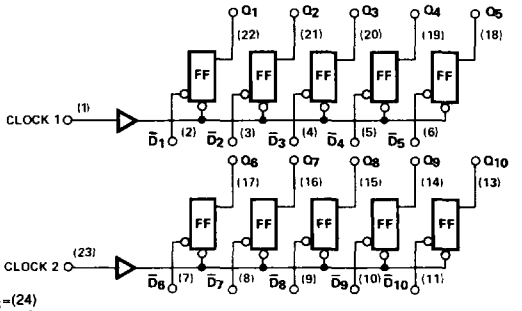
PARAMETER	FROM INPUT	TO OUTPUT	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Propagation delay time						
t_{on} turn-on time	Clock	Q		30	45	ns
	Reset	Q		30	45	
t_{off} turn-off time	Clock	Q		25	40	
t_{setup} setup time				6	15	ns
t_{hold} hold time[2]				0	5	ns
t_w input pulse width min, clock				12	17	ns
Transfer rate			15	35		MHz

LOGIC DIAGRAMS

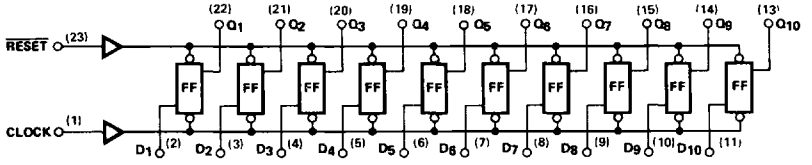
8200 DUAL 5-BIT BUFFER REGISTER



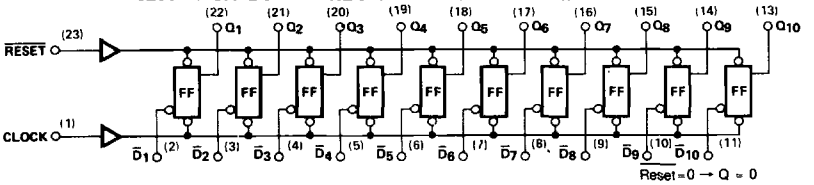
8201 DUAL 5-BIT BUFFER REGISTER-INVERTED INPUTS



8202 10-BIT BUFFER REGISTER

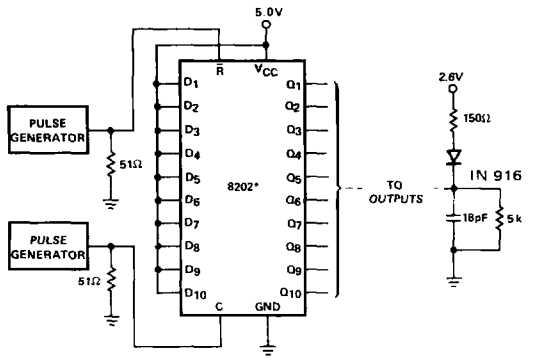


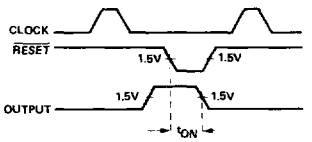
8203 10-BIT BUFFER REGISTER — INVERTED INPUTS



AC TEST FIGURES AND WAVEFORMS

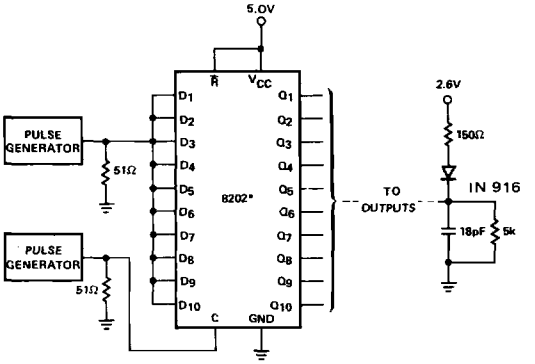
t_{on} FROM RESET TO Q

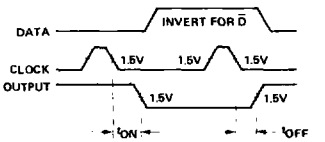




Input pulse:
Amplitude =2.6V
Clock: P.R.R. = 5 MHz
Reset: P.R.R. = 5 MHz
PW = 30 ns (at 50% point)
$t_r = t_f = 5$ ns

t_{pd} FROM CLOCK TO Q

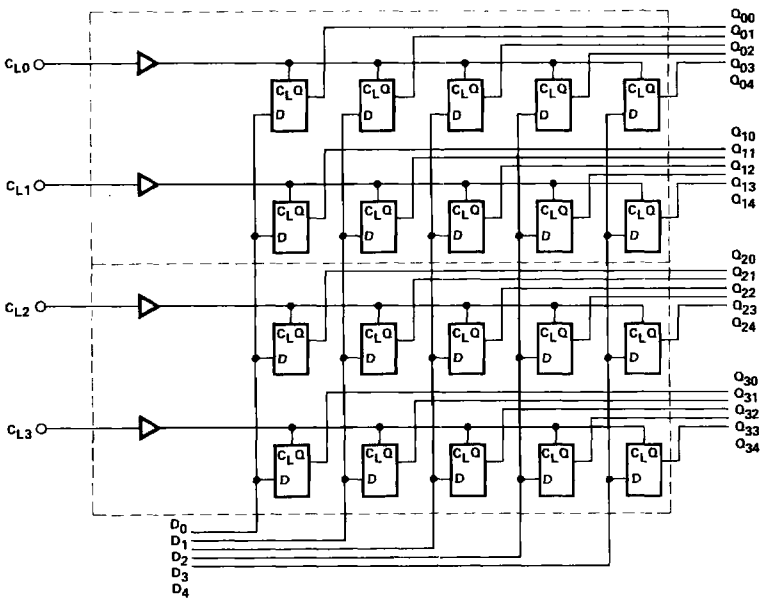




Input pulse:
Data = P.R.R. =7.5 MHz
Clock = P.R.R. = 15 MHz
PW = 17 ns (at 50% point)
$t_r = t_f = 5$ ns Max
Amplitude=2.6V

TYPICAL APPLICATIONS

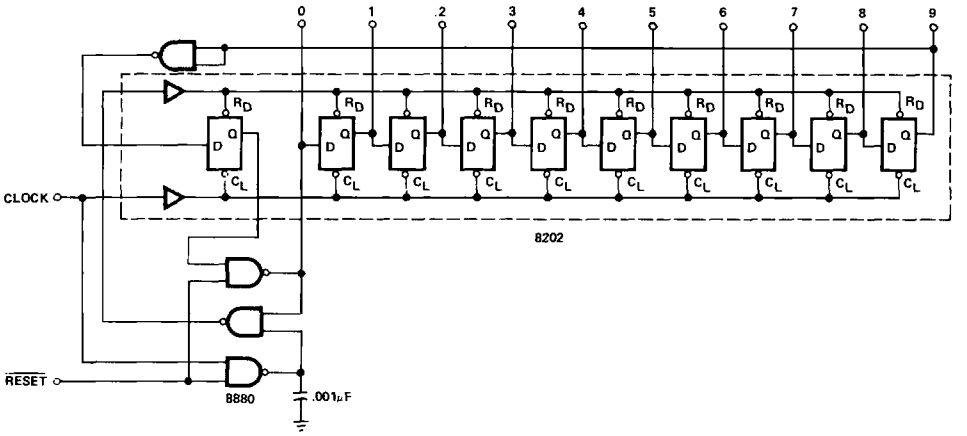
20-BIT (4 WORDS X 5 BITS EACH) MEMORY CELL



LOGIC

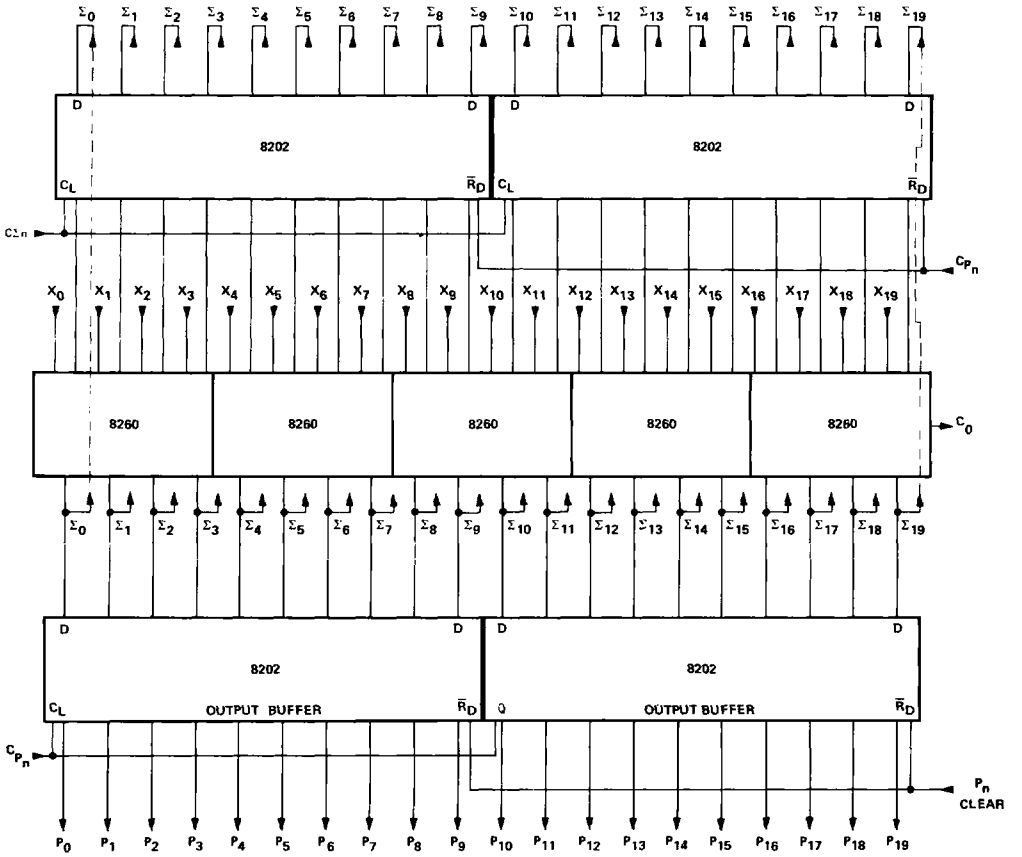
TYPICAL APPLICATIONS (Cont'd)

ONE OUT OF TEN - COUNTER/DISPLAY (SELF-CORRECTING)



TYPICAL APPLICATIONS

MULTIPLICATION AT 10 MHz OF A 20-BIT BINARY WORD



$P_n = (X_n)M$ where $X_n \equiv$ multiplicand
$M \equiv$ multiplier