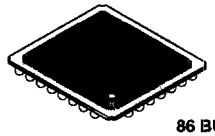
MCM67Q709A

128K x 9 Bit Separate I/O Synchronous Fast Static RAM



86 BUMP PBGA
CASE 896A–02

The Motorola MCM67Q709A is a 1,179,648 bit static random access memory, organized as 131,072 words of 9 bits. It features separate TTL input and output buffers, which drive 3.3 V output levels and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The addresses (A0 – A16), data input (D0 – D8), data output (Q0 – Q8), write enable ($\overline{W}$), chip enable ($\overline{E}$), and output enable ($\overline{G}$), are registered in on the rising edge of clock (K).

The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0 – Q8) will be driven if $\overline{G}$ is registered low. The transparent write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a transparent write (write and pass–through). The input data is available at the ouputs on the next rising edge of clock (K).

The pass–through function is always enabled. $\overline{E}$ high disables the write to the array while allowing a pass through cycle to occur on the next rising edge of clock (K). Only a registered $\overline{G}$ high will three–state the outputs.

The MCM67Q709A is available in an 86 bump surface mount PBGA (Plastic Ball Grid Array) package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (Outputs LVTTL Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$ Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time
- Boundary Scan Implementation
- PBGA Package for High Speed Operation

PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D8	Data Inputs
Q0 – Q8	Data Outputs
K	Clock Input
SCK	Scan Clock Input
SE	Scan Enable
SDI	Scan Data Input
SDO	Scan Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9
A		$\overline{E}$	$\overline{W}$	V_{CC}	SDI	SDO	A4	A0	
B	A16	A14	$\overline{G}$	K	V_{SS}	A6	A2	V_{SS}	D8
C	D7	A15	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q8	V_{SS}
D	V_{SS}	Q7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q6	D6
E	D5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}
F	V_{CC}	Q5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D4	Q4
G	D3	Q3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D2	Q2
H	V_{SS}	D1	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D0	V_{SS}
J	Q1	A12	A10	V_{SS}	A9	A8	A5	A1	Q0
K		A13	A11	SCK	V_{CC}	SE	A7	A3	

TOP VIEW 86 BUMP Not to Scale

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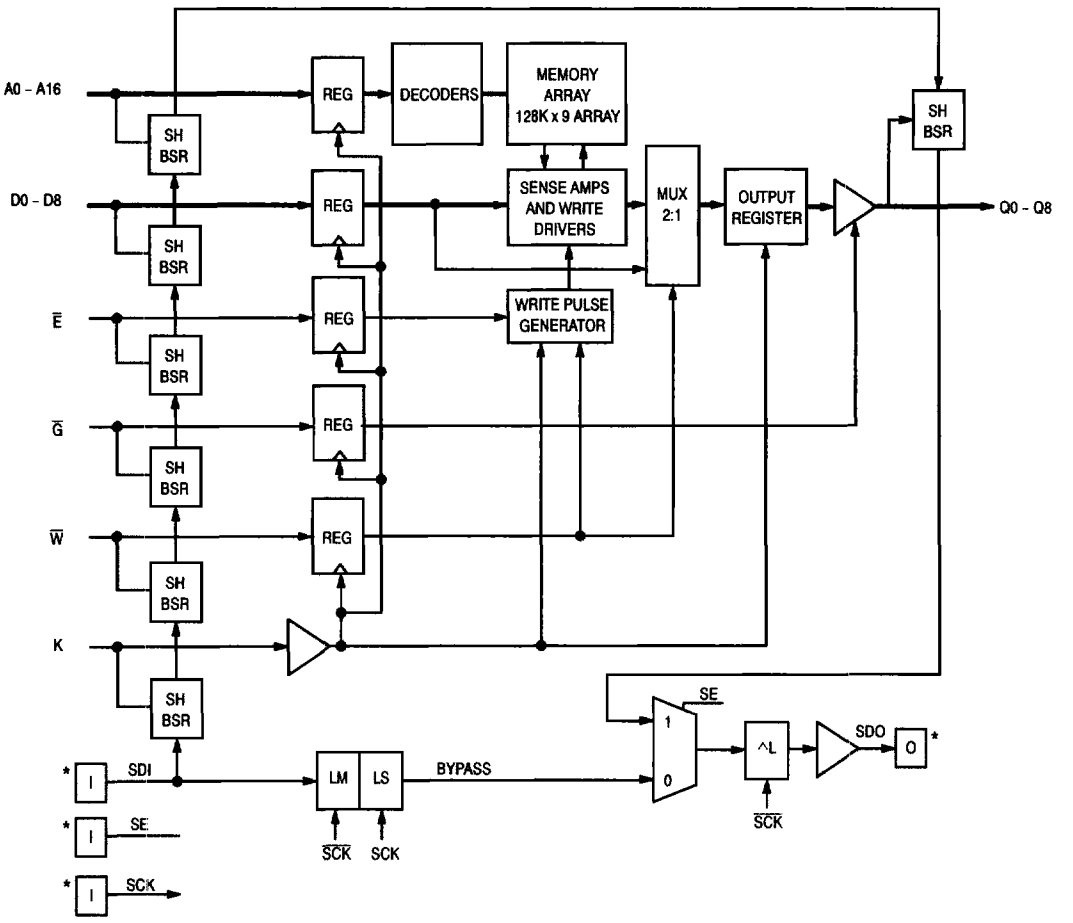
BLOCK DIAGRAM



NOTES:

1. Bypass mode is entered with SE low and SCK cycled.
2. SH BSR = Shadow Bypass Scan Register.
3. 39 bumps used in Boundary Scan. V_{SS}, V_{CC}, NC, SDI, SDO, SE, and SCK not used in Scan Path.
4. SDO Output Sequence A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, K.

* Four added test pins.

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ (t_{n+1})	Mode	D0 – D8 (t_n)	Q0 – Q8 (t_{n+1})	V_{CC} Current
L	L	L	Write and Pass Through	Valid	D0 – D8 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass Through	Valid	D0 – D8 (t_n)	I_{CC}
		H	Pass Through	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	*MCM67Q709A–10 ns*	I_{CCA}	—	230	mA
	MCM67Q709A–12 ns		—	220	
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

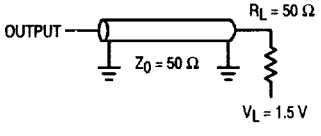
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1a Unless Otherwise Noted

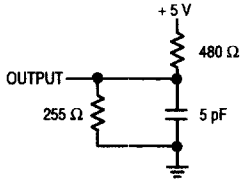
READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67Q709A–10		MCM67Q709A–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	3
Setup Times: A	t_{AVKH}	2	—	2	—	ns	4
$\overline{W}$	t_{WVKH}						
$\overline{E}$	t_{EVKH}						
$\overline{G}$	t_{GVKH}						
D0 – D8	t_{DVKH}						
Hold Times: A	t_{KHAX}	1	—	1	—	ns	4
$\overline{W}$	t_{KHWX}						
$\overline{E}$	t_{KHEX}						
$\overline{G}$	t_{KHGX}						
D0 – D8	t_{KHDX}						

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. Measured at ± 200 mV from steady state. Tested per High–Z Test Load (See Figure 1b).
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.



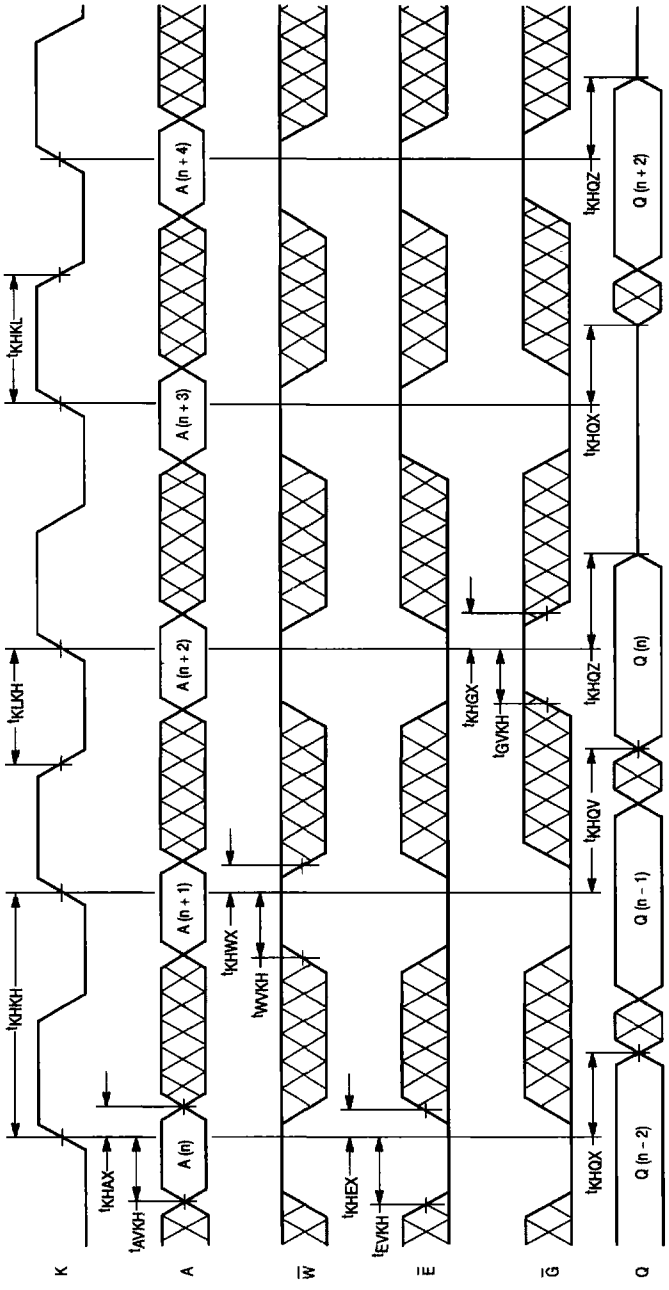
(a)



(b)

Figure 1. Test Loads

READ CYCLE TIMING



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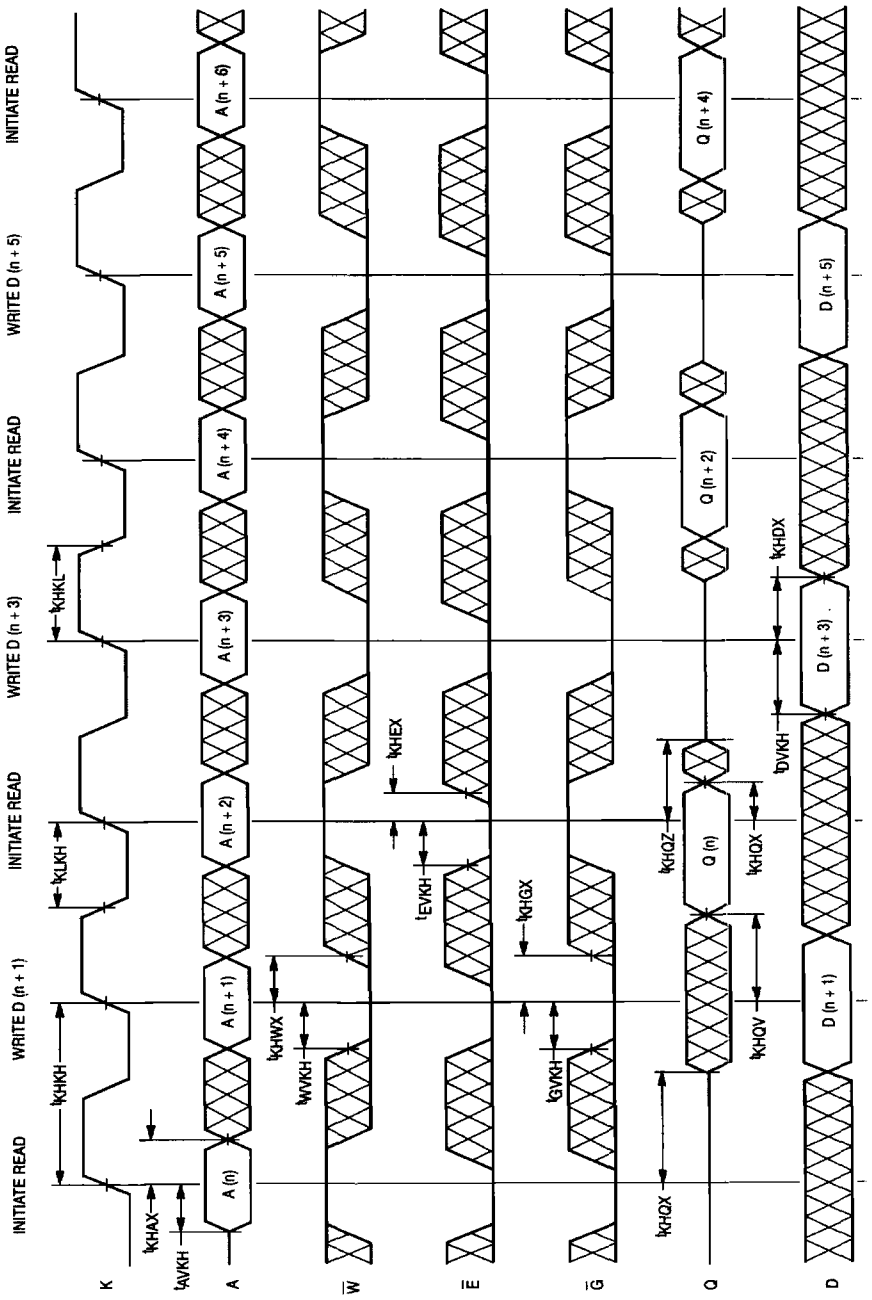
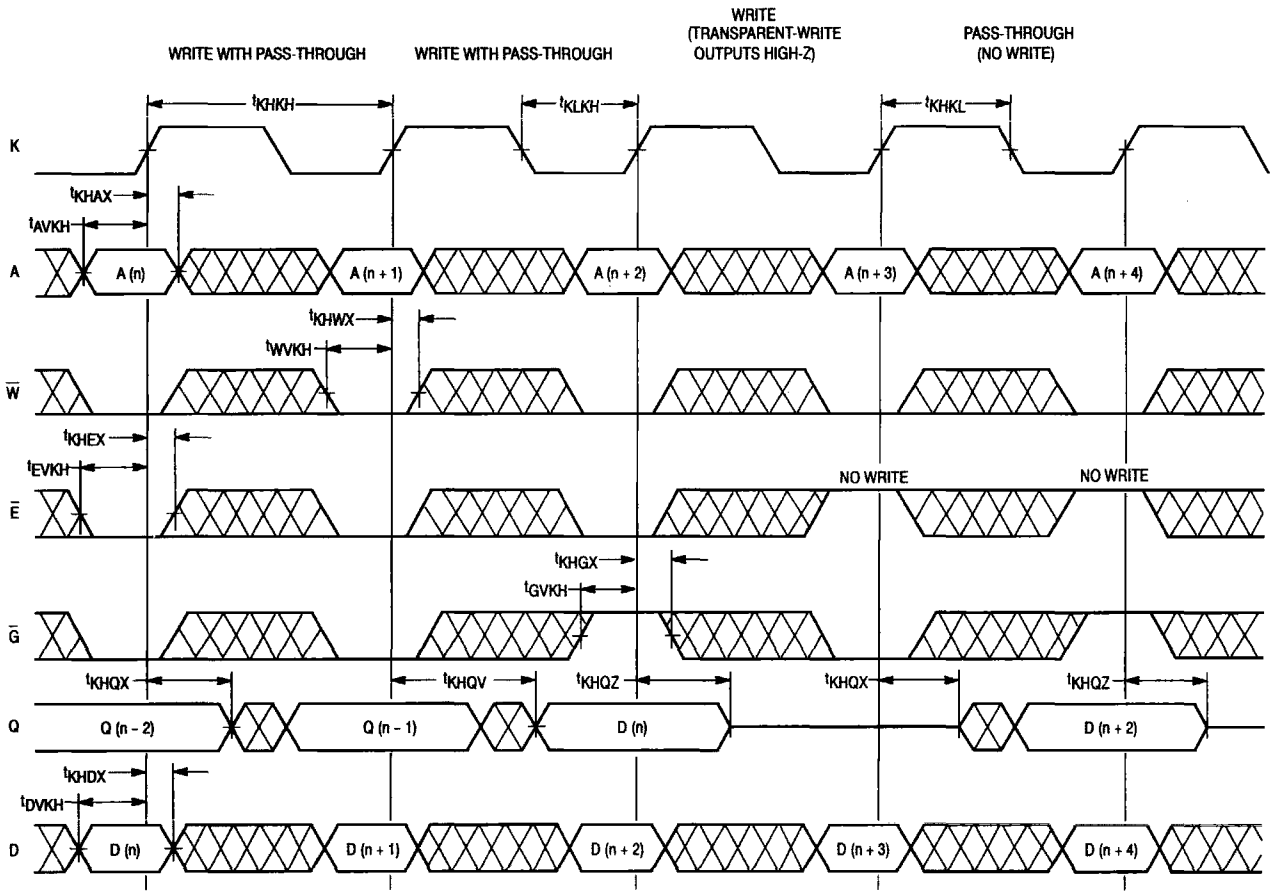
COMBINATION READ/WRITE CYCLE TIMING



TRANSPARENT-WRITE AND PASS-THROUGH CYCLE TIMING



BOUNDARY SCAN CYCLE TIMING

Parameter	Symbol	MCM67Q709A–10		MCM67Q709A–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CHCH2}	100	—	100	—	ns	
Clock High Pulse Width	t_{CHCL2}	40	—	40	—	ns	
Clock Low Pulse Width	t_{CLCH2}	40	—	40	—	ns	
Scan Mode Setup Time	t_{SS}	10	—	10	—	ns	1
Bypass Mode Setup Time	t_{BS}	10	—	10	—	ns	2
Scan Mode Recovery Time	t_{SR}	100	—	100	—	ns	3
SCK Low to SE Hold High	t_{CLMH}	10	—	10	—	ns	4
SE High to SCK High Setup	t_{MHCH}	10	—	10	—	ns	5
SCK High to SE Low Hold Time	t_{CHML}	10	—	10	—	ns	6
SDI Valid to SCK High Setup	t_{IVCH}	10	—	10	—	ns	
SCK High to SDI Don't Care	t_{CHIX}	10	—	10	—	ns	
SCK Low to SDO Valid	t_{CLOV}	—	20	—	20	ns	

NOTES:
1. The minimum delay required between ending normal operation and beginning scan operations.
2. The minimum delay required between ending Shift Mode and beginning Bypass Mode.
3. The minimum delay required before restarting normal RAM operation.
4. The minimum delay required before executing a Parallel Load operation.
5. The minimum delay required between a Parallel Load operation and a Shift.
6. Minimum Shift command hold time.

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BOUNDARY SCAN

OVERVIEW

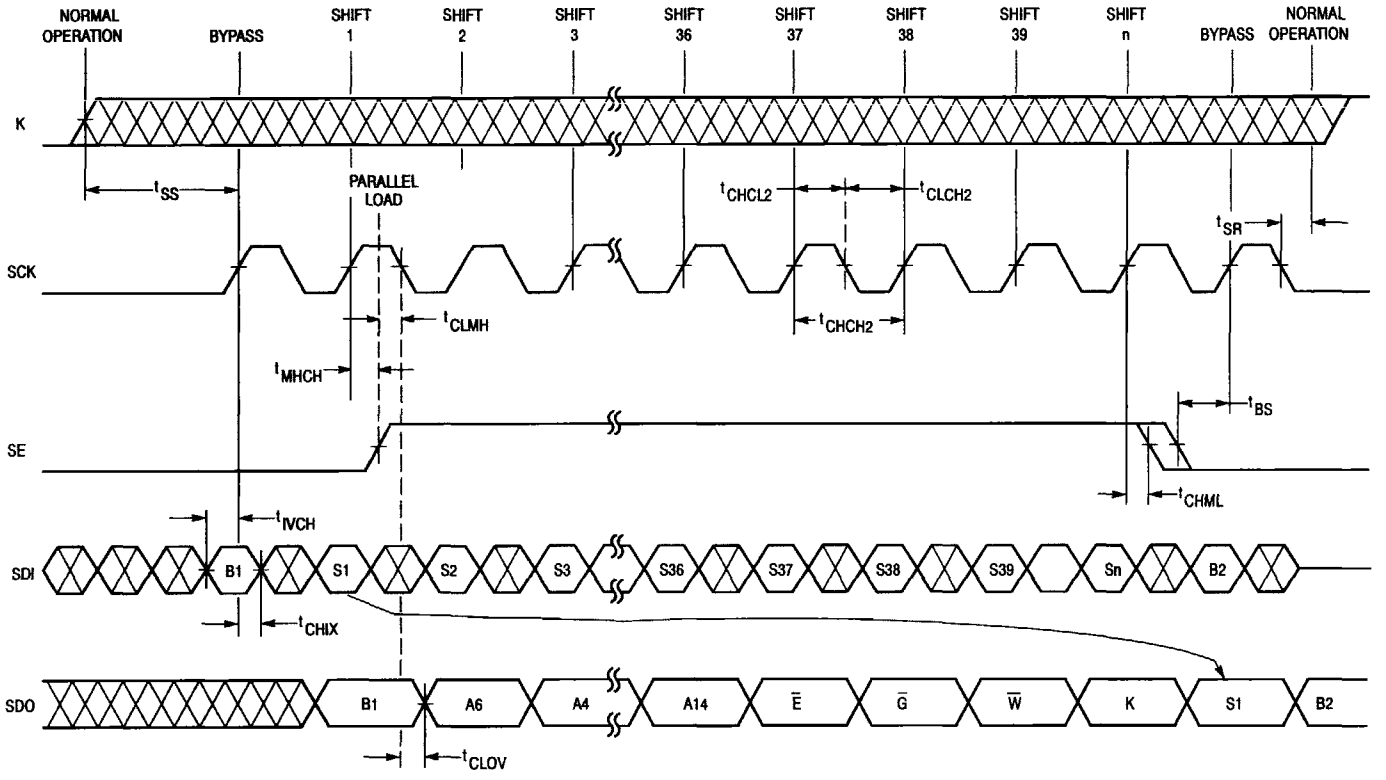
Boundary scan is a simple, non–intrusive scheme that allows verification of electrical continuity for each of a clocked RAM's logically active inputs and I/Os without adversely affecting RAM performance. Boundary scan allows the user to monitor the logic levels applied to each signal I/O on the RAM, and to shift them out in a serial bit stream.

OPERATION

Boundary scan requires four signal pins for implementation: Scan Data In (SDI), Scan Data Out (SDO), Scan Clock (SCK, active high), and Scan Enable (SE, active high).

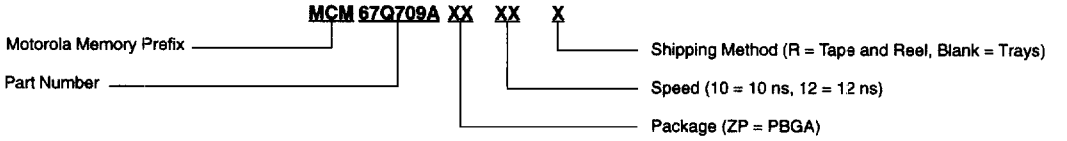
Boundary scan provides three modes of operation: (1) normal RAM operation, (2) scan, and (3) bypass. For normal RAM operation SCK and SE must be held low. The RAM will always return to normal operation immediately after the RAM receives a rising edge of the RAM input clock (K) with SCK and SE held low. To enter scan mode, SCK is activated. The first rising edge of SCK is used to latch in the data on the scan registers. SE is then driven high to disable additional input data from entering the scan registers. Every falling edge of SCK serially shifts data through the scan registers and onto the SDO pin. To enter bypass mode simply exercise SCK with SE held low. In this mode SDI is sampled on the rising edge of SCK. The level found on SDI is then driven out on SDO on the next falling edge of SCK.

BOUNDARY SCAN TIMING DIAGRAM



B1 and B2 = Bypass Serial Data from outside source
S1 – Sn + 1 = Serial Scan Data from outside source
S1 – Sn = RAMs Input Register contents
Scan Order is "A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, K"

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67Q709AZP10 MCM67Q709AZP12
MCM67Q709AZP10R MCM67Q709AZP12R

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