MACH120-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 48 Macrocells
- 12 ns t_{PD} Commercial
  18 ns t_{PD} Industrial
- 77 MHz f_{CNT} Commercial
- 56 Inputs
- 48 Outputs
- 48 Flip-flops; 4 clock choices
- 4 "PAL26V12" blocks
- Pin-compatible with MACH220 and MACH221

GENERAL DESCRIPTION

The MACH120 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately five times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH120 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH120 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

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BLOCK DIAGRAM