

TB62725AP, TB62725AF, TB62725AFN

8-bit Constant-Current LED Driver of the 3.3-V and 5-V Power Supply Voltage Operation

The TB62725AP, TB62725AF and TB62725AFN are comprised of constant-current drivers designed for LEDs and LED displays. The output current value can be set using an external resistor.

As a result, all outputs will have virtually the same current levels.

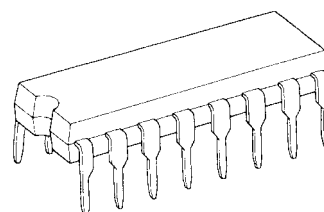
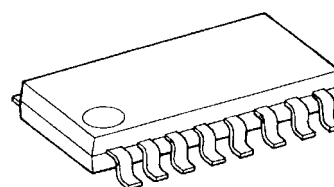
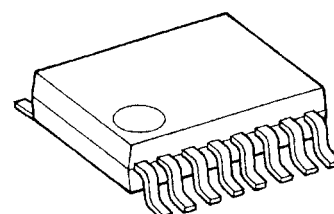
This driver incorporates a 8-bit constant-current output, a 8-bit shift register, a 8-bit latch circuit and a 8-bit AND-gate circuit.

These drivers have been designed using the Bi-CMOS process.

Features

- Output current capability and number of outputs:
90 mA $\times$ 8 outputs
- Constant current range: 2 to 80 mA
- Application output voltage:
0.7 V (output current 2 to 80 mA)
0.4 V (output current 2 to 40 mA)
- For anode-common LEDs
- Input signal voltage level: 3.3-V and 5-V CMOS level (schmitt trigger input)
- Maximum output terminal voltage: 17 V
- Serial data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range: $T_{opr} = -40$ to 85°C
- Package:
 - Type P: DIP16-P-300-2.54A
 - Type F: SSOP16-P-225-1.00A
 - Type FN: SSOP16-P-225-0.65B
- Package and pin layout: Pin layout and functionality are similar to those of the TB62705. (each characteristic value is different.)
- Constant-current accuracy (all outputs on)

Output Voltage	Current Error between Bits	Current Error between ICs	Output Current
≥ 0.4 V	$\pm 6\%$	$\pm 15\%$	2 to 40 mA
≥ 0.7 V			2 to 90 mA

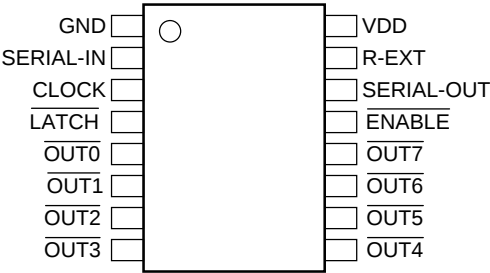
TB62725AP

DIP16-P-300-2.54A
TB62725AF

SSOP16-P-225-1.00A
TB62725AFN

SSOP16-P-225-0.65B

Weight

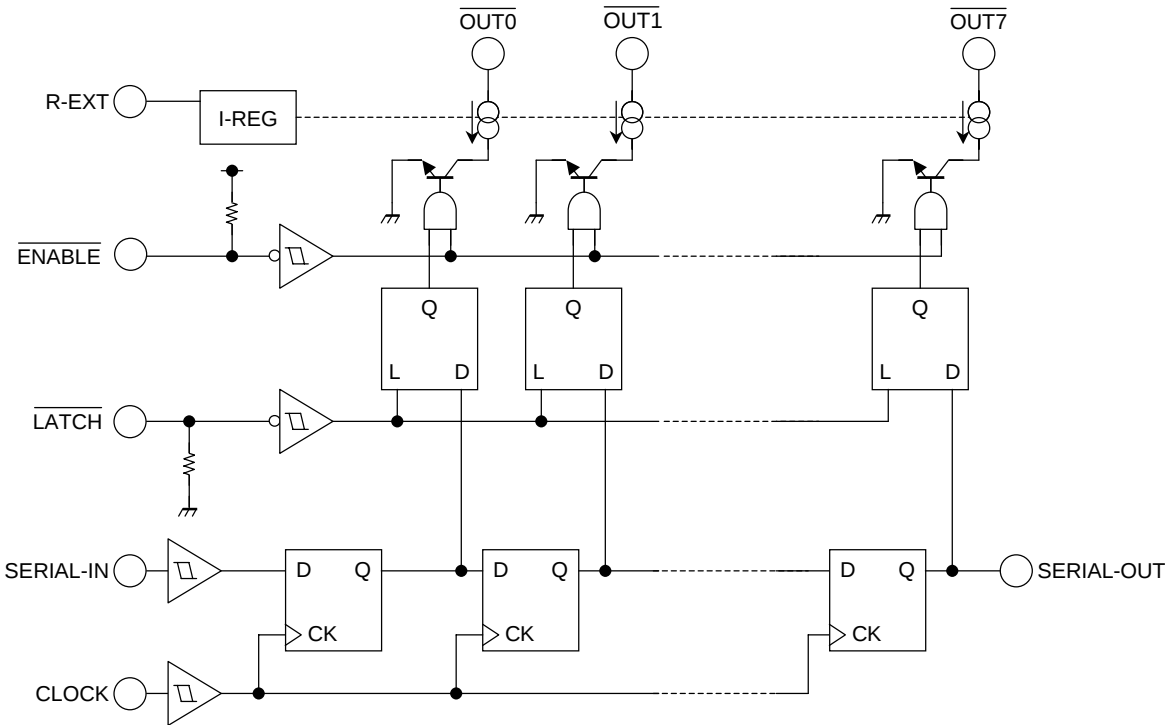
DIP16-P-300-2.54A: 1.11 g (typ.)
 SSOP16-P-225-1.00A: 0.14 g (typ.)
 SSOP16-P-225-0.65B: 0.07 g (typ.)

Pin Assignment (top view)

Pin layout and functionality are similar to those of the TB62705C. (each characteristic value is different.)



Block Diagram

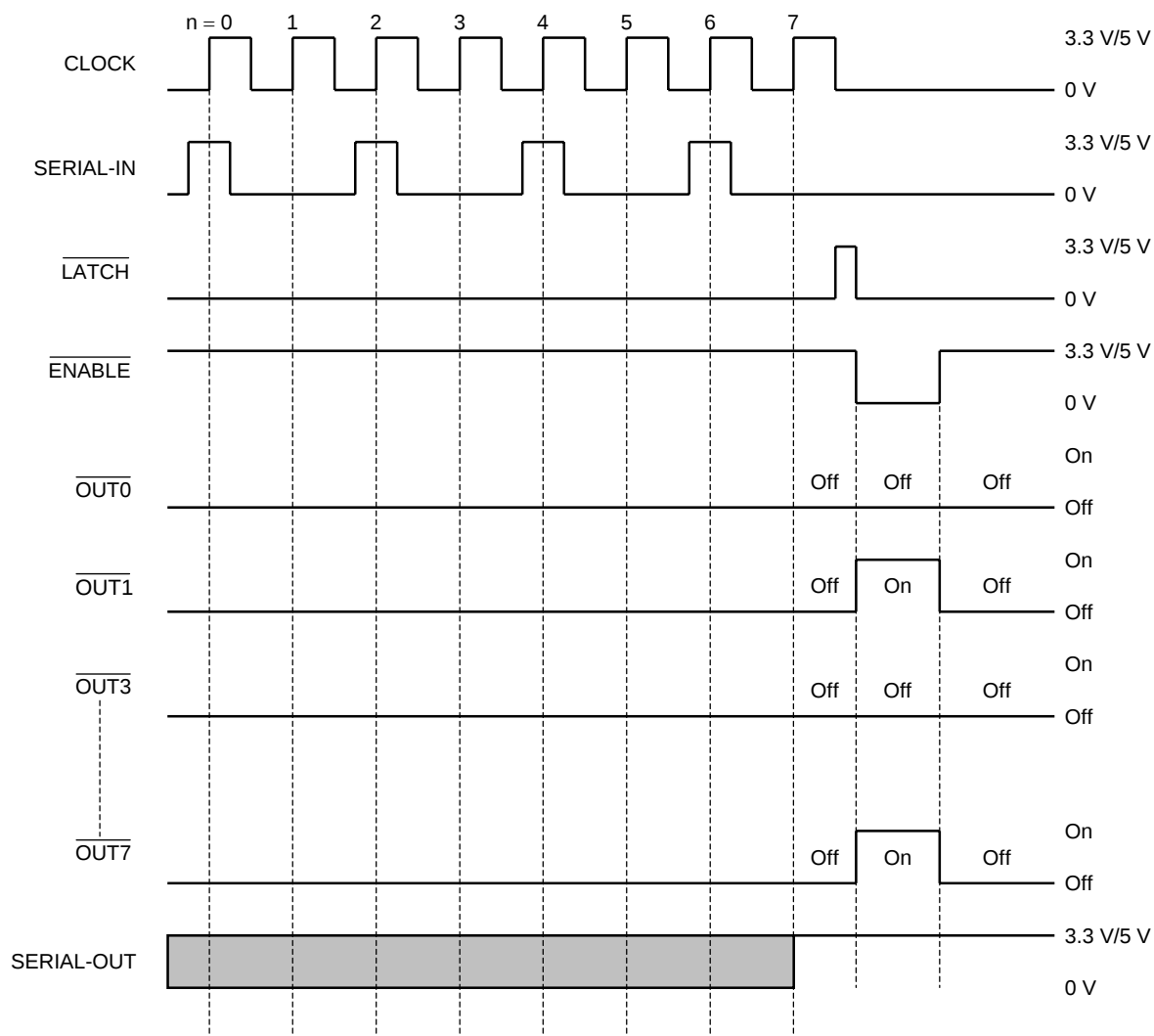


Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ... OUT5 ... OUT7	SERIAL-OUT
	H	L	Dn	Dn ... Dn - 5 ... Dn - 7	Dn - 7
	L	L	Dn + 1	No change	Dn - 6
	H	L	Dn + 2	Dn + 2 ... Dn - 3 ... Dn - 5	Dn - 5
	X	L	Dn + 3	Dn + 2 ... Dn - 3 ... Dn - 5	Dn - 5
	X	H	Dn + 3	Off	Dn - 5

Note 1: $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = On when Dn = H; $\overline{\text{OUT1}}$ to $\overline{\text{OUT7}}$ = Off when Dn = L.
In order to ensure that the level of the power supply voltate is correct, an external resistor must be connected between R-EXT and GND.

Timing Diagram



Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

Note 2: The latches circuit holds data by pulling the $\overline{\text{LATCH}}$ terminal Low.

And, when $\overline{\text{LATCH}}$ terminal is a high-level, latch circuit doesn't hold data, and it passes from the input to the output.

When $\overline{\text{ENABLE}}$ terminal is a low-level, output terminal $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ respond to the data, and on and off does.

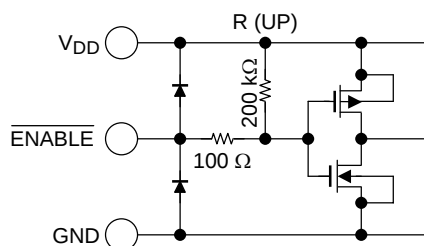
Attention: This IC can be used in 3.3 V or 5.0 V. However, use the V_{DD} power supply and the input level in the same voltage system.

Terminal Description

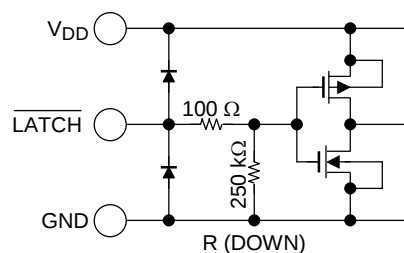
Pin No.	Pin Name	Function
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal for serial data for data shift register.
3	CLOCK	Input terminal for clock for data shift on rising edge.
4	$\overline{\text{LATCH}}$	Input terminal for data strobe. When the $\overline{\text{LATCH}}$ input is driven High, data is latched. When it is pulled Low, data is hold.
5 to 12	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	Constant-current output terminals.
13	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High. And are turned on, when the terminal is driven Low.
14	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal.
15	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
16	V _{DD}	3.3-V and 5-V supply voltage terminal.

Equivalent Circuits for Inputs and Outputs

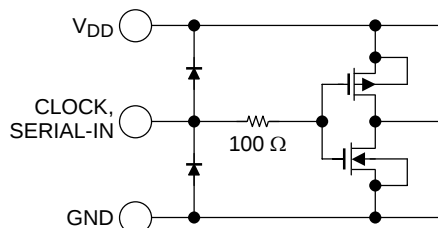
1. $\overline{\text{ENABLE}}$ Terminal



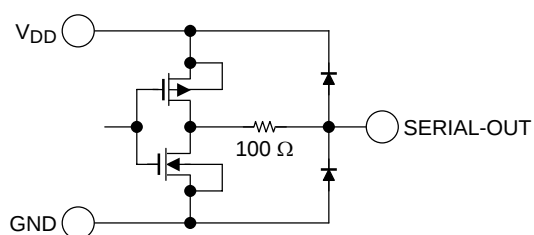
2. $\overline{\text{LATCH}}$ Terminal



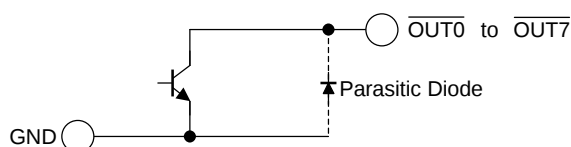
3. CLOCK, SERIAL-IN Terminal



4. SERIAL-OUT Terminal



5. $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ Terminals



Maximum Ratings (T_{opr} = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V _{DD}	6	V
Input voltage		V _{IN}	−0.2 to V _{DD} + 0.2	V
Output current		I _{OUT}	90	mA/ch
Output voltage		V _{OUT}	−0.2 to 17	V
Power dissipation (Note 3)	P-type (when not mounted)	P _{d1}	1.47	W
	AF/AFN-type (when not mounted)	P _{d2}	0.37	
	AF/AFN-type (on PCB)		0.78	
Thermal resistance (Note 3)	P-type (when not mounted)	R _{th (j-a)} 1	85	°C/W
	AF/AFN-type (when not mounted)	R _{th (j-a)} 2	330	
	AF/AFN-type (on PCB)	R _{th (j-a)} 3	160	
Operating temperature		T _{opr}	−40 to 85	°C
Storage temperature		T _{stg}	−55 to 150	°C

Note 3: P-type: Power dissipation is derated by 11.76 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

F- and FN-type: Power dissipation is derated by 7.69 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

With device mounted on glass-epoxy PCB of less than 40% Cu and of dimensions
50 mm × 50 mm × 1.6 mm

Recommended Operating Conditions (T_{opr} = −40°C to 85°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply voltage	V _{DD}	—	3		5.5	V
Output voltage	V _{OUT}	—	—	0.7	4	V
Output current	I _{OUT}	Each DC 1 circuit	2	—	80	mA/ch
	I _{OH}	SERIAL-OUT	—	—	−1	mA
	I _{OL}	SERIAL-OUT	—	—	1	
Input voltage	V _{IH}	—	0.7 × V _{DD}	—	V _{DD} + 0.15	mA
	V _{IL}		−0.15	—	0.3 × V _{DD}	
Clock frequency	f _{CLK}	Cascade Connected	—	—	20	MHz
$\overline{\text{LATCH}}$ pulse width	t _{wLATCH}	—	50	—	—	ns
$\overline{\text{ENABLE}}$ pulse width (Note 4)	t _{wENABLE}	I _{OUT} ≥ 20 mA	2000	—	—	ns
		I _{OUT} < 20 mA	3000	—	—	
CLOCK pulse width	t _{wCLOCK}	—	25	—	—	ns
Set-up time for CLOCK terminal	t _{SETUP1}		10	—	—	
Hold time for CLOCK terminal	t _{HOLD}		10	—	—	
Set-up time for $\overline{\text{LATCH}}$ terminal	t _{SETUP2}		50	—	—	

Note 4: When the pulse of the low level is inputted to the $\overline{\text{ENABLE}}$ terminal held in the high level.

Electrical Characteristics ($V_{DD} = 5\text{ V}$, $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
Supply voltage	V_{DD}	Normal operation		4.5	5	5.5	V
Output current	I_{OUT1}	$V_{OUT} = 0.4\text{ V}$, $V_{DD} = 3.3\text{ V}$	$R_{EXT} = 490\ \Omega$	29.84	35.10	40.36	mA
	I_{OUT2}	$V_{OUT} = 0.4\text{ V}$, $V_{DD} = 5\text{ V}$	$R_{EXT} = 250\ \Omega$	29.58	34.80	40.02	
	I_{OUT3}	$V_{OUT} = 0.7\text{ V}$, $V_{DD} = 3.3\text{ V}$	$R_{EXT} = 490\ \Omega$	58.40	68.70	79.00	
	I_{OUT4}	$V_{OUT} = 0.7\text{ V}$, $V_{DD} = 5\text{ V}$	$R_{EXT} = 250\ \Omega$	57.55	67.70	77.85	
Output current Error between bits	ΔI_{OUT1}	$V_{OUT} = 0.4\text{ V}$, All outputs ON	$R_{EXT} = 490\ \Omega$	—	± 1.5	± 6	%
	ΔI_{OUT2}	$V_{OUT} = 0.7\text{ V}$, All outputs ON	$R_{EXT} = 250\ \Omega$	—	± 1.5	± 6	
Output leakage current	I_{OZ}	$V_{OUT} = 15\text{ V}$		—	1	5	μA
Input voltage	V_{IH}	—		$0.7 V_{DD}$	—	V_{DD}	V
	V_{IL}	—		GND	—	$0.3 V_{DD}$	
SOUT terminal	V_{OL}	$I_{OH} = 1.0\text{ mA}$, $V_{DD} = 3.3\text{ V}$		—	—	0.3	V
		$I_{OH} = 1.0\text{ mA}$, $V_{DD} = 5\text{ V}$		—	—	0.3	
Output voltage	V_{OH}	$I_{OL} = -1.0\text{ mA}$, $V_{DD} = 3.3\text{ V}$		3	—	—	V
		$I_{OH} = 1.0\text{ mA}$, $V_{DD} = 5\text{ V}$		4.7	—	—	
Output current Supply voltage Regulation	$\%V_{DD}$	$V_{DD} = 3\text{ V} \rightarrow 5.5\text{ V}$		—	± 1.5	± 5.0	%
Pull-up resistor	$R_{(Up)}$	$\overline{\text{ENABLE}}$ terminal		100	200	400	$\text{k}\Omega$
Pull-down resistor	$R_{(Down)}$	$\overline{\text{LATCH}}$ terminal		125	250	500	$\text{k}\Omega$
Supply current	$I_{DD}(\text{OFF})\ 1$	$V_{OUT} = 15.0\text{ V}$	$R_{EXT} = \text{OPEN}$	—	0.1	0.5	mA
	$I_{DD}(\text{OFF})\ 2$	$V_{OUT} = 15.0\text{ V}$, All outputs OFF	$R_{EXT} = 490\ \Omega$	1	3	5	
	$I_{DD}(\text{OFF})\ 3$	$V_{OUT} = 15.0\text{ V}$, All outputs OFF	$R_{EXT} = 250\ \Omega$	3	6	8	
	$I_{DD}(\text{ON})\ 1$	$V_{OUT} = 0.7\text{ V}$, All outputs ON	$R_{EXT} = 490\ \Omega$	—	6	9	
		Same as the above, $T_{opr} = -40^\circ\text{C}$		—	—	15	
	$I_{DD}(\text{ON})\ 2$	$V_{OUT} = 0.7\text{ V}$, All outputs ON	$R_{EXT} = 250\ \Omega$	—	12	17	
		Same as the above, $T_{opr} = -40^\circ\text{C}$		—	—	29	

Switching Characteristics ($T_{opr} = 25^{\circ}\text{C}$ unless otherwise specified)

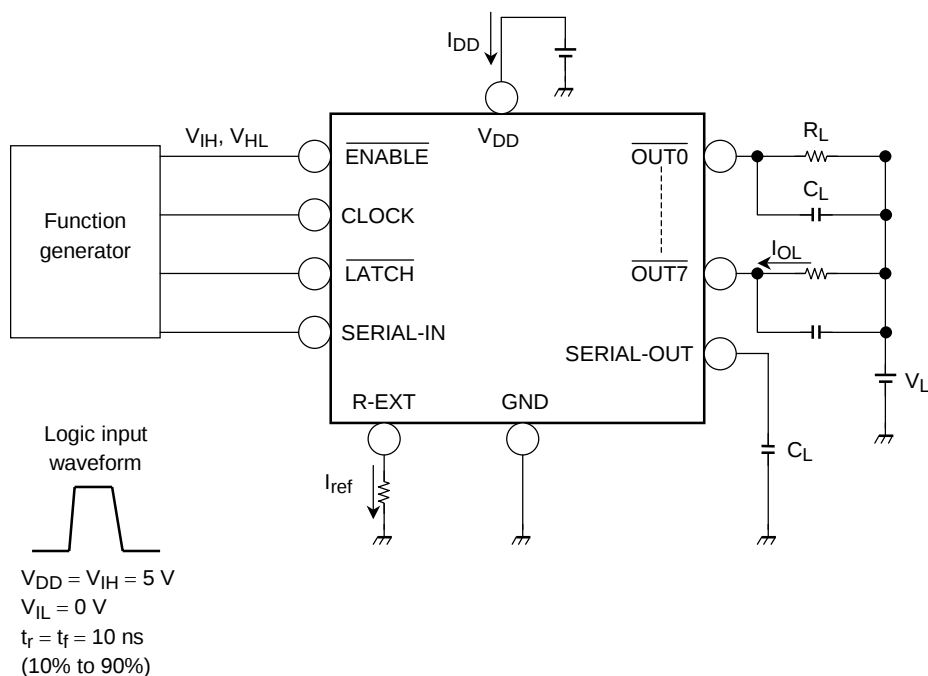
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Propagation delay time	t_{pLH1}	CLK to $\overline{\text{OUTn}}$, $\overline{\text{LATCH}} = \text{"H"}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	150	300	ns
	t_{pLH2}	$\overline{\text{LATCH}}$ to $\overline{\text{OUTn}}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	140	300	
	t_{pLH3}	$\overline{\text{ENABLE}}$ to $\overline{\text{OUTn}}$, $\overline{\text{LATCH}} = \text{"H"}$	—	140	300	
	t_{pLH}	CLK to SERIAL OUT	2	5	—	
	t_{pHL1}	CLK to $\overline{\text{OUTn}}$, $\overline{\text{LATCH}} = \text{"H"}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	170	340	
	t_{pHL2}	$\overline{\text{LATCH}}$ to $\overline{\text{OUTn}}$, $\overline{\text{ENABLE}} = \text{"L"}$	—	170	340	
	t_{pHL3}	$\overline{\text{ENABLE}}$ to $\overline{\text{OUTn}}$, $\overline{\text{LATCH}} = \text{"H"}$	—	170	340	
	t_{pHL}	CLK to SERIAL OUT	2	5	—	
Output rise time	t_{or}	10 to 90% of voltage waveform	40	85	150	ns
Output fall time	t_{of}	90 to 10% of voltage waveform	40	70	150	ns
Maximum clock rise time	t_r	Cascade connection isn't guarantee.	—	—	5	us
Maximum clock fall time	t_f	(Note 5)	—	—	5	us

Conditions: (refer to test circuit.)

$T_{opr} = 25^{\circ}\text{C}$, $V_{DD} = V_{IH} = 5\text{ V}$, $V_{OUT} = 0.7\text{ V}$, $V_{IL} = 0\text{ V}$, $R_{EXT} = 490\ \Omega$, $V_L = 5.0\text{ V}$, $R_L = 100\ \Omega$,
 $C_L = 10.5\text{ pF}$

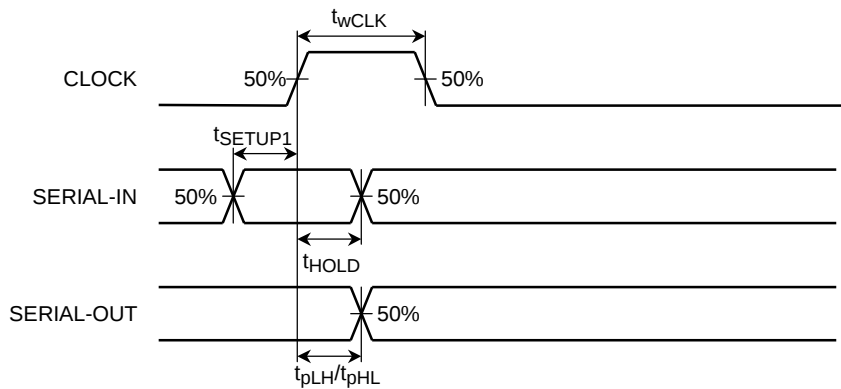
Note 5: If the device is connected in a cascade and t_r/t_f for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

Test Circuit

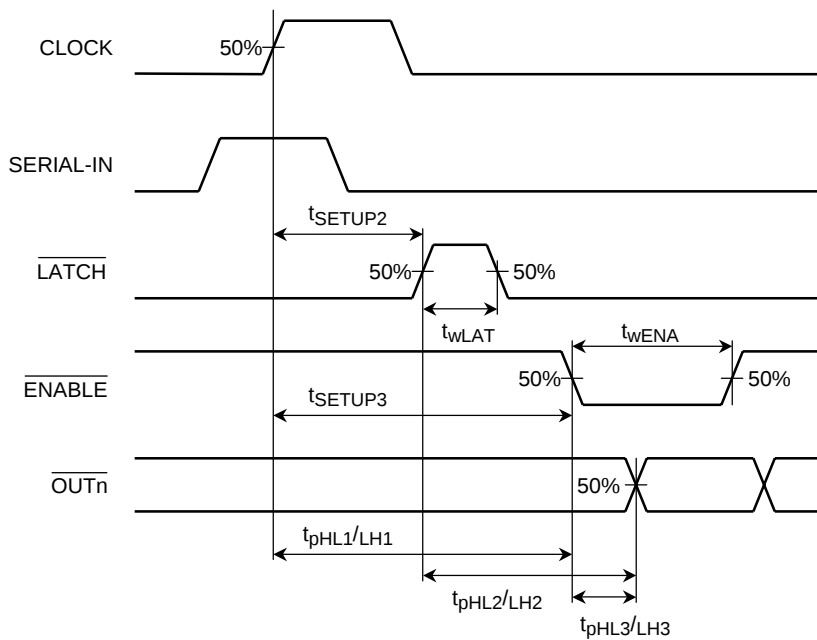


Timing Waveforms

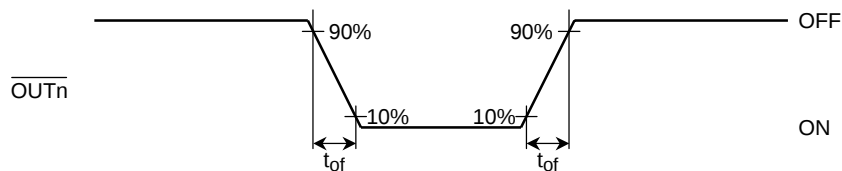
1. CLOCK, SERIAL-IN, SERIAL-OUT



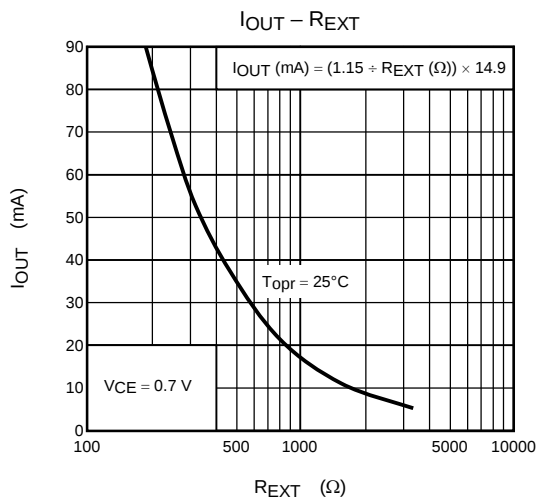
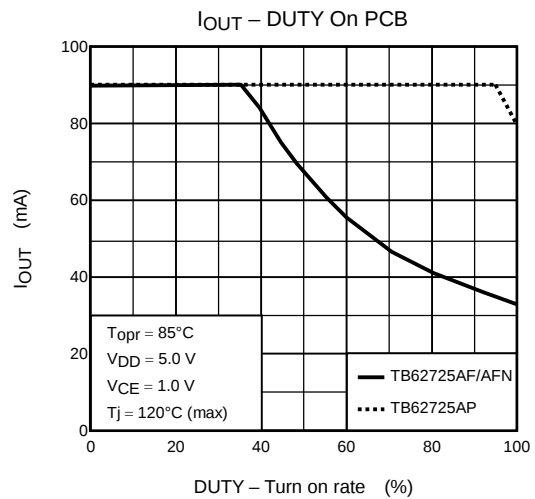
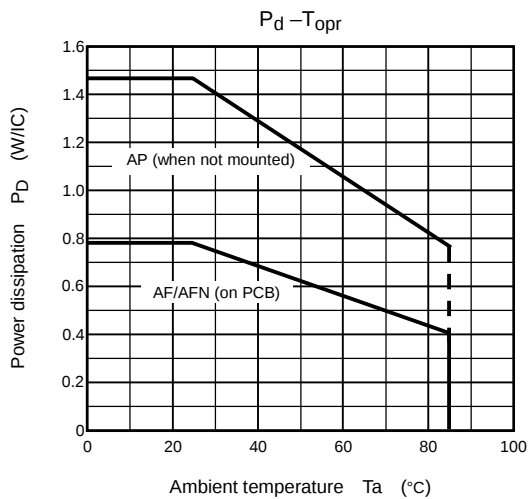
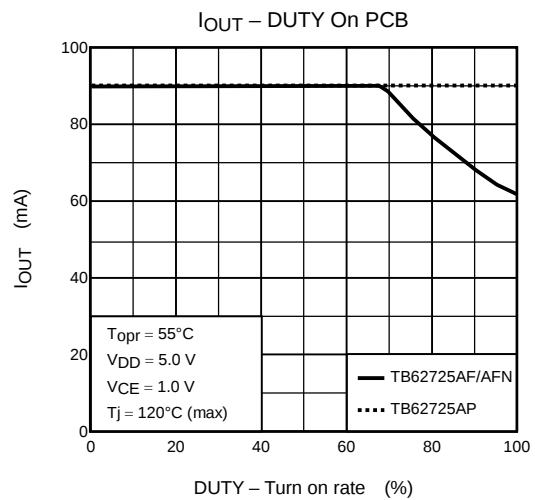
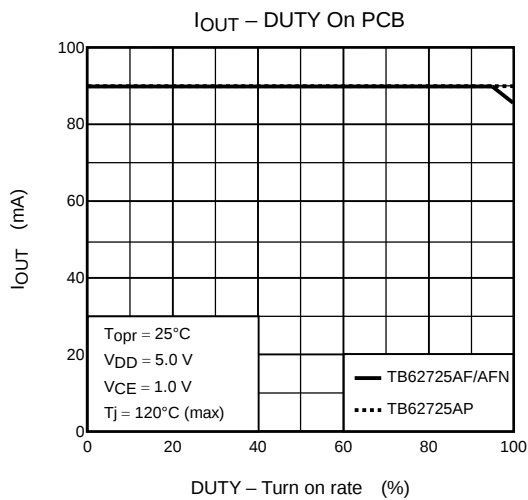
2. CLOCK, SERIAL-IN, $\overline{LATCH}$, $\overline{ENABLE}$, $\overline{OUTn}$



3. $\overline{OUTn}$



Output Current – Duty (LED turn-on rate)

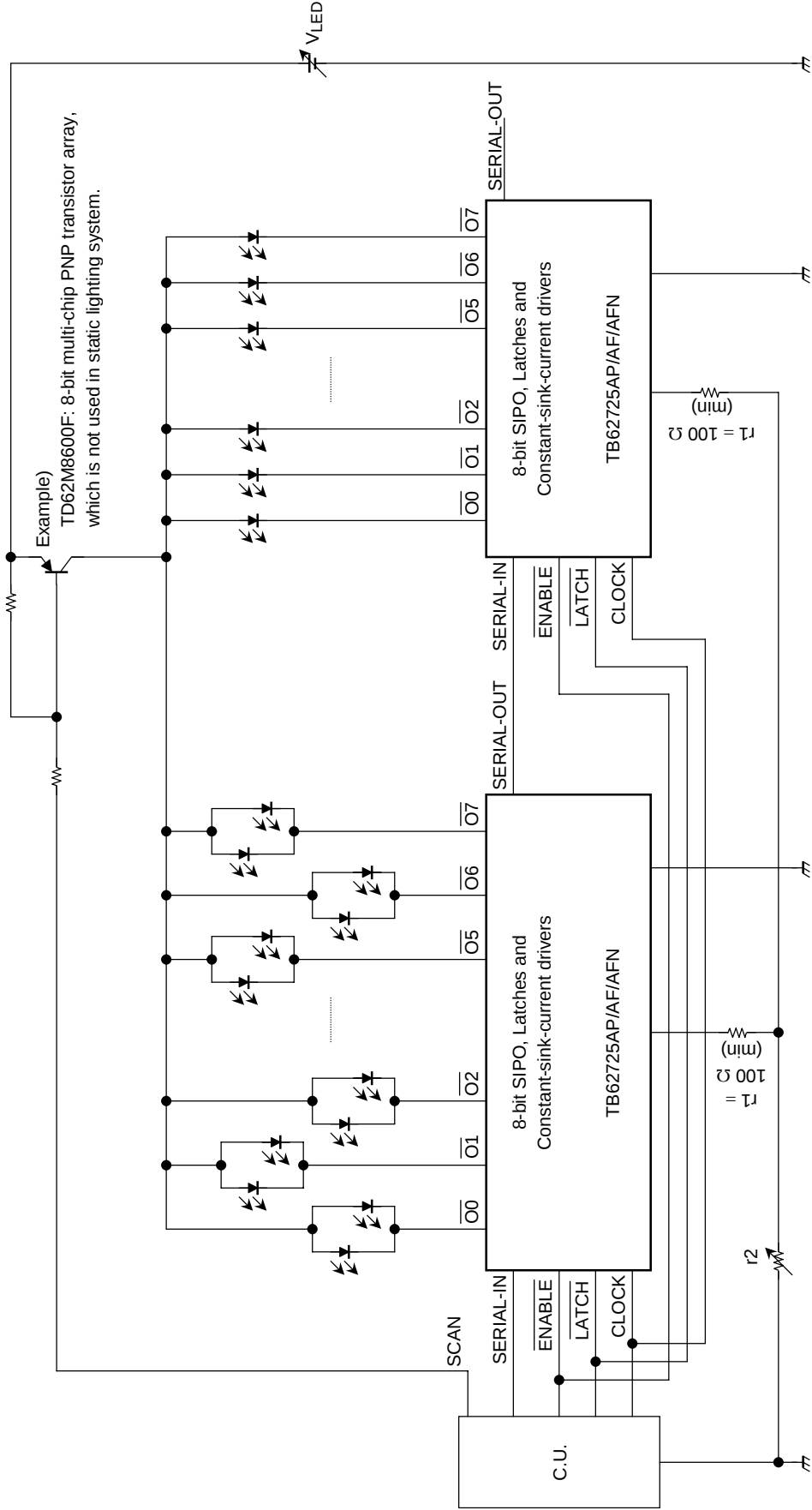


Application Circuit (example 1): The general composition in static lighting of LED.

More than $V_{LED} (V) \geq V_f (\text{total max}) + 0.7$ is recommended with the following application circuit with the LED power supply V_{LED} .

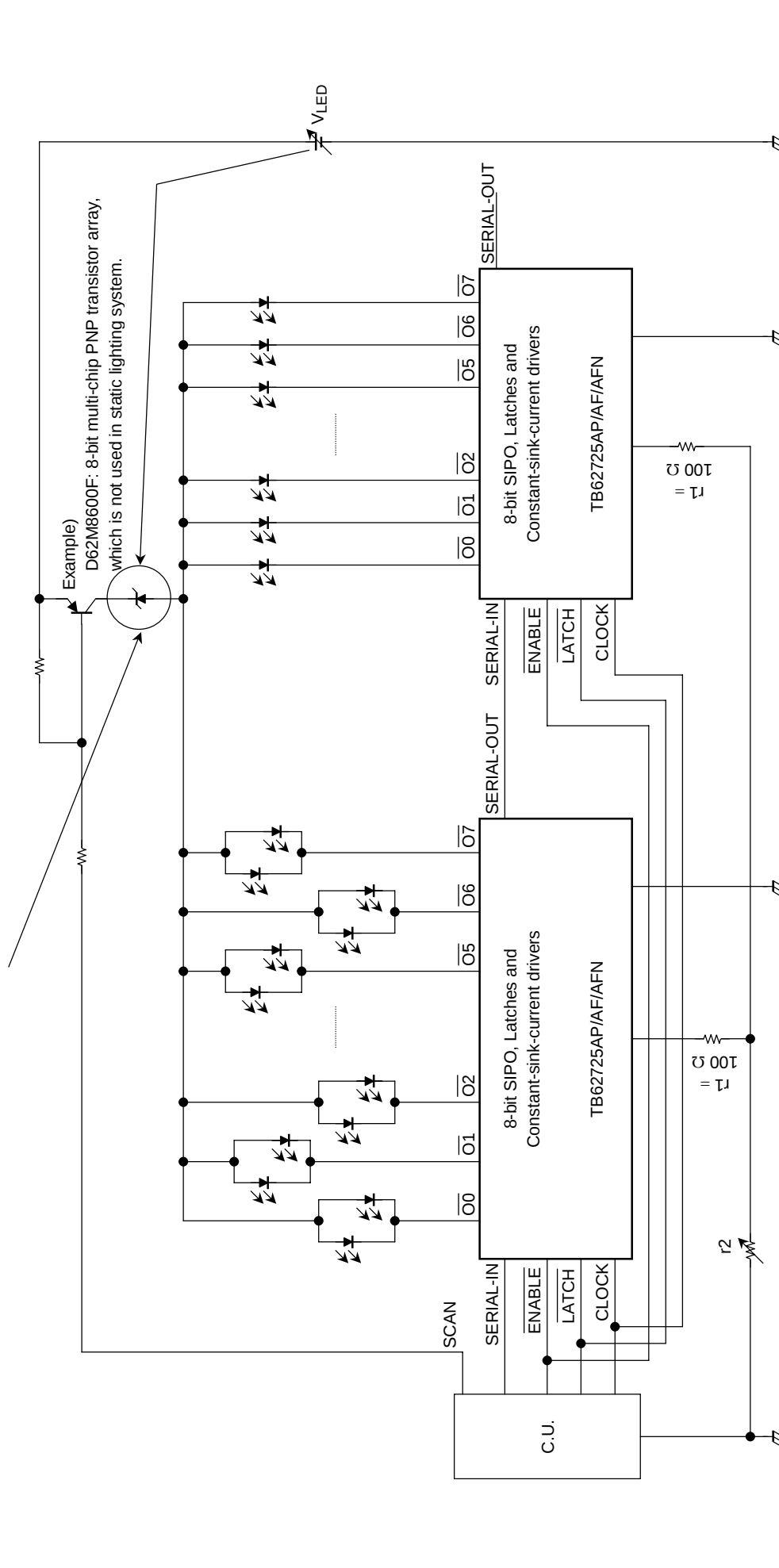
r1: The setup resistance for the setup of output current of every IC.

r2: The variable resistance for the brightness control of every LED module.



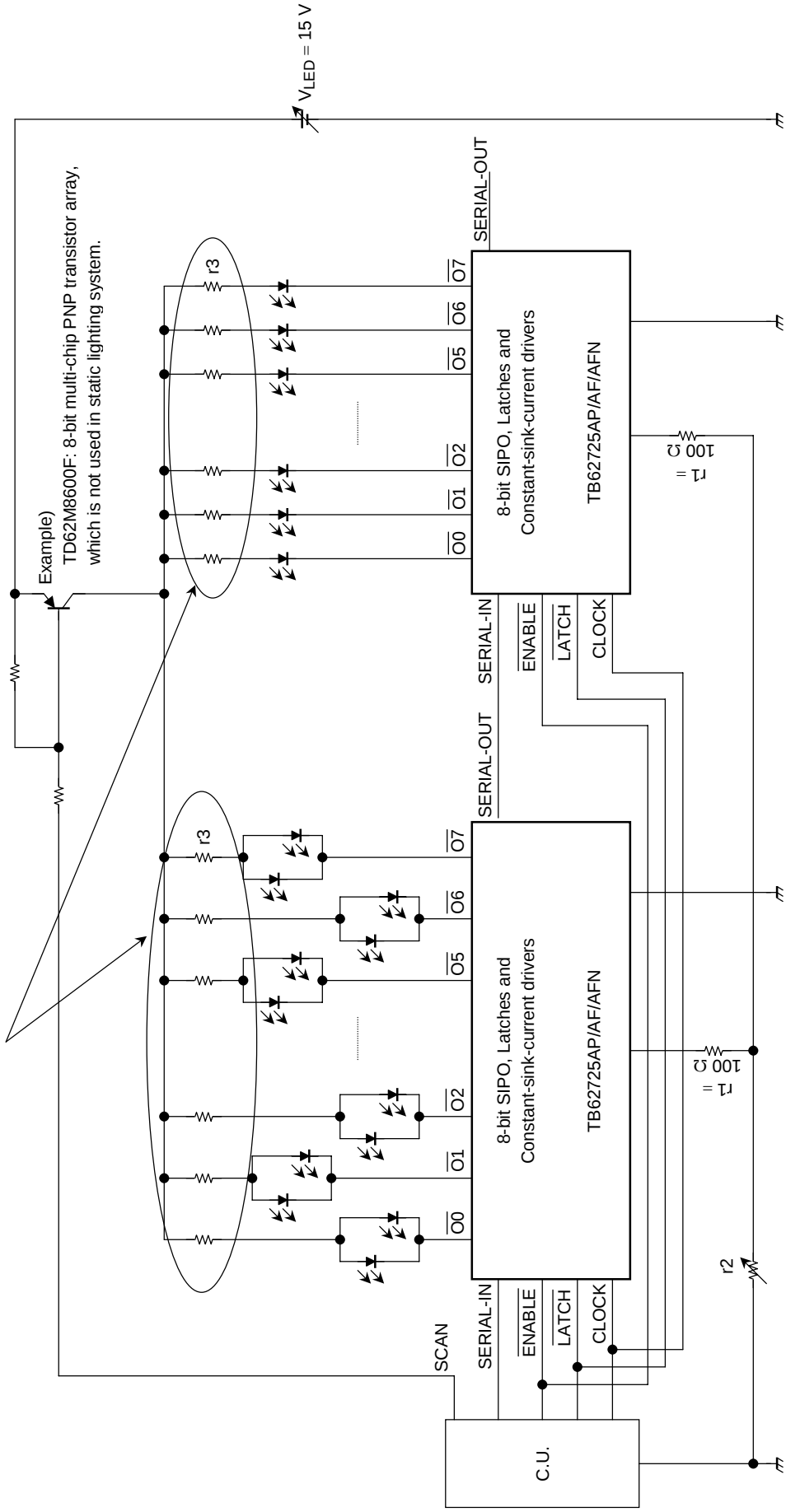
Application Circuit (example 2): When the condition of V_{LED} is $V_{LED} > 17\text{ V}$.

The unnecessary voltage is one effective technique as to making the voltage descend with the zenor diode.



Application Circuit (example 3): When the condition of V_{LED} is $V_f + 0.7 < V_{LED} < 17$ V.

$V_{OUT} = V_{LED} - V_f = 0.7$ to 1.0 V is the most suitable for V_{OUT} .
 Surplus V_{OUT} causes an IC fever and the useless consumption electric power.
 It is the one way of being effective to build in the $r3$ in this problem.
 $r3$ can make a calculation to the formula $r3 \text{ (ohms)} = \text{surplus } V_{OUT}/I_{OUT}$.
 Though the resistance parts increase, the fixed constant current performance is kept.



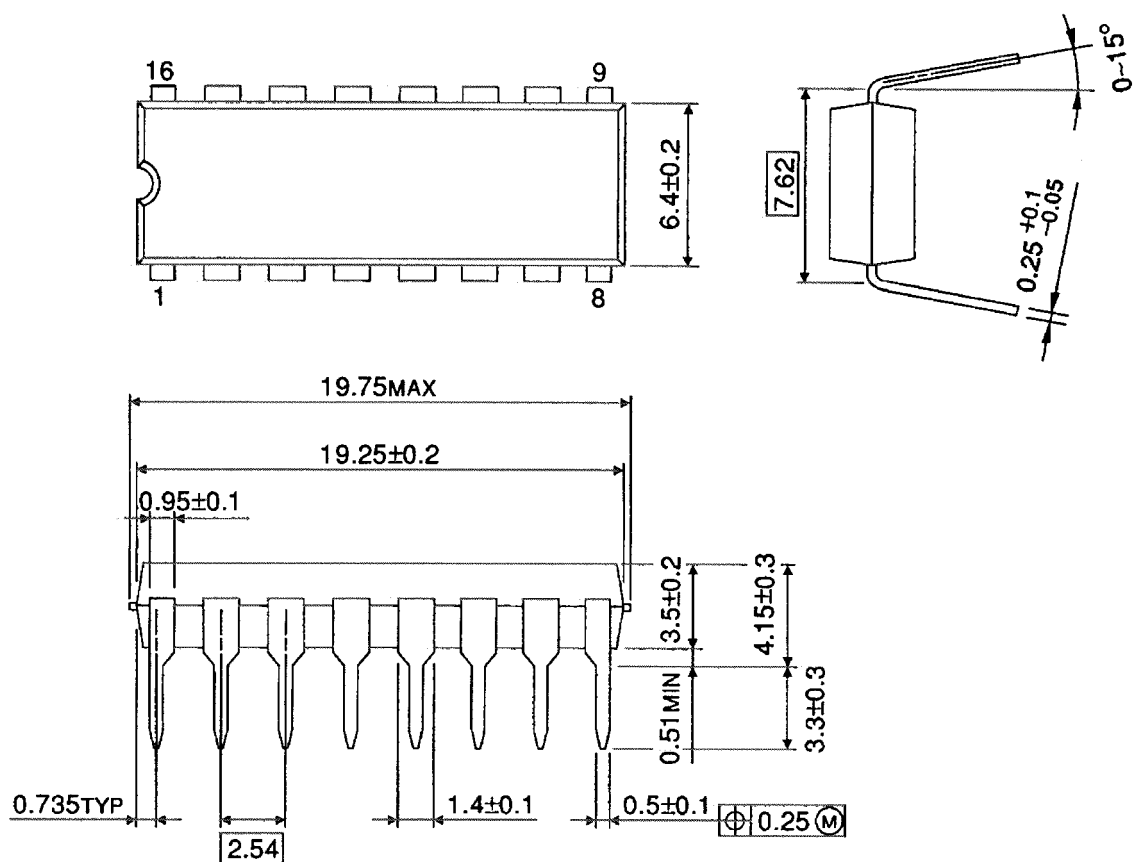
Notes

- Operation may become unstable due to the electromagnetic interference caused by the wiring and other phenomena.
To counter this, it is recommended that the IC be situated as close as possible to the LED module.
If overvoltage is caused by inductance between the LED and the output terminals, both the LED and the terminals may suffer damage as a result.
- There is only one GND terminal on this device when the inductance in the GND line and the resistor are large, the device may malfunction due to the GND noise when output switching by the circuit board pattern and wiring.
To achieve stable operation, it is necessary to connect a resistor between the REXT terminal and the GND line. Fluctuation in the output waveform is likely to occur when the GND line is unstable or when a capacitor (of more than 50 pF) is used.
Therefore, take care when designing the circuit board pattern layout and the wiring from the controller.
- This application circuit is a reference example and is not guaranteed to work in all conditions.
Be sure to check the operation of your circuits.
- This device does not include protection circuits for overvoltage, overcurrent or overtemperature.
If protection is necessary, it must be incorporated into the control circuitry.
- The device is likely to be destroyed if a short-circuit occurs between either of the power supply pins and any of the output terminals when designing circuits, pay special attention to the positions of the output terminals and the power supply terminals (VDD and VLED), and to the design of the GND line.

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

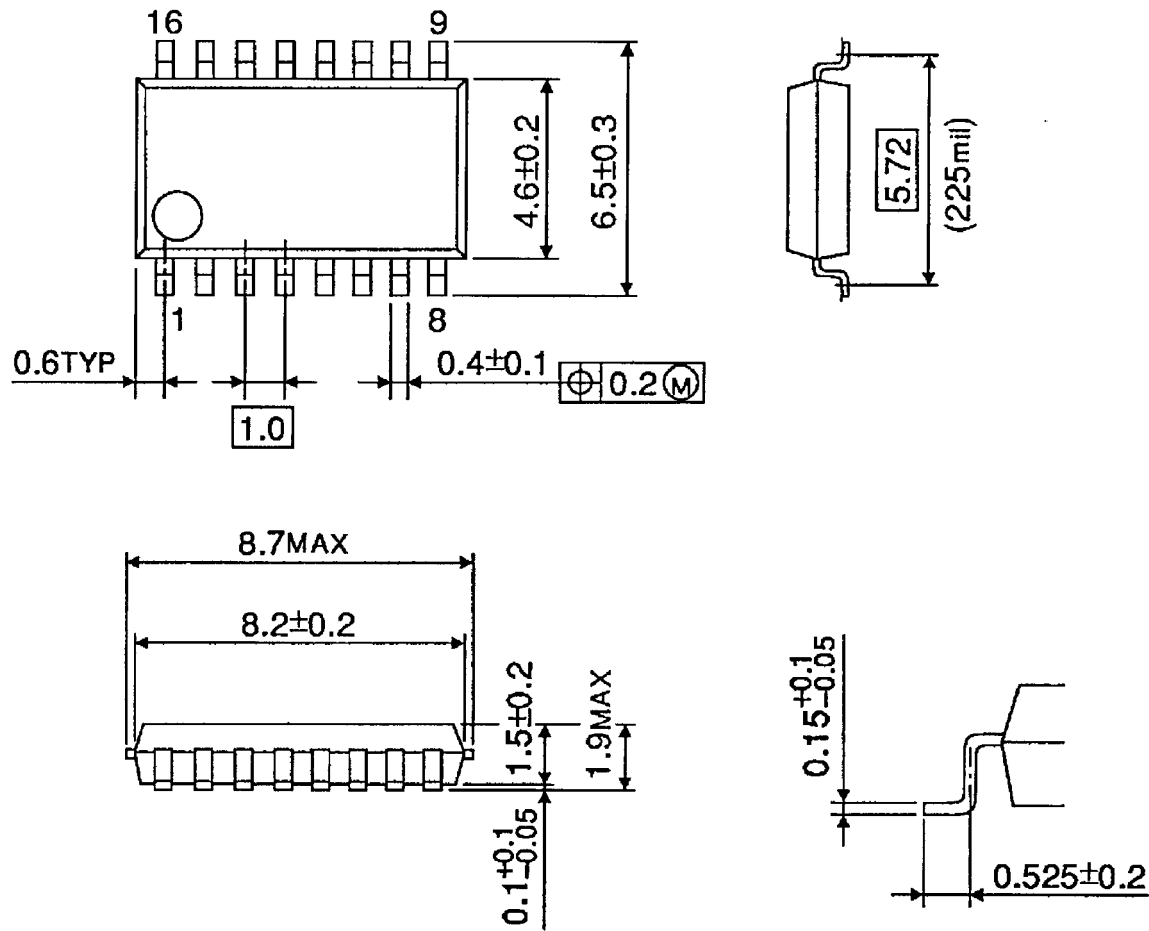


Weight: 1.11 g (typ.)

Package Dimensions

SSOP16-P-225-1.00A

Unit : mm

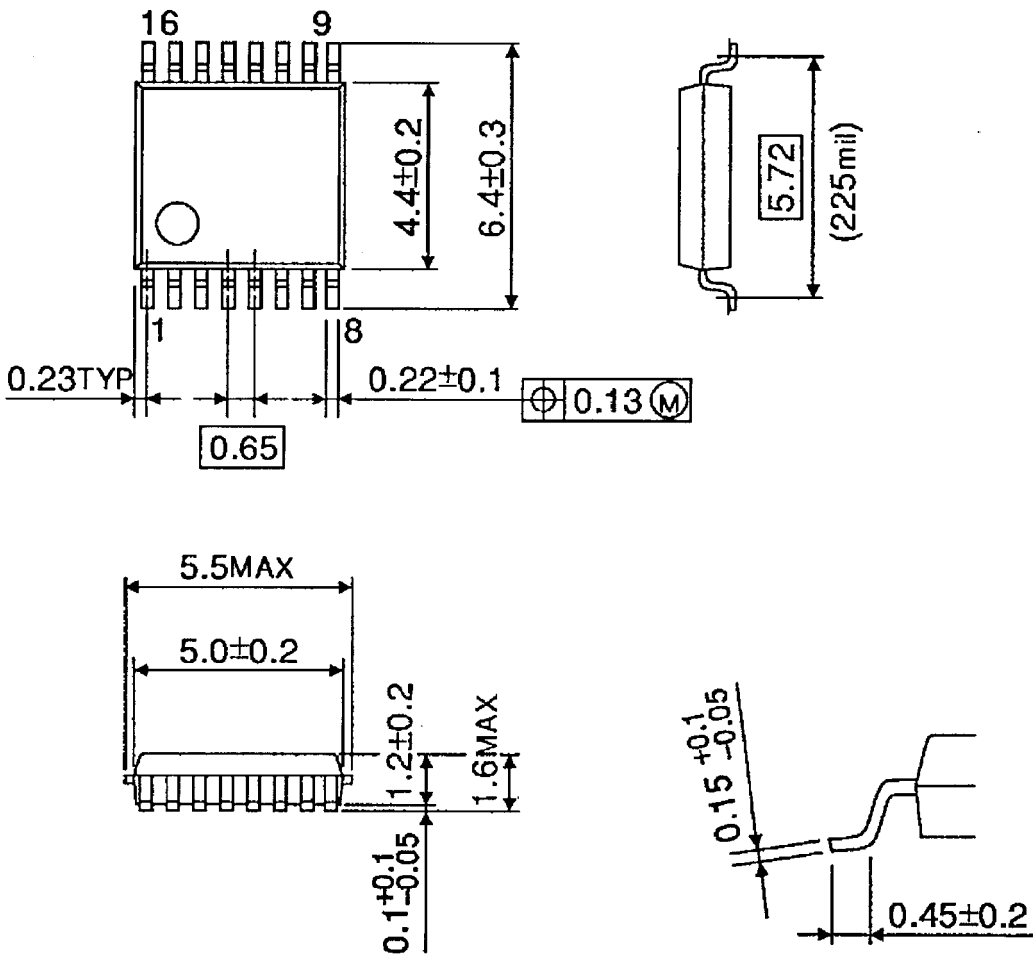


Weight: 0.14 g (typ.)

Package Dimensions

SSOP16-P-225-0.65B

Unit : mm



Weight: 0.07 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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