SSI 34P570
2-Channel Floppy Disk Read/Write Device

July, 1990

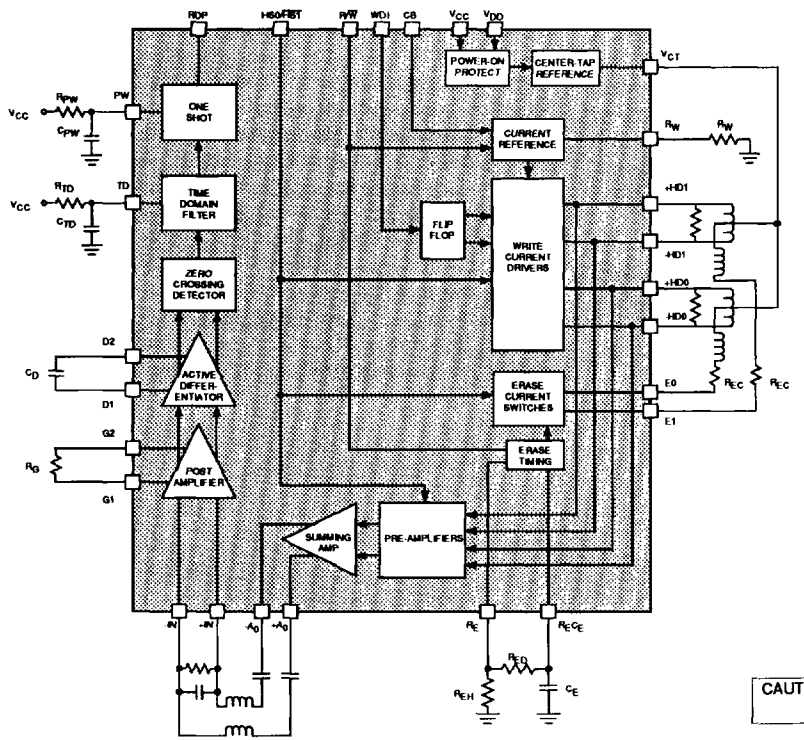
DESCRIPTION

The SSI 34P570 is an integrated circuit which performs the functions of generating write signals, amplifying and processing read signals required for a double-sided floppy disk drive. The write data circuitry includes switching differential current drivers and the erase head drive with programmable delay and hold times. The read data circuitry includes low noise amplifiers for each channel as well as a programmable gain stage and necessary equalization and filtering capability using external passive components. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility. The circuit operates on +12 volt and +5 volt power supplies and is available in 28-pin plastic DIP and PLCC packages.

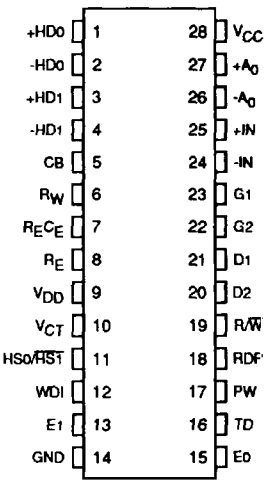
FEATURES

- **Single-chip read/write amplifier and read data processing function**
- **Compatible with 8", 5 1/4" and 3 1/2" drives**
- **Internal write and erase current sources, externally set**
- **Control signals are TTL compatible**
- **Schmitt trigger inputs for higher noise immunity on bussed control signals**
- **TTL selectable write current boost**
- **Operates on +12 volt and +5 volt power supplies**
- **High gain, low noise, low peak shift (0.3% typical) read processing circuits**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

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FUNCTIONAL DESCRIPTION

WRITE MODE CIRCUITRY

In Write Mode (R/$\overline{W}$ low), the circuit provides controlled write and erase currents to either of two magnetic heads. The write-erase circuitry consists of two differential write current drivers, a center tap voltage reference, two erase current switches and control circuits for head selection and erase timing.

Write current is toggled between opposing sides of the head on each negative transition of the write data input (WDI) and is set externally by a single resistor, Rw connected between the Rw terminal and ground. Since driver output impedance is large, proper damping resistors must be provided across each head. A signal at the CB terminal provides write current boost.

Erase current is also set externally through resistors REC connected in series with each erase coil. Erase can be activated by, but delayed from, selection of the write mode, and is held active after mode deselection. The turn-on delay is determined by the charging of CE through RED, while the hold time is determined by the discharge of CE through the series combination of RED and REH(see connection diagram). The RECE node may be driven directly by a logic gate, with external resistors per Figure 4, if the erase period is to be controlled separately from the write mode selection. For applications where no delays are required, CE is omitted.

The Center Tap Voltage Reference supplies both write and erase currents. A power turn-on protection circuit prevents undesired writing or erasure by holding the voltage reference off until the supply voltages are within their operating ranges.

READ MODE CIRCUITRY

In the Read Mode (R/$\overline{W}$ high), the circuit performs the functions of amplifying and detecting the selected head output pulses which correspond to magnetic transitions in the media. The read circuitry consists of two differential preamplifiers, a summing amplifier, a postamplifier, an active differentiator, a zero-crossing detector, a time domain filter, and an output one-shot.

The selected preamplifier drives the summing amplifier whose outputs are AC coupled to the postamplifier through an external filter network. The postamplifier adjusts signal amplitudes prior to application of signals to the active differentiator. Postamplifier gain is set as required by connecting a resistor across the gain terminals, G1 and G2. If desired, an additional frequency/phase compensation network may also be connected across these gain terminals.

The differentiator, driven by the postamplifier, provides zero-crossing output voltages in response to input signal peaks. Differentiator response characteristics are set by an external capacitor or more complex series network connected between the D1 and D2 terminals.

The zero-crossing detector provides a unipolar output for each positive or negative zero-crossing of the differentiator output. To enhance signal peak detection the time domain filter inhibits the detection of zero-crossings if they are not sufficiently separated in time. The filter period is set by an external RC network connected to the TD pin.

The time domain filter drives the output one-shot which generates uniform output data pulses. The pulse width is set by an external RC network connected to the PW pin. The output one-shot is inhibited while in the write mode.

ELECTRICAL CHARACTERISTIC Unless otherwise specified, 4.75 V ≤V_{CC} ≤5.25 V; 11.4 V ≤V_{DD}≤12.6; 0°C≤T_A≤70°C; R_W = 430 Ω; R_{ED} = 62 kΩ; C_E = 0.012 µF; R_{EH} = 62 kΩ; R_{EC} = 220 Ω

ABSOLUTE MAXIMUM RATINGS *(Operating above absolute maximum ratings may damage the device.)*

PARAMETER	RATING	UNIT
5 V Supply Voltage, V_{CC}	7	V
12 V Supply Voltage, V_{DD}	14	V
Storage Temperature	65 to +130	°C
Junction Operating Temperature	130	°C
Logic Input Voltage	-0.5 V to 7.0 V	dc
Lead Temperature (Soldering, 10 sec.)	260	°C
Power Dissipation	800	mW

POWER SUPPLY CURRENTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
I_{CC} - 5 V Supply Current	Read Mode			35	mA
	Write Mode			38	mA
I_{DD} - 12 V Supply Current	Read Mode			26	mA
	Write Mode (excluding Write & Erase currents)			24	mA

LOGIC SIGNALS - READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), CURRENT BOOST (CB)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low Voltage (V_{IL})				0.8	V
Input Low Current (I_{IL})	V_{IL} = 0.4 V			-0.4	mA
Input High Voltage (V_{IH})		2.0			V
Input High Current (I_{IH})	V_{IH} = 2.4 V			20	µA

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LOGIC SIGNALS - WRITE DATA INPUT (WDI), HEAD SELECT (HSO/$\overline{HS1}$)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Threshold Voltage, V_T+ Positive - going		1.4		1.9	V
Threshold Voltage, V_T - Negative - going		0.6		1.1	V
Hysteresis, V_T + to V_T-		0.4			V
Input High Current, I_{IH}	V_{IH} = 2.4V			20	µA
Input Low Current, I_{IL}	V_{IL} = 0.4V			-0.4	mA

CENTER TAP VOLTAGE REFERENCE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage (V_{CT})	I_{WC} + I_E = 3 mA to 60 mA	V_{DD} -1.5		V_{DD} - .5	V
Vcc Turn-Off Threshold	(See Note 1)	4.0			V
V_{DD} Turn-Off Threshold	(See Note 1)	9.6			V
V_{CT} Disabled Voltage				1.0	V

NOTE1: Voltage below which center tap voltage reference is disabled.

ERASE OUTPUTS (E1,E0)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Unselected Head Leakage	V_{E0}, V_{E1} = 12.6 V			100	µA
Output on Voltage (V_{E1}, V_{E0})	I_E = 50 mA			0.5	V

WRITE CURRENT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Unselected Head Leakage	V_{E1}, V_{E0} = 12.6 V			25	µA
Write Current Range	Rw = 820 Ω to 180 Ω	3		10	mA
Current Reference Accuracy	I_{WC} = 2.3/Rw V_{CB}(current boost) = 0.5 V	-5		+5	%
Write Current Unbalance	I_{WC} = 3 mA to 10 mA			1.0	%
Differential Head Voltage Swing	Δ I_{WC} ≤ 5%	12.8			Vpk
Current Boost	V_{CB} = 2.4 V	1.25 I_{WC}		1.35 I_{WC}	

ERASE TIMING

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Erase Delay Range	R_{ED} = 39 kΩ to 82 kΩ C_E= 0.0015 µF to 0.043 µF	0.1		1.0	msec
Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100\%$	T_{ED} = 0.69 R_{ED} C_E R_{ED} = 39 kΩ to 82 kΩ; C_E = 0.0015 µF to 0.043 µF	-15		+15	%
Erase Hold Range	R_{EH} + R_{ED} =78 kΩ to164 kΩ; C_E = 0.0015 µF to 0.043 µF	0.2		2.0	msec
Erase Hold Accuracy $\frac{\Delta T_{EH}}{T_{EH}} \times 100\%$	T_{EH}= 0.69 (R_{EH} + R_{ED}) C_E R_{EH} + R_{ED} = 78 kΩ to 164 kΩ; C_E= 0.0015 µF to 0.043 µF	-15		+15	%

ELECTRICAL CHARACTERISTICS (Unless otherwise specified: V_{IN} (Preamplifier) = 10 mVpp sine wave, dc coupled to center tap. (See Figure 1.) Summing Amplifier Load = 2 kΩ line-line, ac coupled. V_{IN} (Postamplifier) = 0.2 Vpp sine wave, ac coupled; R_G = open; Data Pulse Load = 1 kΩ to Vcc; C_D = 240 pF; C_{TD} = 100 pF; R_{TD} = 7.5 kΩ ; C_{PW} = 47 pF; R_{PW}= 7.5 kΩ.)

READ MODE

PREAMPLIFIER - SUMMING AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Freq. = 250 kHz	85		115	V/V
Bandwidth (-3 dB)		3			MHz
Gain Flatness	Freq. = dc to 1.5 MHz			±1.0	dB
Differential Input Impedance	Freq. = 250 kHz	20			kΩ
Max Differential Output Voltage Swing	V_{IN} = 250 kHz sine wave, THD ≤ 5%	2.5			Vpp
Small Signal Differential Output Resistance	Io ≤ 1.0 mApp			75	Ω
Common Mode Rejection Ratio	V_{IN} = 300 mVpp @ 500 kHz Inputs Shorted	50			dB
Power Supply Rejection Ratio	Δ V_{DD} = 300 mVpp @500 kHz Inputs shorted to V_{CT}.	50			dB
Channel Isolation	Unselected Channel V_{IN} 100 mVpp @ 500 kHz Selected channel input connected to V_{CT}	40			dB

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PREAMPLIFIER - SUMMING AMPLIFIER (cont'd.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Equivalent Input Noise	Power BW = 10 kHz to 1 MHz Inputs shorted to VCT.			10	µVrms
Center Tap Voltage, V_{CT}			1.5		V

POSTAMPLIFIER - ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ao, Differential Voltage Gain + IN, -IN to D1, D2	Freq. = 250 kHz (See Figure 2)	8.5		11.5	V/V
Bandwidth (-3 dB) + IN< -IN to D1, D2	C_D = 0.1 µF, R_D = 2.5 kΩ	3			MHz
Gain Flatness + IN, -IN to D1, D2	Freq. = dc to 1.5 MHz C_D = 0.1 µF, R_D = 2.5 kΩ			±1.0	dB
Max Differential Output Voltage Swing	V_{IN} = 250 kHz sine wave, ac coupled. ≤ 5% THD in voltage across C_D. (See Figure 2)	5.0			Vpp
Max Differential Input Voltage	V_{IN} = 250 kHz sine wave, ac coupled. ≤ 5% THD in voltage across C_D. R_G = 1.5 kΩ	2.5			2.5 Vpp
Differential Input Impedance		10			kΩ
Gain Control Accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G/(8 \times 10^3 + R_G)$ R_G = 2 kΩ	-25		+25	%
Threshold Differential Input Voltage. (See Note 2)	Min differential input voltage at post amp that results in a change of state at RDP V_{IN} = 250 kHz square wave, C_D = 0.1 µF, R_D = 500 Ω, T_R, TF ≤0.2 µsec No overshoot; Data Pulse from each V_{IN} . transition. (See Figure 3)			3.7	mVpp
Peak Differentiator Network Current		1.0			mA

NOTE 2: Threshold Differential Input Voltage can be related to peak shift by the following formula:

$$\text{Peak Shift} = \frac{3.7\,mv}{\pi Vin} \times 100\%$$

where Vin = peak to peak input voltage at post amplifier. Note that this formula demonstrates an inverse relationship between the input amplitude and the Peak Shift.

TIME DOMAIN FILTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	T_{TD} = 0.58 R_{TD} x (C_{TD} + 10^{-11}) +50 nsec, R_{TD} = 5 kΩ, to 10 kΩ $C_{TD} \geq$ 56 pF. V_{IN} = 50 mVpp @ 250 kHz square wave, T_R, $T_F \leq$ 20 nsec, ac coupled. Delay measured from 50% input amplitude to1.5 V Data Pulse	-15		+15	%
Delay Range	T_{TD} = 0.58 R_{TD} x (C_{TD} + 10^{-11}) + 50 nsec, R_{TD} = 5 kΩ to 10 kΩ, C_{TD} = 56 pF to 240 pF	240		2370	ns

DATA PULSE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	T_{PW} = 0.58 R_{PW} x (C_{PW} +8 x 10^{-12}) + 20 nsec. R_{PW} = 5 kΩ to 10 kΩ C_{PW} = ≥36 pF width measured at 1.5V amplitudes	-20		+20	%
Active Level Output Voltage	I_{OH} = 400 µA	2.7			V
Inactive Level Output Leakage	I_{OL} =4 mA			0.5	V
Pulse Width	T_{PW} = 0.58 R_{PW} x (C_{PW} +8 x10-12) + 20 nsec. R_{PW} = 5 kΩ to 10 kΩ C_{PW} = 36 pF to 200 pF	145		1225	ns

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TEST SCHEMATICS

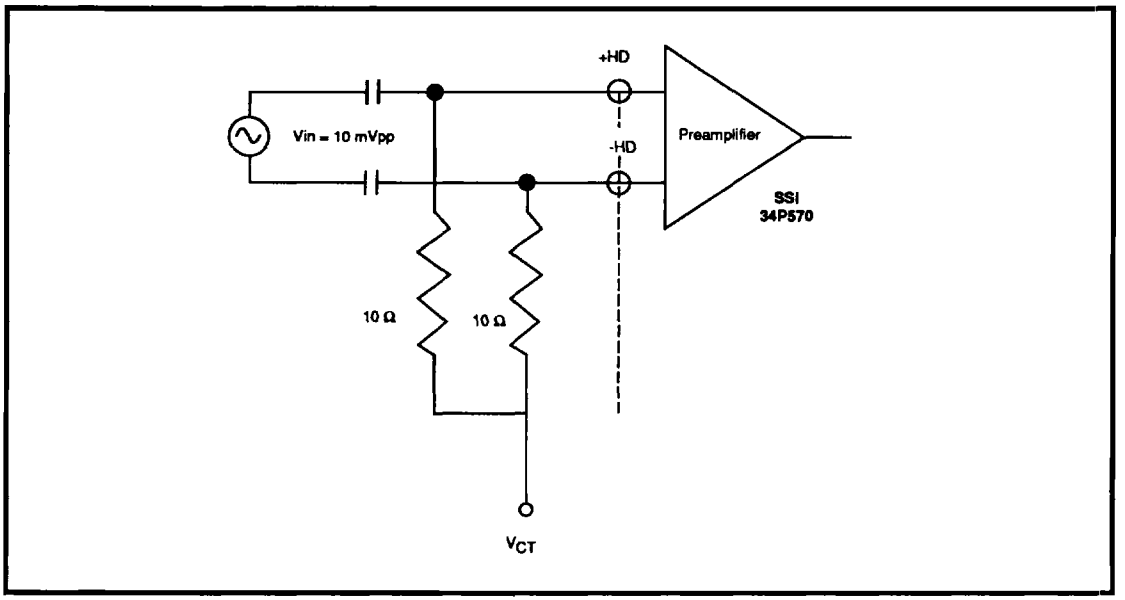

FIGURE 1: Preamplifier Characteristics

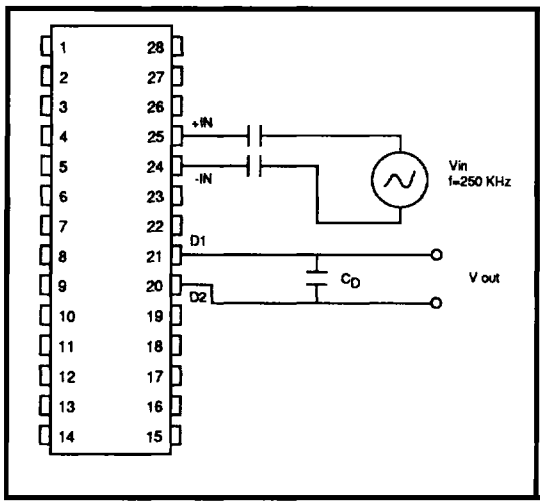

FIGURE 2:
Postamplifier Differential Output Voltage Swing and Voltage Gain

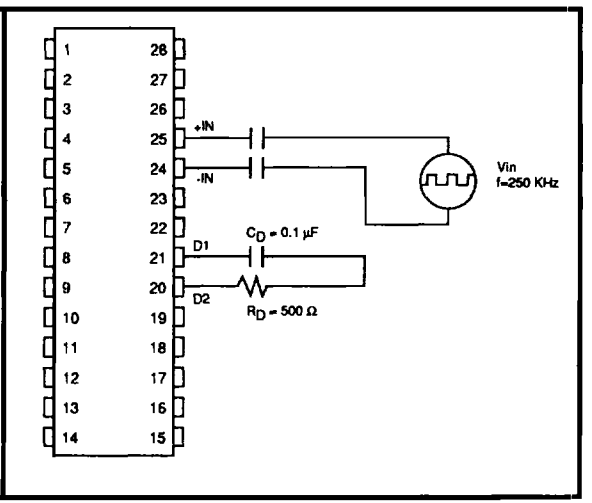

FIGURE 3:
Postamplifier Threshold Differential Input Voltage

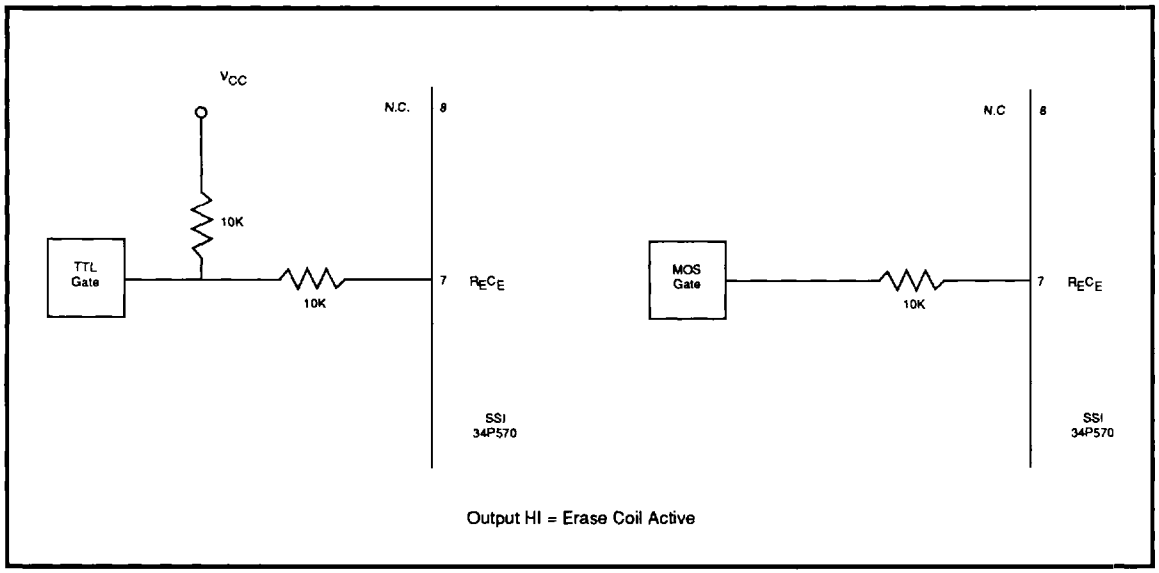

FIGURE 4 : External Erase Control Connections

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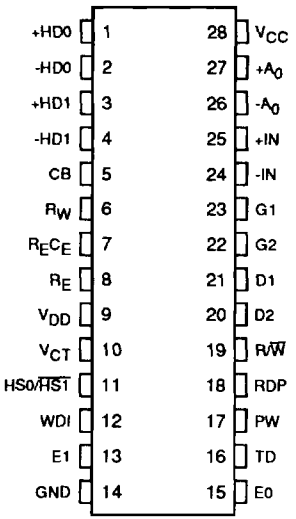
SSI 34P570
2-Channel Floppy Disk Read/Write Device

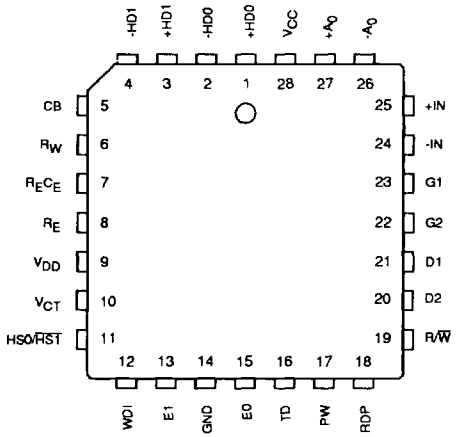
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-Pin DIP

THERMAL CHARACTERISTICS: Ø ja

28-Pin	DIP	55°C/W
28-Pin	PLCC	65°C/W



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34P570 28-Pin DIP	SSI 34P570-CP	34P570-CP
SSI 34P570 28-Pin PLCC	SSI 34P570-CH	34P570-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457