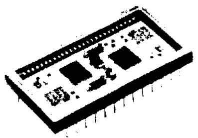
DDC ILC DATA DEVICE CORPORATION

SDC-14620 SERIES

TWO CHANNEL, PROGRAMMABLE SYNCHRO/RESOLVER-TO-DIGITAL CONVERTERS



PRELIMINARY

DESCRIPTION

The SDC-14620 Series are small, low-cost two-channel hybrid Synchro- or Resolver-to-Digital converters based on a single-chip monolithic. The two channels are independent but share the digital outputs and +5Vdc power pins. The package is 54 pin ceramic, the size of a 28 pin DDIP.

Resolution programming allows selection of 10, 12, 14, or 16 bit modes. This feature allows selection of either low resolution for fast tracking or higher resolution for higher accuracy.

The velocity outputs (VEL-A, VEL-B) from the SDC-14620 Series, which can be used to replace a tachometer, are ±4V signals referenced to analog ground with a linearity of 1% of output voltage.

The converter series also offers Built-In-Test outputs for each channel (BIT-A, BIT-B).

The SDC-14620 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C. 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14620 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- ***Single 5V power supply***
- ***10, 12, 14, or 16 bit programmable resolution***
- ***2 Independent Converters***
- ***Small 54 Pin Ceramic Package***
- ***BIT Output***
- ***Velocity Output Eliminates Tachometer***
- ***High-Reliability Single-Chip Monolithic per Channel***
- ***-55°C to +125°C Operating Temperature Range***
- ***883B Processing Available***

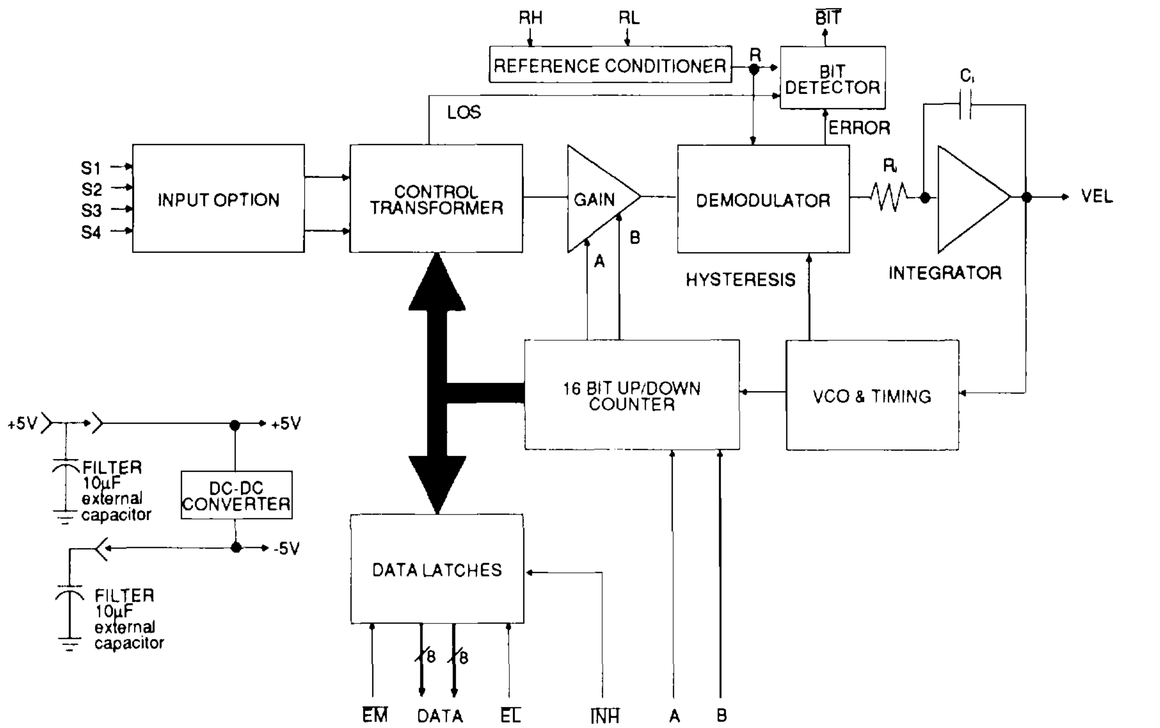


FIGURE 1. SDC-14620 BLOCK DIAGRAM (one channel)

TABLE 1. SDC-14620 SPECIFICATIONS (Each Channel)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. **Each Channel unless stated otherwise.**

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	programmable 10,12,14,or 16	
ACCURACY GRADES	Min	±2 or ±4, + 1LSB (see Table 4)	
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(RH,RL) **Each Channel**	
Type		differential	
		2 & 11.8V units	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5k	see note
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS		**Each Channel**	
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pF max. CMOS transient protected	
Resolution Control (A & B)		See Table 2.	
Each Channel		**Each Channel**	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$) Enable Bits 9 to 16 ($\overline{EL}$)		Logic 0 enables; Data stable within 150 ns. Logic 1 = High Impedance. Data High Z within 100 ns	
Outputs		**Common to Both Channels**	
Parallel Data	bits	16 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC-14620 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE	
DIGITAL INPUT/OUTPUT			
Outputs (continued)			
Each Channel		**Each Channel**	
Built -In-Test		Logic 0 = BIT condition. ± 100LSBs of error with a filter of 500µs. LOS or LOR	
Drive Capability	TTL	50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max. Logic 1; 10 TTL loads, -0.4 mA at 2.8V min	
	CMOS	Logic 0; 100mV max. Logic 1; +5V supply minus 100mV min	
VELOCITY CHARACTERISTICS		**Each Channel**	
Polarity		Positive for increasing angle	
Voltage Range(Full Scale)	±V	4.5 typ	4 min
Scale Factor	±%	10 typ	20 max
Scale Factor TC	ppm/°C	100 typ	200 max
Reversal Error	±%	1 typ	2 max
Linearity	±%	0.5 typ	1 max
Zero Offset	mV	5 typ	10 max
Zero Offset TC	µV/°C	15 typ	30 max
Load	kOhm		20 max
Noise	(Vp/V)%	1 typ	2 max
POWER SUPPLIES		**Total Device**	
Nominal Voltage	V	+5	
Voltage Range	±%	5	
Max Volt. w/o Damage	V	+7	
Current	mA	48 typ, 68 max	
TEMPERATURE RANGE			
Operating			
-30X	°C	0 to +70	
-10X	°C	-55 to +125	
Storage	°C	-65 to +150	
PHYSICAL CHARACTERISTICS			
Size	in(max) (mm)	1.50 x 0.78 x 0.21 (36.75 x 19.81 x 5.33)	
Weight	oz	0.66	

Note: 47 - 5k for 90V, 60Hz; 360 - 5k for 90V, 400Hz

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TABLE 2. RESOLUTION CONTROL (A&B)

Resolution	B	A
10 bit	0	0
12 bit	0	1
14 bit	1	0
16 bit	1	1

THEORY OF OPERATION

The SDC-14620 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology, which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

CONVERTER OPERATION

Figure 1 is the Functional Block Diagram of SDC-14620 Series. The converter operates with a single +5Vdc power supply and internally generates a minus voltage of approximately 5 volts. This minus voltage comes out on pin 24(channel 'B' filter point) and pin 52(channel 'A' filter point) — see GENERAL SETUP CONSIDERATIONS. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver, and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $\text{SIN}\theta\text{COS}\phi - \text{COS}\theta\text{SIN}\phi = \text{SIN}(\theta-\phi)$ using amplifiers, switches, logic, and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage, which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output), which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14620 Series converters:

1) The power supply is +5Vdc. For lowest noise performance it is recommended that a 10µF/10Vdc (or larger)tantalum filter capacitor be connected to ground (pin 19) near the converter package.
2) Direct inputs are referenced to A GND.
3) Connect (close to the hybrid) pins 5 & 32(Analog Ground) to pin 19(GND).
4) A 10µF/10Vdc tantalum filter capacitor must be added externally from pin 24(channel 'B' filter point) to pin 19 (ground). Furthermore, a 10µF/10Vdc tantalum filter capacitor must be added externally from pin 52(channel 'A' filter point)to pin 19 (ground).

SPECIAL FUNCTIONS

PROGRAMMABLE RESOLUTION

Resolution is controlled by Pins 49 and 50 for channel A; pins 21 and 22 for channel B . The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist, between counting and changing the resolution, the resolution control is latched internally. Refer to Table 2 for Channel A and B resolution control.

$\overline{\text{BIT}}$, BUILT-IN-TEST

This output is a logic line that will flag an internal fault condition, LOS (Loss-Of-Signal), or LOR (Loss-Of-Reference). The internal fault detector monitors the internal loop error and, when it exceeds ± 100LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500µs filter.) $\overline{\text{BIT}}$ will set for an overvelocity condition because the converter loop can't maintain input/output sync. $\overline{\text{BIT}}$ will also be set if either a LOS or LOR input occurs.

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

INTERFACING

SOLID-STATE BUFFER INPUT PROTECTION — TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high ac and dc common rejection , so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent ac peak + dc common mode voltage should not exceed the values in Table 1.

The 90V line-to-line systems may have voltage transients which exceed the 300V specification listed in Table 1. **These transients can destroy the thin-film input resistor network in the hybrid.** Therefore, 90V L-L solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever a synchro is switched on and off. For instance a 1000V transient can be generated when the primary of a CX or TX input is opened. See figure 2.

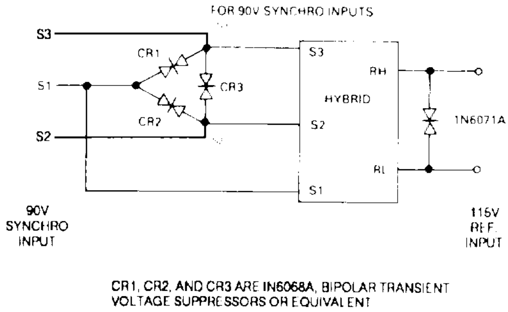

FIGURE 2. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in four bytes. The Enable MSB ($\overline{EM}$-A or $\overline{EM}$-B) is used for the most significant 8 bits and Enable LSB ($\overline{EL}$-A or $\overline{EL}$-B) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

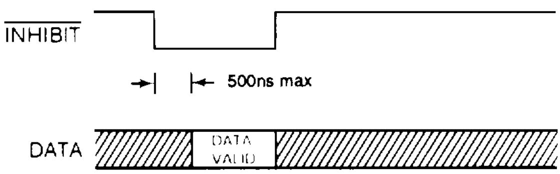

FIGURE 3. INHIBIT TIMING

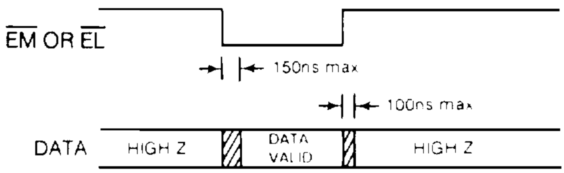

FIGURE 4. ENABLE TIMING

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DYNAMIC PERFORMANCE

A Type II servo loop ($K_v = \infty$) and very high acceleration constants give the SDC-14620 superior dynamic performance.

TRANSFER FUNCTION AND BODE PLOT

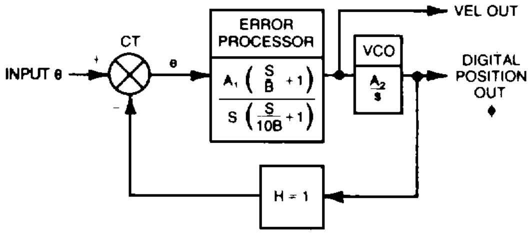
The dynamic performance of the converter can be determined from its Functional Block Diagram (figure 1), its transfer function block diagram (figure 5), and its Bode Plots (open and closed loop – figure 6). Values for the transfer function block can be obtained from Table 3.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation



$$\text{Open Loop Transfer Function} = \text{Output}\ \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}\qquad \text{WHERE: } A^2 = A_1A_2$$

FIGURE 5. TRANSFER FUNCTION BLOCK DIAGRAM

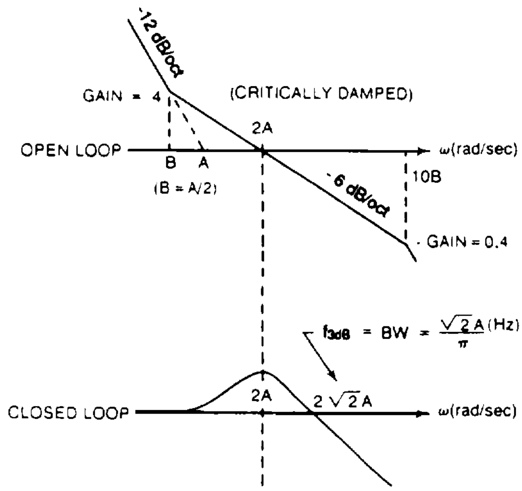


FIGURE 6. BODE PLOTS

ACCURACY AND RESOLUTION

Table 4 lists the total accuracy including quantinization for the various resolution and accuracy grades.

TABLE 4. ACCURACY/RESOLUTION

ACCURACY (minutes)	RESOLUTION (minutes) 10 BIT	12 BIT	14 BIT	16 BIT
±2 +1LSB	23.1	7.3	3.3	2.3
±4 +1LSB	25.1	9.3	5.3	4.3

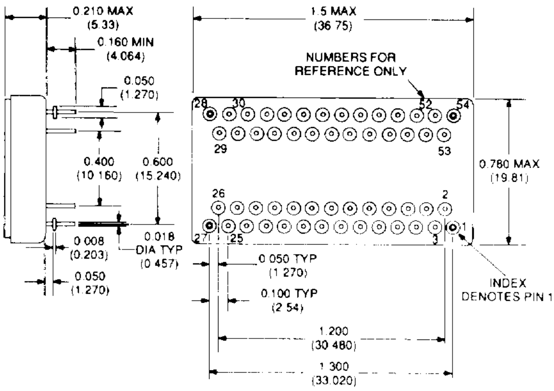
TABLE 3. DYNAMIC CHARACTERISTICS

Each Channel		DEVICE TYPE 60Hz				400Hz			
Input Frequency	Hz	47 - 5k				360 - 5k			
Bandwidth(Closed Loop)	Hz	15				103			
Ka	$1/s^2$	830				53k			
A1	1/s	0.17				1.33			
A2	1/s	5k				40k			
A	1/s	29				230			
B	1/s	14.5				115			
Resolution	**bits**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**
Tracking Rate (rps)									
typical	rps	32	8	2	0.5	160	40	10	2.5
minimum	rps	25.6	6.4	1.6	0.4	128	32	8	2
Accelleration (1LSB lag)	deg/s^2	720	180	45	11.3	18,600	4,640	1,160	290
Settling Time (179° step max)	msec	400	500	1,100	2,500	50	60	140	320

TABLE 4. PINOUT

Pin				Pin			
1	S1-A(R)	S1-A(S)	N.C.	54	VEL-A (Velocity Output chan.A)		
2	S2-A(R)	S2-A(S)	COS-A(D)	53	N.C.		
3	S3-A(R)	S3-A(S)	SIN-A(D)	52	Filter Point - Channel A		
4	S4-A(R)	N.C.	N.C.	51	$\overline{INH}$-A (Inhibit chan.B)		
5	A GND-A (analog gnd chan.A)			50	resolution control B (Channel A)		
6	RH-A (+Reference Input)			49	resolution control A (Channel A)		
7	RL-A (-Reference Input)			48	$\overline{EL}$-A (Enable LSBs chan. B)		
8	$\overline{EM}$-A (Enable MSBs chan. A)			47	N.C.		
9	$\overline{BIT}$-A (Built-In-Test chan. A)			46	Bit 16 (LSB, 16-bit mode)		
10	Bit 1 (MSB)			45	Bit 8		
11	Bit 9			44	Bit 15		
12	Bit 2			43	Bit 7		
13	Bit 10 (LSB, 10-bit mode)			42	Bit 14 (LSB, 14-bit mode)		
14	Bit 3			41	Bit 6		
15	Bit 11			40	Bit 13		
16	Bit 4			39	Bit 5		
17	Bit 12 (LSB, 10-bit mode)			38	$\overline{BIT}$-B (Built-In-Test chan. A)		
18	+5V (Power Supply)			37	$\overline{EM}$-B (Enable MSBs chan. B)		
19	GND (Ground)			36	N.C.		
20	$\overline{EL}$-B (Enable LSBs chan. B)			35	RL-B (-Reference Input)		
21	resolution control A (Channel B)			34	RH-B (+Reference Input)		
22	resolution control B (Channel B)			33	N.C.		
23	$\overline{INH}$-B (Inhibit chan.B)			32	A GND-B (analog gnd chan.B)		
24	Filter Point - Channel B			31	N.C.	S4-B(S)	N.C.
25	N.C.			30	S3-B(R)	S3-B(S)	+SIN-B(D)
26	VEL B (Velocity Output chan.B)			29	S2-B(R)	S2-B(S)	+COS-B(D)
27	N.C.			28	S1-B(R)	S1-B(S)	N.C.

Notes:
1. (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct
2. Connect (close to the hybrid) pins 5 & 32 to pin 19.
3. Connect a 10µF/10Vdc tantalum filter cap from pins 24 to pin 19.
4. Connect a 10µF/10Vdc tantalum filter cap from pin 52 to pin 19.
5. Connect a 10µF/10Vdc tantalum filter cap from pin 18 to pin 19.



NOTES:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ± 0.005 (0.127) of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is hermetically sealed ceramic package.

FIGURE 7. SDC-14620 MECHANICAL OUTLINE

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ORDERING INFORMATION

SDC- 1462X - X X X

Accuracy:
- 2 = 4 min + 1 LSB
- 4 = 2 min + 1 LSB

Reliability:
- 0 = Standard DDC procedures
- 1 = 883B Processing Available*
- 2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C (standard reliability only)

Input Option:
- 0 = 11.8V, Synchro, 400Hz
- 1 = 11.8V, Resolver, 400Hz
- 2 = 90V, Synchro, 400Hz
- 3 = 2V, Direct, 400Hz
- 4 = 90V, Synchro, 60Hz

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*** -55°C to +125°C temperature range only**