

P54/74PCT543/A P54/74PCT544/A OCTAL REGISTERED TRANSCEIVER

PRELIMINARY

T-52-31

FEATURES

- Full CMOS Implementation
- Low Power Operation
- 8-Bit Octal Transceiver with D Type Latches
- Separate Controls for Data Flow In Each Direction
- Back to Back Latches for Storage
- Fully TTL Compatible Input and Output Levels
- Three-State Output
- Produced with PACE II Technology™
- Compact Pinout
 - 24-Pin 300 mil DIP, SOIC
 - 28-Pad 450 mil sq. LCC

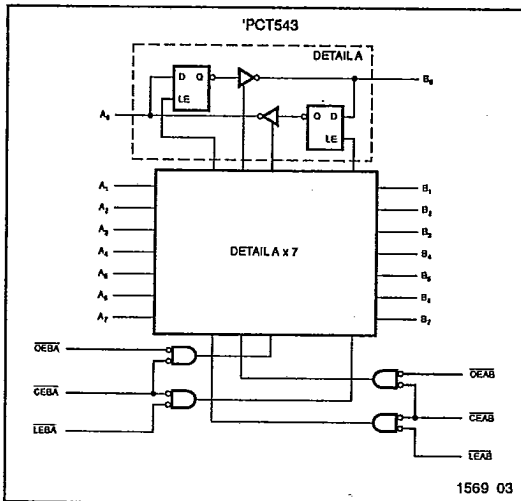
DESCRIPTION

The P54/74PCT543/A and P54/74PCT544/A Octal Registered Transceivers contain two sets of eight D-type latches with separate Latch Enable (LEAB, LEBA) and Output Enable (OEAB, OEBA) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable (OEAB) input must be LOW in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the truth table. With OEAB LOW, a

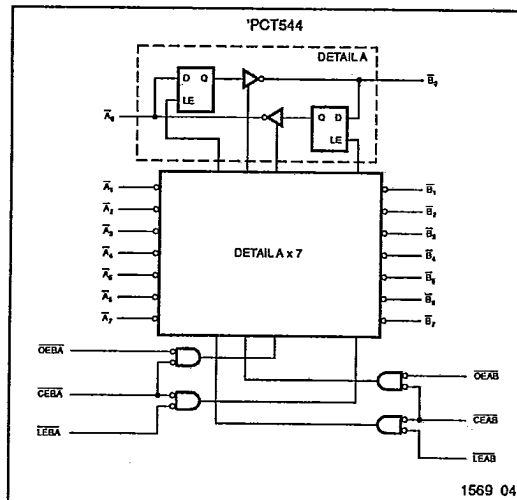
LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their output no longer change with the A inputs. With CEAB and OEAB both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses CEAB, LEAB and OEAB inputs.

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FUNCTIONAL BLOCK DIAGRAM



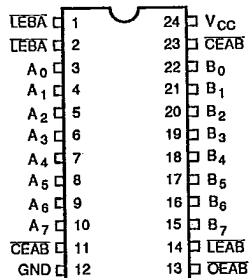
FUNCTIONAL BLOCK DIAGRAM



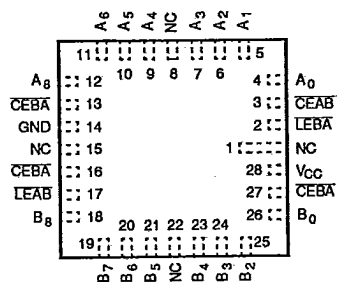
PIN CONFIGURATIONS

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'PCT543



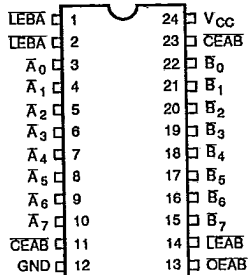
DIP (D4, P4) SOIC (S4)



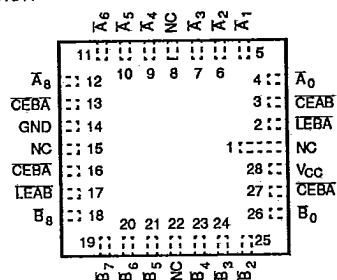
LCC (L5-1)

1569 05

'PCT544



DIP (D4, P4) SOIC (S4)

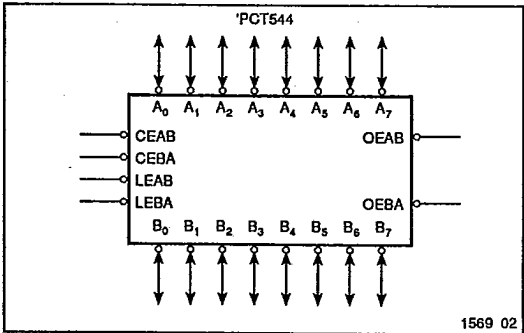
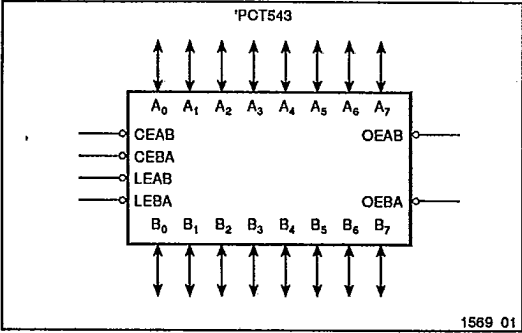


LCC (L5-1)

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LOGIC SYMBOL

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PIN DESCRIPTIONS

Pin Name	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Enable Input (Active LOW)
CEBA	B-to-A Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input (Active LOW)
LEBA	B-to-A Latch Enable Input (Active LOW)
A ₀ –A ₇	A-to-B Data Inputs or B-to-A 3-State Outputs
B ₀ –B ₇	B-to-A Data Inputs or A-to-B 3-State Outputs

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ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Ambient Temperature Under Bias	-55 to +125	°C
V _{CC}	V _{CC} Potential to Ground	-0.5 to +7.0	V
I _{IN}	Input Current	-30 to +5.0	mA

Notes: 1569 Tbl 02
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

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Symbol	Parameter	Value	Unit
I _{OUTPUT}	Current Applied to Output	100	mA
V _{IN}	Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{OUT}	Voltage Applied to Output	-0.5 to V _{CC} + 0.5	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V _{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0		V _{CC} + 0.5	V		
V _{IL}	Input LOW Voltage	-0.5		0.8	V		
V _H	Hysteresis		.35		V		All inputs
V _{CD}	Input Clamp Diode Voltage			-1.2	V	MIN	I _{IN} = -18mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V		V _{CC} - 0.2	V		I _{OH} = -32μA
		Military/Commercial (CMOS)		V _{CC} - 0.2	V	MIN	I _{OH} = -300μA
		Military (TTL)		2.4	V	MIN	I _{OH} = -12mA
		Commercial (TTL)		2.7	V	MIN	I _{OH} = -15mA
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V		0.2	V		I _{OL} = 300μA
		Military/Commercial (CMOS)		0.2	V	MIN	I _{OL} = 300μA
		Military (TTL)		0.55	V	MIN	I _{OL} = 48mA
		Commercial (TTL)		0.55	V	MIN	I _{OL} = 64mA
I _{IH}	Input HIGH Current			5	μA	MAX	V _{IN} = V _{CC}
I _{IL}	Input LOW Current			-5	μA	MAX	V _{IN} = GND
I _{IH}	Input HIGH Current ³			5	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current ³			-5	μA	MAX	V _{IN} = 0.5V
I _{IH}	Input HIGH Current (I/O Pins only)			15	μA	MAX	V _{IN} = V _{CC}
I _{IL}	Input LOW Current (I/O Pins only)			-15	μA	MAX	V _{IN} = GND
I _{IH}	Input HIGH Current ³ (I/O Pins only)			15	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current ³ (I/O Pins only)			-15	μA	MAX	V _{IN} = 0.5V
I _{OS}	Output Short Circuit Current ²	-60			mA	MAX	V _{OUT} = 0.0V
C _{IN}	Input Capacitance ³		5	10	pF		All inputs
C _{OUT}	Output Capacitance ³		9	12	pF		All outputs

Notes:

- Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- This parameter is guaranteed but not tested.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs) Mill	.003 .003	0.3 0.5	mA mA	$V_{CC} = \text{MAX}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, $f = 0$, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)		2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³		0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, $\overline{CEAB} + \overline{OEAB} = \text{Low}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open, $\overline{CEAB} = \text{High}$
I_{CC}	Total Power Supply Current ⁵		4.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ One Bit Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			5.6	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ One Bit Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$ $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
			7.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ Eight Bits Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			15.0 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, $\overline{CEAB} + \overline{OEAB} = \text{Low}$ 50% Duty Cycle, Outputs Open, $\overline{CEBA} = \text{High}$ Eight Bits Toggling at $f_1 = 5\text{MHz}$, $f_0 = \overline{LEAB} = 10\text{MHz}$ $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_{CC} = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD} (f_0/2 + f_1 N_I)$
 I_{CCQC} = Quiescent Current with CMOS input levels

I_{CCQT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_1 = Input Frequency

N_I = Number of Inputs at f_1

All currents are in milliamperes and all frequencies are in megahertz.

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TRUTH TABLE FOR A-TO-B (Symmetric with B-to-A)

Inputs			Latch Status	Outputs 'PCT543	Outputs 'PCT544
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0-B7	B0-B7
H	X	X	Storing	High Z	High Z
X	H	—	Storing	—	—
X	—	H	—	High Z	High Z
L	L	L	Transparent	Current A Inputs	Previous A Inputs
L	H	L	Storing	Previous A Inputs	Current A Inputs

* = Before $\overline{LEAB}$ LOW-to-HIGH Transition

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$

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AC CHARACTERISTICS

Sym.	Parameter	P54/74PCT543 P54/74PCT544					P54/74PCT543A P54/74PCT544A					Units	Fig. No.
		T _A =+25°C V _{CC} =+5.0V		MIL		COM'L	T _A =+25°C V _{CC} =+5.0V		MIL		COM'L		
		Typ.	Min. ¹	Max.	Min. ¹	Max.	Typ.	Min. ¹	Max.	Min. ¹	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	5.0 5.0	2.0 2.0	10.0 10.0	3.0 3.0	8.5 8.5	4.5 5.5	1.0 1.0	7.0 8.5	2.0 2.0	6.0 7.0	ns ns	1 5
t _{PLH} t _{PHL}	Propagation Delay LEBA to A _n LEBA to B _n	8.5 8.5	3.0 3.0	14.0 14.0	3.0 3.0	12.5 12.5	5.0 6.5	1.0 1.0	8.0 9.5	2.0 2.0	6.5 8.0	ns ns	1 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n	7.0 7.0	3.0 3.0	14.0 14.0	3.0 3.0	12.0 12.0	4.5 4.5	1.0 1.0	8.0 7.5	1.0 1.0	6.5 5.5	ns ns	1 7 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n	5.5 5.5	2.5 2.5	13.0 13.0	2.5 2.5	9.0 9.0	3.5 3.0	1.0 1.0	4.5 4.0	1.0 1.0	5.5 3.5	ns ns	1 7 8

Note: Minimum limits are guaranteed on Propagation Delays.

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AC OPERATING REQUIREMENTS

Sym.	Parameter	P54/74PCT543 P54/74PCT544					P54/74PCT543A P54/74PCT544A					Units	Fig. No.
		T _A =+25°C V _{CC} =+5.0V		MIL		COM'L	T _A =+25°C V _{CC} =+5.0V		MIL		COM'L		
		Typ.	Min. ¹	Max.	Min. ¹	Max.	Typ.	Min. ¹	Max.	Min. ¹	Max.		
t _s (H)	Set-up Time HIGH or LOW A _n or B _n to LEBA or LEAB	—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	9
t _s (L)	Set-up Time HIGH or LOW A _n or B _n to LEBA or LEAB	—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	9
t _h (H)	Hold Time HIGH or LOW A _n or B _n to LEBA or LEAB	—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	9
t _h (L)	Hold Time HIGH or LOW A _n or B _n to LEBA or LEAB	—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	9

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P54/74PCT543/A—P54/74PCT544A

AC OPERATING REQUIREMENTS

Sym.	Parameter	P54/74PCT543 P54/74PCT544					P54/74PCT543A P54/74PCT544A					Units	Fig. No.
		$T_A=+25^\circ\text{C}$ $V_{CC}=+5.0\text{V}$		MIL		COM'L	$T_A=+25^\circ\text{C}$ $V_{CC}=+5.0\text{V}$		MIL		COM'L		
		Typ.	Min. ¹	Max.	Min. ¹	Max.	Typ.	Min. ¹	Max.	Min. ¹	Max.		
t_s (H)	Set-up Time HIGH or LOW A_n or B_n to LEBA or LEAB	—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	9
t_s (L)		—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	
t_h (H)	Hold Time HIGH or LOW A_n or B_n to LEBA or LEAB	—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	9
t_h (L)		—	3.0	—	3.0	—	—	2.0	—	2.0	—	ns	

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ORDERING INFORMATION

PxxPCT Temp. Class	xxxx Device type	x Package	x Temperature	x Processing	
				B	MIL-STD-883, Class B
				C	0°C to +70°C
				M	−55°C to +125°C
				P	Plastic DIP
				D	CERDIP
				S	Small Outline IC
				L	Leadless Chip Carrier
				543	Non-Inverting Octal Registered Transceiver
				544	Inverting Octal Registered Transceiver
				543A	Fast Non-Inverting Octal Registered Transceiver
				544A	Fast Inverting Octal Registered Transceiver
				74	Commercial
				54	Military

1569 07