MOTOROLA

MC74AC153
MC74ACT153

Product Preview

Dual 4-Input Multiplexer

DUAL 4-INPUT
MULTIPLEXER

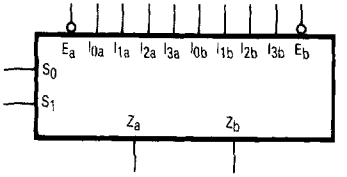
The MC74AC153/74ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the MC74AC153/74ACT153 can act as a function generator and generate any two functions of three variables.

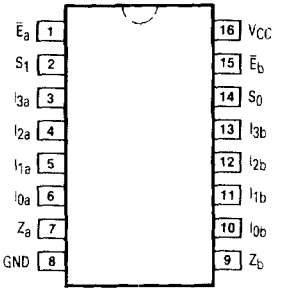
- Outputs Source/Sink 24 mA
- 'ACT153 Has TTL Compatible Inputs

N SUFFIX
CASE 648-08
PLASTIC

D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\bar{E}_a$	Side A Enable Input
$\bar{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

TRUTH TABLE

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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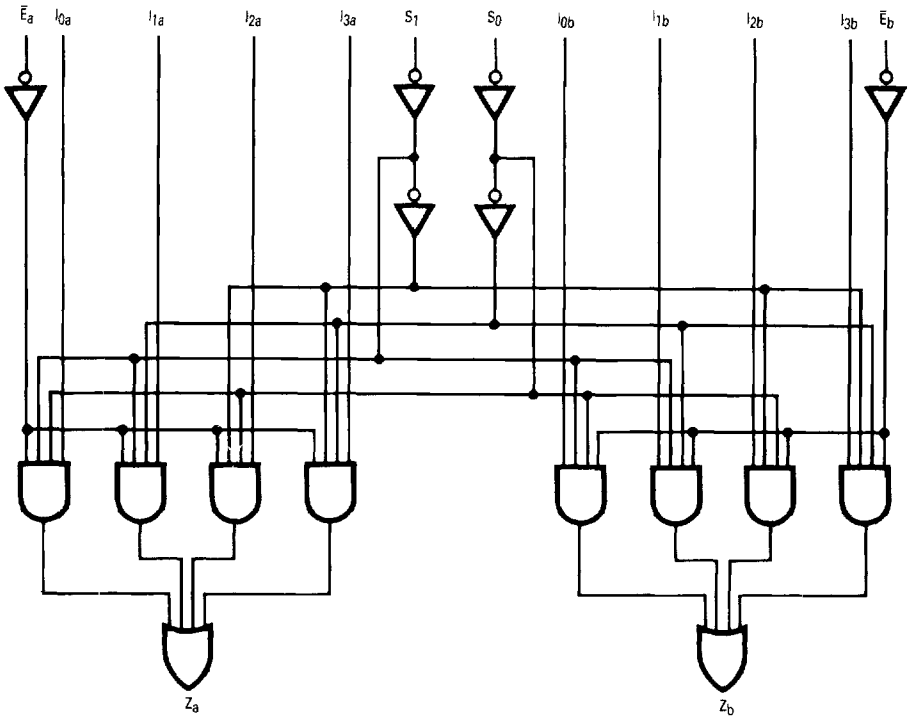
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC153/74ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The MC74AC153/74ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	9.5 6.5	15 11	1.0 1.0	17.5 12.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	8.5 6.5	14.5 11	1.0 1.0	16.5 12	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 5.0	1.0 1.0	8.0 5.5	13.5 9.5	1.0 1.0	16 11	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 5.0	1.0 1.0	7.0 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	14.5 10.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.5	1.0 1.0	13 10	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	13.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.5	10.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.0	9.5	1.0	11	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	9.5	1.0	11	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	9.5	1.0	11	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	65	pF	V_{CC} = 5.0 V