M37701E2-XXXSP,M37701E2AXXXSP

PROM VERSION of M37701M2-XXXSP,M37701M2AXXXSP

DESCRIPTION

The M37701E2-XXXSP and the M37701E2AXXXSP are single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in a 64-pin shrink plastic molded DIP. The features of these chips are similar to those of the M37701M2-XXXSP and the M37701M2AXXXSP except that this chip has a 16K-byte PROM built in.

These single-chip microcomputers have a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. These microcomputers are suitable for office, business and industrial equipment controller that require high-speed processing of large data.

Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

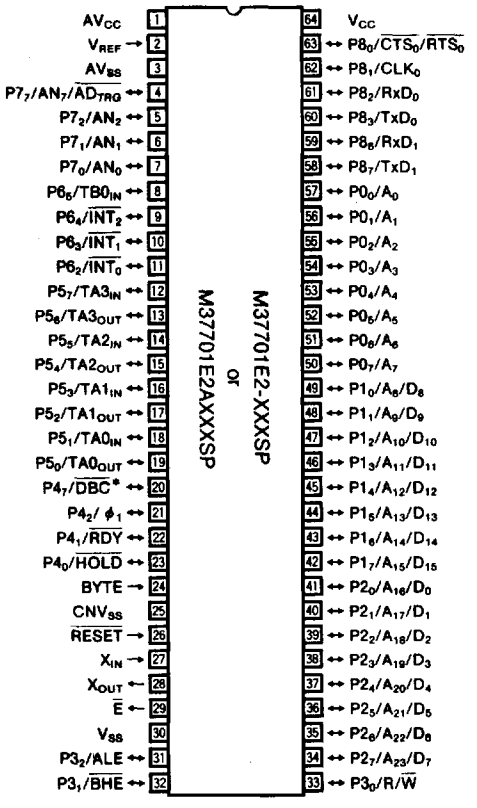
The differences between M37701E2-XXXSP and the M37701E2AXXXSP are the external clock input frequency as shown below. Therefore, the following descriptions will be for the M37701E2-XXXSP unless otherwise noted.

Type name	External clock input frequency
M37701E2-XXXSP	8 MHz
M37701E2AXXXSP	16MHz

DISTINCTIVE FEATURES

- Number of basic instructions 103
- Memory size PROM ..... 16K bytes
  RAM ..... 512 bytes
- Instruction execution time
  M37701E2-XXXSP
  (The fastest instruction at 8 MHz frequency) 500ns
  M37701E2AXXXSP
  (The fastest instruction at 16 MHz frequency) 250ns
- Single power supply ..... 5V±5%
- Low power dissipation (at 8 MHz frequency)
  ..... 30mW (Typ.)
- Interrupts ..... 19 types 7 levels
- Multiple function 16-bit timer ..... 5+3
- UART (may also be synchronous) 2
- 8-bit A-D converter ..... 4-channel inputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 53

PIN CONFIGURATION (TOP VIEW)



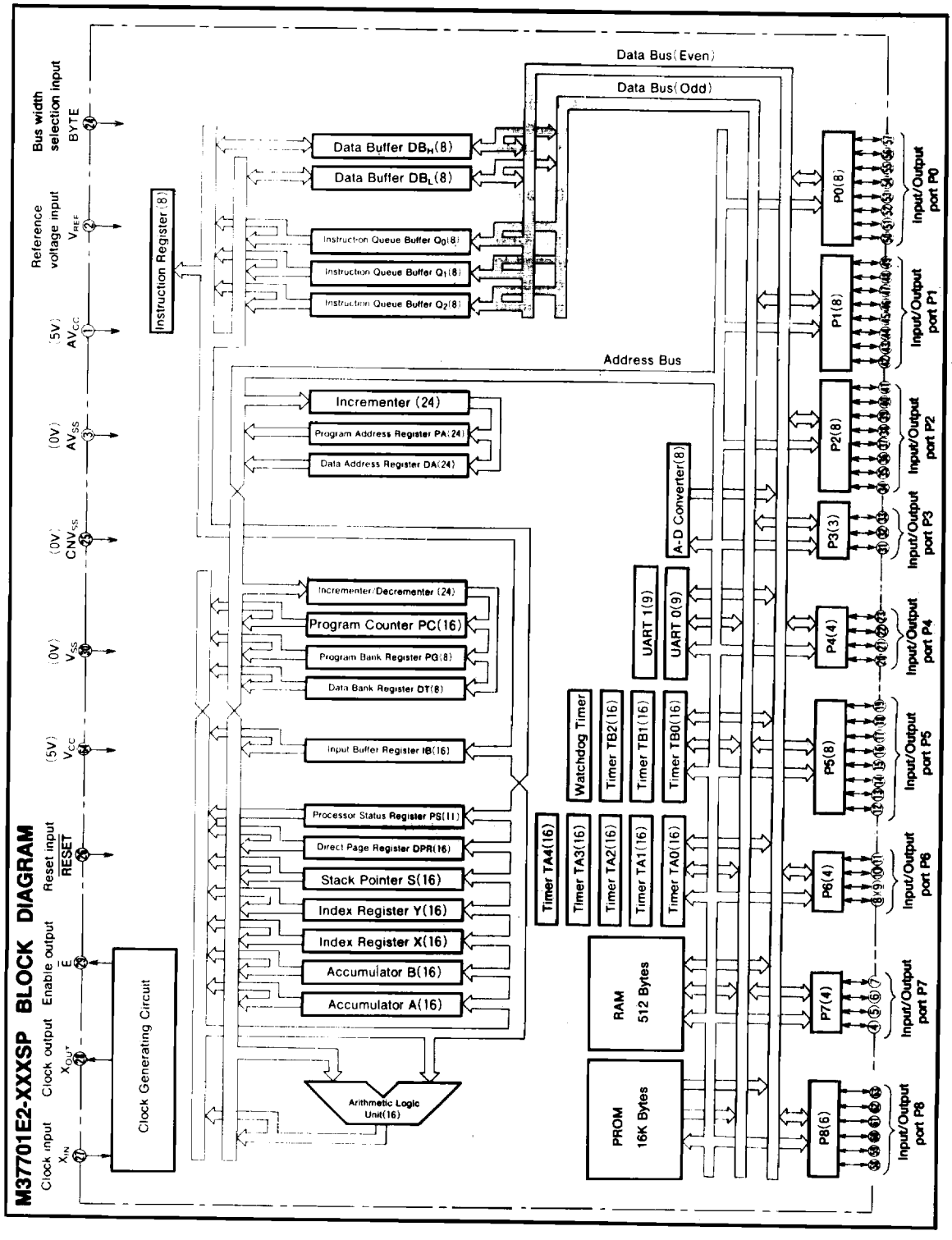
Outline 64P4B

*: Used in the evaluation chip mode only

APPLICATION

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

Control devices for industrial equipment such as ME, NC, communication, and measuring instruments



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FUNCTIONS OF M37701E2-XXXSP

Parameter		Functions
Number of basic instructions		103
Instruction execution time	M37701E2-XXXSP	500ns (the fastest instructions, at 8MHz frequency)
	M37701E2AXXXSP	250ns (the fastest instructions, at 16MHz frequency)
Memory size	PROM	16K bytes
	RAM	512 bytes
Input/Output ports	P0, P1, P2, P5	8-bit× 4
	P8	6-bit× 1
	P4, P6, P7	4-bit× 3
	P3	3-bit× 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit× 5 (4 input/Output functions)
	TB0, TB1, TB2	16-bit× 3 (1 input function)
Serial I/O		UART× 2 (One can be set clock synchronous serial I/O.)
A-D converter		8-bit× 1 (4 channels)
Watchdog timer		12-bit× 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0 ~ 7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		5 V±5 %
Power dissipation		30mW(at external 8 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16M bytes
Operating temperature range		−10~70℃
Device structure		CMOS high-performance silicon gate process
Package		64-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5 V± 5 % to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS} input	Input	This pin controls the processor mode. Connect to V_{SS} for single-chip mode.
$\overline{RESET}$	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV_{CC}, AV_{SS}	Analog supply input		Power supply for the A-D converter. Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS} externally.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0$~$P0_7$	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O directional register is available so that each pin can be programmed for input or output. These ports are in input mode when reset . Address(A_7~A_0)is output in memory expansion mode or microprocessor mode.
$P1_0$~$P1_7$	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D_{15}~D_8)is input or output when $\overline{E}$ output is "L" and an address (A_{15}~A_8) is output when $\overline{E}$ output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address(A_{15}~A_8)is output.
$P2_0$~$P2_7$	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data(D_7~D_0) is input or output when $\overline{E}$ output is "L" and an address(A_{23}~A_{16})is output when $\overline{E}$ output is "H".
$P3_0$~$P3_2$	I/O port P3	I/O	In single-chip mode , these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/$\overline{W}$, $\overline{BHE}$, and ALE signals are output.
$P4_0$~$P4_2$, $P4_7$	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$ and $P4_1$ become $\overline{HOLD}$ and $\overline{RDY}$ input pin respectively. Functions of other pins are the same as in single-chip mode. Port $P4_2$ can be programed for ϕ_1 output pin divided the clock to X_{IN} pin by 2.
$P5_0$~$P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2, and timer A3.
$P6_2$~$P6_5$	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as external interrupt input $\overline{INT_0}$, $\overline{INT_1}$, and $\overline{INT_2}$ pins, and input pins for timer B0.
$P7_0$~$P7_2$, $P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN_0~AN_2 and AN_7 input pins. $P7_7$ also has an A-D conversion trigger input function.
$P8_0$~$P8_3$, $P8_6$, $P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as R_XD, T_XD, CLK, $\overline{CTS}$/$\overline{RTS}$ pins for UART 0, and as RxD, TxD pins for UART 1.

PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5 V± 5 % to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
BYTE	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV_{CC}, AV_{SS}	A-D power supply		Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
$P0_0$~$P0_7$	Address input (A_0~A_7)	Input	Port P0 functions as the lower 8 bits address input (A_0~A_7).
$P1_0$~$P1_7$	Address input (A_8~A_{14})	Input	Port $P1_0$~$P1_6$ functions as the higher 7 bits address input (A_8~A_{14}). Connect $P1_7$ to V_{CC}.
$P2_0$~$P2_7$	Data I/O (D_0~D_7)	I/O	Port P2 functions as the 8 bits data bus (D_0~D_7).
$P3_0$~$P3_2$	Input port P3	Input	Connect to V_{SS}.
$P4_0$~$P4_2$, $P4_7$	Input port P4	Input	Connect to V_{SS}.
$P5_0$~$P5_7$	Control signal input	Input	$P5_1$ and $P5_2$ functions as $\overline{OE}$ and $\overline{CE}$ input pin. Connect $P5_0$, $P5_3$, $P5_4$ and $P5_5$ to V_{CC}. Connect $P5_6$ and $P5_7$ to V_{SS}.
$P6_2$~$P6_5$	Input port P6	Input	Connect to V_{SS}.
$P7_0$~$P7_2$, $P7_7$	Input port P7	Input	Connect to V_{SS}.
$P8_0$~$P8_3$, $P8_6$, $P8_7$	Input port P8	Input	Connect to V_{SS}.

EPROM MODE

The M37701E2-XXXSP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Fig. 1 gives the pin connections in the EPROM mode.

When in the EPROM mode, ports P0, P1, P2, $P5_1$, $P5_2$, CNV_{SS} and BYTE are used for the EPROM (equivalent to the M5M27C256K). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5M27C256K.

This chip does not have Device Identifer Mode, so that set the corresponding program algorithm. The program area should specify address 4000_{16}~$7FFF_{16}$ for the M37701E2-XXXSP.

Connect the clock which is either ceramic resonator or external clock to X_{IN} pin and X_{OUT} pin.

Table 1 Pin function in EPROM programming mode

	M37701E2-XXXSP	M5M27C256K
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}, BYTE	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$~$P1_6$	A_0~A_{14}
Data I/O	Port P2	D_0~D_7
$\overline{CE}$	$P5_2$	$\overline{CE}$
$\overline{OE}$	$P5_1$	$\overline{OE}$

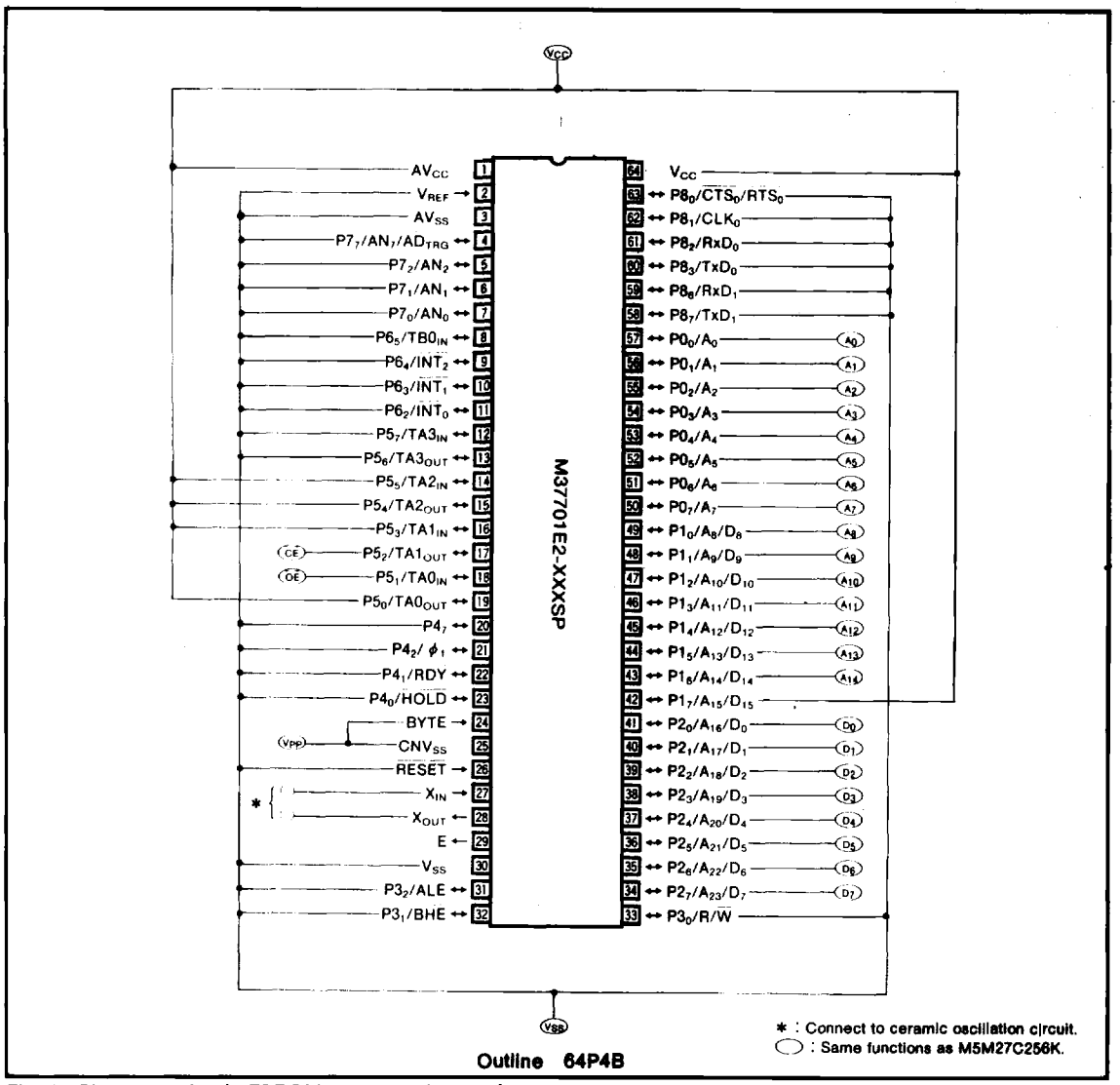


Fig. 1 Pin connection in EPROM programming mode

FUNCTION IN EPROM MODE

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data (A_0~A_{14}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{14}, and the data to be written is input to pins D_0 ~D_7. Set the $\overline{CE}$ pin to a "L" level to being writing.

FAST PROGRAMMING ALGORITHM

To program the M37701E2-XXXSP with fast programming algorithm, first set V_{CC}=6V, V_{PP}=12.5, and set the address to "0". Apply a 1ms write pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 1ms write pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (N) before the data can be read OK, and then write the data again, applying a further three times this number of pulses (3×N ms).

When this series of write operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been written, read with V_{CC}=V_{PP}=5V (or V_{CC}=V_{PP}=5.25V).

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	5 V	5 V	Output
Output Disable	V_{IL}	V_{IH}	5 V	5 V	Floating
	V_{IH}	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	12.5V	6 V	Input
Programming Verify	V_{IH}	V_{IL}	12.5V	6 V	Output
Program Disable	V_{IH}	V_{IH}	12.5V	6 V	Floating

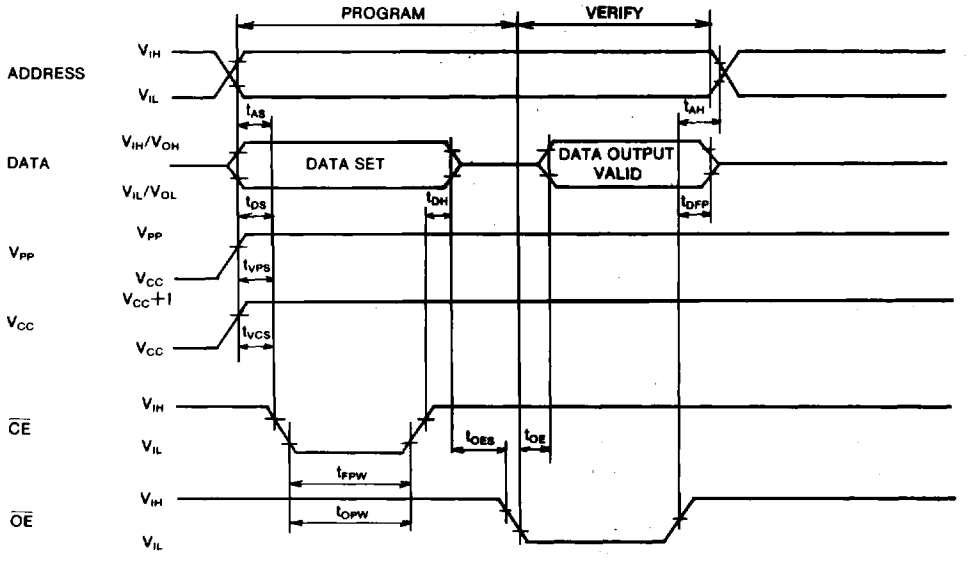
Note 1 : An X indicates either V_{IL} or V_{IH}.

Program operation

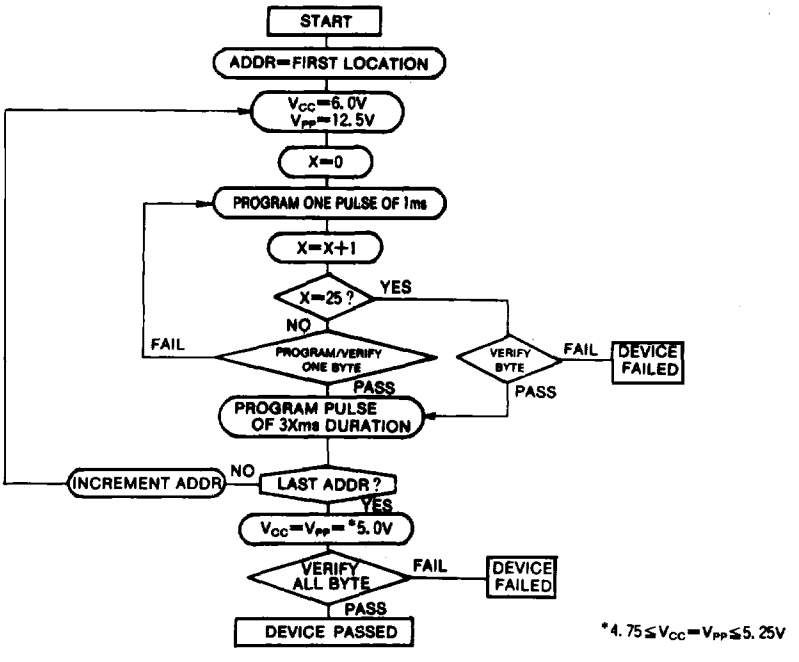
AC ELECTRICAL CHARACTERISTICS (T_a=25±5℃, V_{CC}=6V±0.25V, V_{PP}=12.5±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC waveforms



Fast programming algorithm flow chart



*4.75≤$V_{CC}=V_{PP}$≤5.25V

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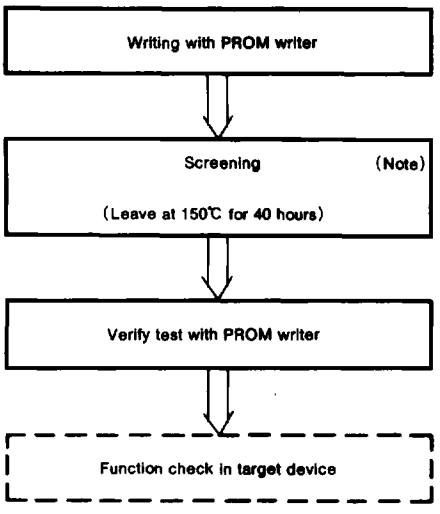
CAUTION: UNITS SHIPPED AS BLANKS

The programmable M37701E2SP and M37701E2ASP that are shipped in blank are also provided. For the M37701E2SP and M37701E2ASP, Mitsubishi Electric corp. does not perform PROM write test and screening following the assembly processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note :
Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

BASIC FUNCTION BLOCKS

Since these processors operate in exactly the same way as the M37701M2-XXXSP, refer to the section on the M37701M2-XXXSP.

ADDRESSING MODES

The M37701E2-XXXSP has 28 powerful addressing modes. Refer to the Series MELPS 7700 addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37701E2-XXXSP has 103 machine instructions. Refer to the Series MELPS 7700 machine instruction list for details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM .

(1) M37701E2-XXXSP writing to PROM order confirmation form
(2) Mark specification form for 64P4B
(3) ROM data (EPROM 3sets)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
AV_{CC}	Analog supply voltage		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}, BYTE		−0.3∼12	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_6$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$, V_{REF}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_6$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$, X_{OUT}, $\overline{E}$		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1. Input voltage for CNV_{SS} and BYTE pins is 13V in writing to PROM.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
AV_{CC}	Analog supply voltage		V_{CC}		V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	High-level input voltage $P0_0$∼$P0_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_5$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in single-chip mode)	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in memory expansion mode and microprocessor mode)	0.5V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage $P0_0$∼$P0_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_5$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in single-chip mode)	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16V_{CC}	V
$I_{OH(peak)}$	High-level peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_5$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$			−10	mA
$I_{OH(avg)}$	High-level average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_5$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$			−5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_5$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$			10	mA
$I_{OL(avg)}$	Low-level average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P4_0$∼$P4_2$, $P4_7$, $P5_0$∼$P5_7$, $P6_2$∼$P6_5$, $P7_0$∼$P7_2$, $P7_7$, $P8_0$∼$P8_3$, $P8_6$, $P8_7$			5	mA
$f_{(X_{IN})}$	External clock frequency input — M37701E2-XXXSP			8	MHz
	External clock frequency input — M37701E2AXXXSP			16	MHz

Note 1. Average output current is the average value of a100ms interval.
2. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3 and P8 must be 80mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3 and P8 must be 80mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6 and P7 must be 80mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6 and P7 must be 80mA or less.

M37701E2-XXXSP

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$	I_{OH}=−10mA	3			V
V_{OH}	High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$	I_{OH}=−400μA	4.7			V
V_{OH}	High-level output voltage $P3_2$	I_{OH}=−10mA	3.1			V
		I_{OH}=−400μA	4.8			
V_{OH}	High-level output voltage $\overline{E}$	I_{OH}=−10mA	3.4			V
		I_{OH}=−400μA	4.8			
V_{OL}	Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$	I_{OL}=10mA			2	V
V_{OL}	Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$	I_{OL}=2mA			0.45	V
V_{OL}	Low-level output voltage $P3_2$	I_{OL}=10mA			1.9	V
		I_{OL}=2mA			0.43	
V_{OL}	Low-level output voltage $\overline{E}$	I_{OL}=10mA			1.6	V
		I_{OL}=2mA			0.4	
V_{T+}−V_{T-}	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$~$TA3_{IN}$, $TB0_{IN}$, $\overline{INT_0}$~$\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, CLK_0		0.4		1	V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$		0.2		0.5	V
V_{T+}−V_{T-}	Hysteresis X_{IN}		0.1		0.3	V
I_{IH}	High-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5	μA
I_{IL}	Low-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			−5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset. f(X_{IN})=8MHz, square waveform		6	12	mA
		T_a=25℃ when clock is stopped.			1	μA
		T_a=70℃ when clock is stopped.			10	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time		28.5			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

TIMING REQUIREMENTS (V_{CC}=5V± 5 %, V_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

External clock input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C	External clock input cycle time		125			ns
$t_{W(H)}$	External clock input high-level pulse width		50			ns
$t_{W(L)}$	External clock input low-level pulse width		50			ns
t_r	External clock rise time				20	ns
t_f	External clock fall time				20	ns

Single-chip mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P0D-E)}$	Port P0 input setup time		200			ns
$t_{SU(P1D-E)}$	Port P1 input setup time		200			ns
$t_{SU(P2D-E)}$	Port P2 input setup time		200			ns
$t_{SU(P3D-E)}$	Port P3 input setup time		200			ns
$t_{SU(P4D-E)}$	Port P4 input setup time		200			ns
$t_{SU(P5D-E)}$	Port P5 input setup time		200			ns
$t_{SU(P6D-E)}$	Port P6 input setup time		200			ns
$t_{SU(P7D-E)}$	Port P7 input setup time		200			ns
$t_{SU(P8D-E)}$	Port P8 input setup time		200			ns
$t_{h(E-P0D)}$	Port P0 input hold time		0			ns
$t_{h(E-P1D)}$	Port P1 input hold time		0			ns
$t_{h(E-P2D)}$	Port P2 input hold time		0			ns
$t_{h(E-P3D)}$	Port P3 input hold time		0			ns
$t_{h(E-P4D)}$	Port P4 input hold time		0			ns
$t_{h(E-P5D)}$	Port P5 input hold time		0			ns
$t_{h(E-P6D)}$	Port P6 input hold time		0			ns
$t_{h(E-P7D)}$	Port P7 input hold time		0			ns
$t_{h(E-P8D)}$	Port P8 input hold time		0			ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P1D-E)}$	Port P1 input setup time		60			ns
$t_{SU(P2D-E)}$	Port P2 input setup time		60			ns
$t_{SU(RDY-\phi_1)}$	$\overline{RDY}$ input setup time		70			ns
$t_{h(E-P1D)}$	Port P1 input hold time		0			ns
$t_{h(E-P2D)}$	Port P2 input hold time		0			ns
$t_{h(\phi 1-RDY)}$	$\overline{RDY}$ input hold time		0			ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time		250			ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		125			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		125			ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time		1000			ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		500			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		500			ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time		500			ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		250			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		250			ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		250			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		250			ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(UP)}$	TAi_{OUT} input cycle time		1000			ns
$t_{W(UPH)}$	TAi_{OUT} input high-level pulse width		500			ns
$t_{W(UPL)}$	TAi_{OUT} input low-level pulse width		500			ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time		500			ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width		250			ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width		250			ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time		1000			ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width		500			ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width		500			ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time		1000			ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width		500			ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width		500			ns

A-D trigger input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)		2000			ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width		250			ns

Serial I/O

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(CK)}$	CLKi input cycle time		500			ns
$t_{W(CKH)}$	CLKi input high-level pulse width		250			ns
$t_{W(CKL)}$	CLKi input low-level pulse width		250			ns
$t_{d(C-Q)}$	TxDi output delay time				150	ns
$t_{h(C-Q)}$	TxDi hold time		30			ns
$t_{SU(D-C)}$	RxDi input setup time		60			ns
$t_{h(C-D)}$	RxDi input hold time		90			ns

External interrupt $\overline{INTi}$ input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high-level pulse width		250			ns
$t_{W(INL)}$	$\overline{INTi}$ input low-level pulse width		250			ns

SWITCHING CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=8MHz, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Figure 2			200	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time				200	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time				200	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time				200	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time				200	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Figure 2	100			ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")				120	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")				40	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		100			ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				120	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time				40	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		100			ns
$t_{d(ALE-E)}$	ALE output delay time		4			ns
$t_{W(ALE)}$	ALE pulse width		100			ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		100			ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		100			ns
$t_{d(E-\phi 1)}$	ϕ_1 output delay time		0		30	ns
$t_{h(E-P0A)}$	Port P0 address hold time		50			ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9			ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		50			ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		50			ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		50			ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9			ns
$t_{h(E-P2Q)}$	Port P2 data hold time		50			ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		50			ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		20			ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		20			ns
$t_{W(EL)}$	$\overline{E}$ pulse width		220			ns

Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Figure 2	350			ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")				120	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")				40	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		350			ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				120	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time				40	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		350			ns
$t_{d(ALE-E)}$	ALE output delay time		4			ns
$t_{W(ALE)}$	ALE pulse width		350			ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		350			ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		350			ns
$t_{d(E-\phi 1)}$	ϕ_1 output delay time		0		30	ns
$t_{h(E-P0A)}$	Port P0 address hold time		50			ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9			ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		50			ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		50			ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		50			ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9			ns
$t_{h(E-P2Q)}$	Port P2 data hold time		50			ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		50			ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		20			ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		20			ns
$t_{W(EL)}$	$\overline{E}$ pulse width		470			ns

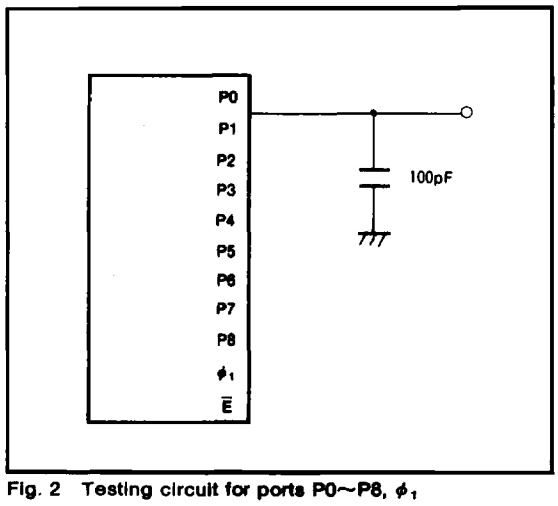


Fig. 2 Testing circuit for ports P0~P8, ϕ_1

M37701E2AXXXSP

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=16MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$	I_{OH}=−10mA	3			V
V_{OH}	High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$	I_{OH}=−400μA	4.7			V
V_{OH}	High-level output voltage $P3_2$	I_{OH}=−10mA	3.1			V
		I_{OH}=−400μA	4.8			
V_{OH}	High-level output voltage $\overline{E}$	I_{OH}=−10mA	3.4			V
		I_{OH}=−400μA	4.8			
V_{OL}	Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$	I_{OL}=10mA			2	V
V_{OL}	Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$	I_{OL}=2mA			0.45	V
V_{OL}	Low-level output voltage $P3_2$	I_{OL}=10mA			1.9	V
		I_{OL}=2mA			0.43	
V_{OL}	Low-level output voltage $\overline{E}$	I_{OL}=10mA			1.6	V
		I_{OL}=2mA			0.4	
$V_{T+}-V_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$~$TA3_{IN}$, $TB0_{IN}$, $\overline{INT_0}$~$\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, CLK_0		0.4		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$		0.2		0.5	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.3	V
I_{IH}	High-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_5$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5	μA
I_{IL}	Low-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P4_0$~$P4_2$, $P4_7$, $P5_0$~$P5_7$, $P6_2$~$P6_6$, $P7_0$~$P7_2$, $P7_7$, $P8_0$~$P8_3$, $P8_6$, $P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			−5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset. f(X_{IN})=16MHz, square waveform		12	24	mA
		T_a=25℃ when clock is stopped.			1	μA
		T_a=70℃ when clock is stopped.			10	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=16MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time		14.25			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

TIMING REQUIREMENTS (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=16MHz, unless otherwise noted)

External clock input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C	External clock input cycle time		62			ns
$t_{W(H)}$	External clock input high-level pulse width		25			ns
$t_{W(L)}$	External clock input low-level pulse width		25			ns
t_r	External clock rise time				10	ns
t_f	External clock fall time				10	ns

Single-chip mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P0D-E)}$	Port P0 input setup time		100			ns
$t_{SU(P1D-E)}$	Port P1 input setup time		100			ns
$t_{SU(P2D-E)}$	Port P2 input setup time		100			ns
$t_{SU(P3D-E)}$	Port P3 input setup time		100			ns
$t_{SU(P4D-E)}$	Port P4 input setup time		100			ns
$t_{SU(P5D-E)}$	Port P5 input setup time		100			ns
$t_{SU(P6D-E)}$	Port P6 input setup time		100			ns
$t_{SU(P7D-E)}$	Port P7 input setup time		100			ns
$t_{SU(P8D-E)}$	Port P8 input setup time		100			ns
$t_{h(E-P0D)}$	Port P0 input hold time		0			ns
$t_{h(E-P1D)}$	Port P1 input hold time		0			ns
$t_{h(E-P2D)}$	Port P2 input hold time		0			ns
$t_{h(E-P3D)}$	Port P3 input hold time		0			ns
$t_{h(E-P4D)}$	Port P4 input hold time		0			ns
$t_{h(E-P5D)}$	Port P5 input hold time		0			ns
$t_{h(E-P6D)}$	Port P6 input hold time		0			ns
$t_{h(E-P7D)}$	Port P7 input hold time		0			ns
$t_{h(E-P8D)}$	Port P8 input hold time		0			ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P1D-E)}$	Port P1 input setup time		45			ns
$t_{SU(P2D-E)}$	Port P2 input setup time		45			ns
$t_{SU(\overline{RDY}-\phi 1)}$	$\overline{RDY}$ input setup time		60			ns
$t_{h(E-P1D)}$	Port P1 input hold time		0			ns
$t_{h(E-P2D)}$	Port P2 input hold time		0			ns
$t_{h(\phi 1-\overline{RDY})}$	$\overline{RDY}$ input hold time		0			ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time		125			ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		62			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		62			ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time		500			ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		250			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		250			ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time		250			ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		125			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		125			ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width		125			ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width		125			ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(UP)}$	TAi_{OUT} input cycle time		500			ns
$t_{W(UPH)}$	TAi_{OUT} input high-level pulse width		250			ns
$t_{W(UPL)}$	TAi_{OUT} input low-level pulse width		250			ns

Timer B input (Cont input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TBI_{IN} input cycle time		250			ns
$t_{W(TBH)}$	TBI_{IN} input high-level pulse width		125			ns
$t_{W(TBL)}$	TBI_{IN} input low-level pulse width		125			ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TBI_{IN} input cycle time		500			ns
$t_{W(TBH)}$	TBI_{IN} input high-level pulse width		250			ns
$t_{W(TBL)}$	TBI_{IN} input low-level pulse width		250			ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TBI_{IN} input cycle time		500			ns
$t_{W(TBH)}$	TBI_{IN} input high-level pulse width		250			ns
$t_{W(TBL)}$	TBI_{IN} input low-level pulse width		250			ns

A-D trigger input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)		1000			ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width		125			ns

Serial I/O

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(CK)}$	CLKi input cycle time		250			ns
$t_{W(CKH)}$	CLKi input high-level pulse width		125			ns
$t_{W(CKL)}$	CLKi input low-level pulse width		125			ns
$t_{d(C-Q)}$	TxDi output delay time				90	ns
$t_{h(C-Q)}$	TxDi hold time		30			ns
$t_{su(D-C)}$	RxDi input setup time		30			ns
$t_{h(C-D)}$	RxDi input hold time		90			ns

External interrupt $\overline{INTi}$ input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high-level pulse width		250			ns
$t_{W(INL)}$	$\overline{INTi}$ input low-level pulse width		250			ns

SWITCHING CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=16MHz, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Figure 2			100	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time				100	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				100	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time				100	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time				100	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time				100	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time				100	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time				100	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time				100	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

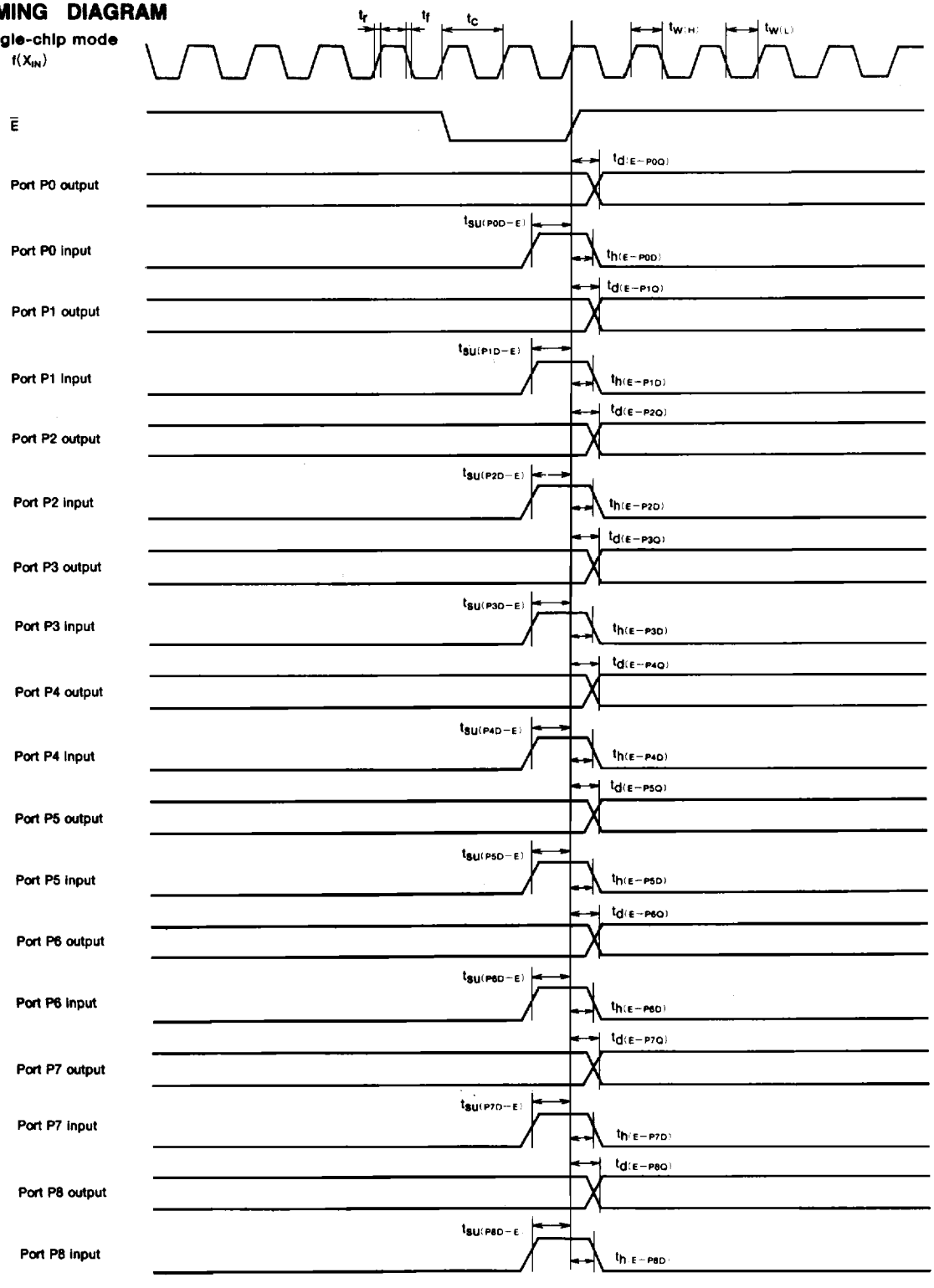
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Figure 2	30			ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")				80	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")				40	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		30			ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				80	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time				40	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		30			ns
$t_{d(ALE-E)}$	ALE output delay time		4			ns
$t_{W(ALE)}$	ALE pulse width		40			ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		30			ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		30			ns
$t_{d(E-\phi 1)}$	ϕ_1 output delay time		0		20	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25			ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9			ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25			ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25			ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25			ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9			ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25			ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		25			ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		20			ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		20			ns
$t_{W(EL)}$	$\overline{E}$ pulse width		95			ns

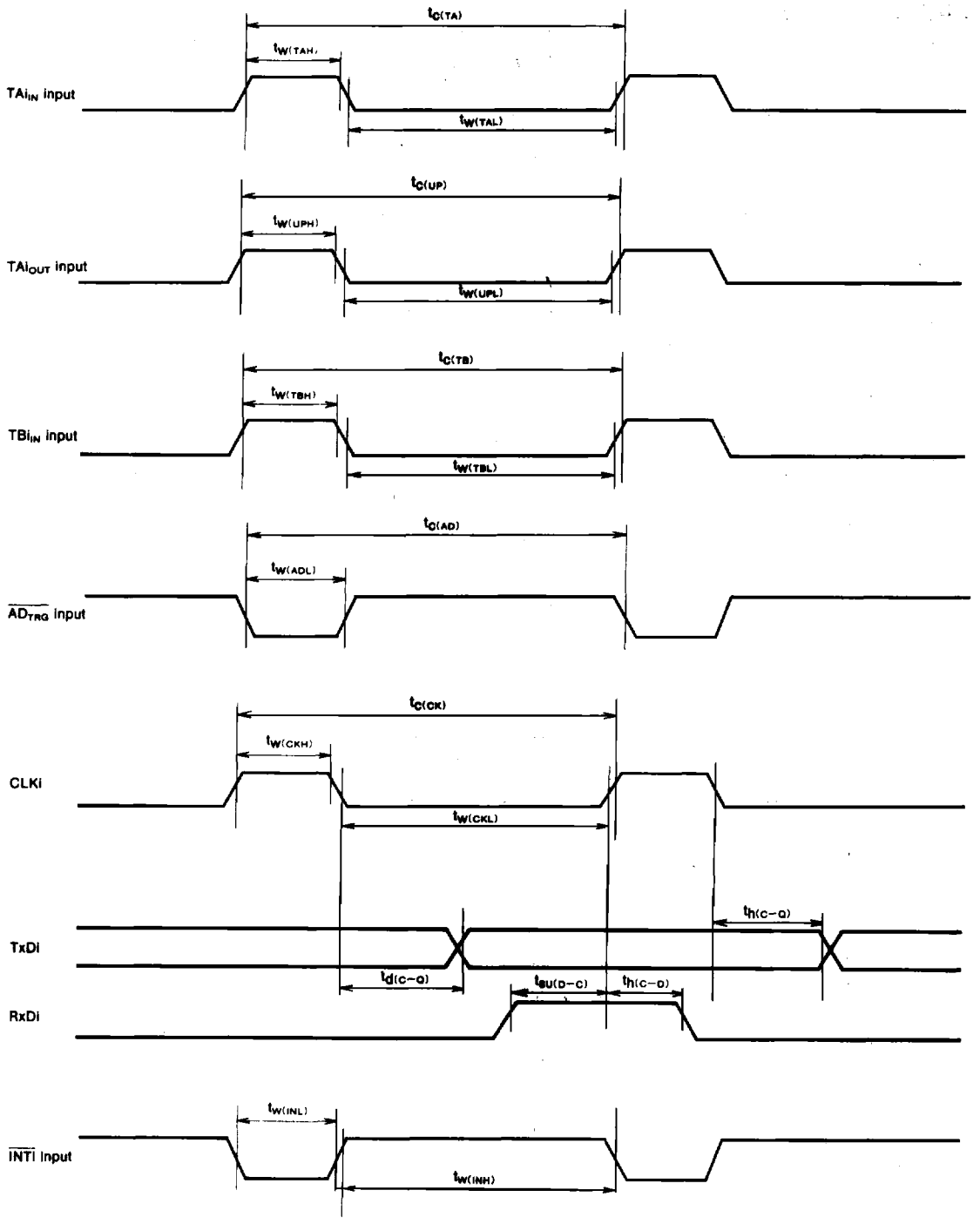
Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Figure 2	155			ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")				80	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")				40	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		155			ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				80	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time				40	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		155			ns
$t_{d(ALE-E)}$	ALE output delay time		4			ns
$t_{W(ALE)}$	ALE pulse width		165			ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		155			ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		155			ns
$t_{d(E-\phi 1)}$	ϕ_1 output delay time		0		20	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25			ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9			ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25			ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25			ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25			ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9			ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25			ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		25			ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		20			ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		20			ns
$t_{W(EL)}$	$\overline{E}$ pulse width		220			ns

TIMING DIAGRAM

Single-chip mode





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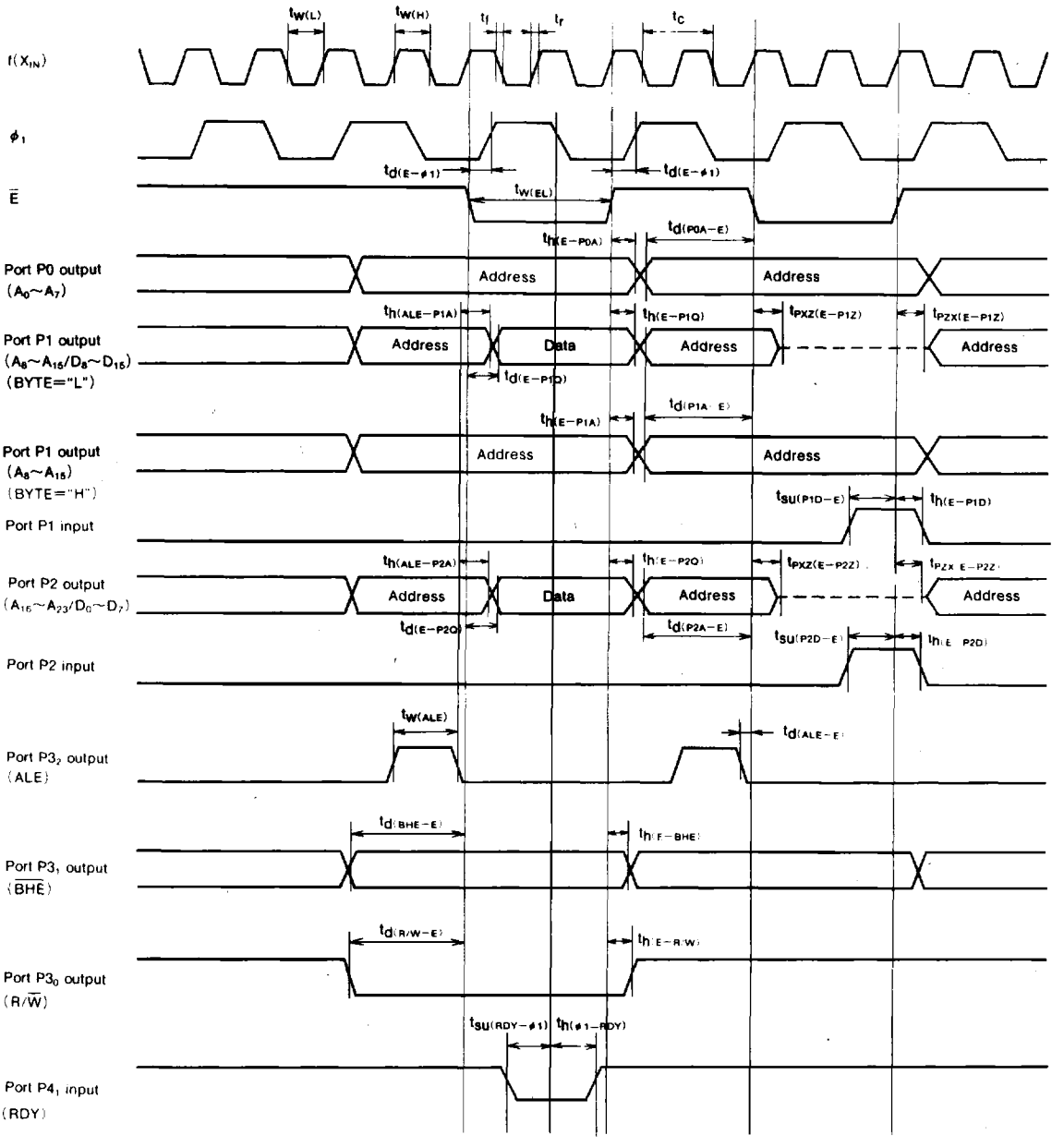
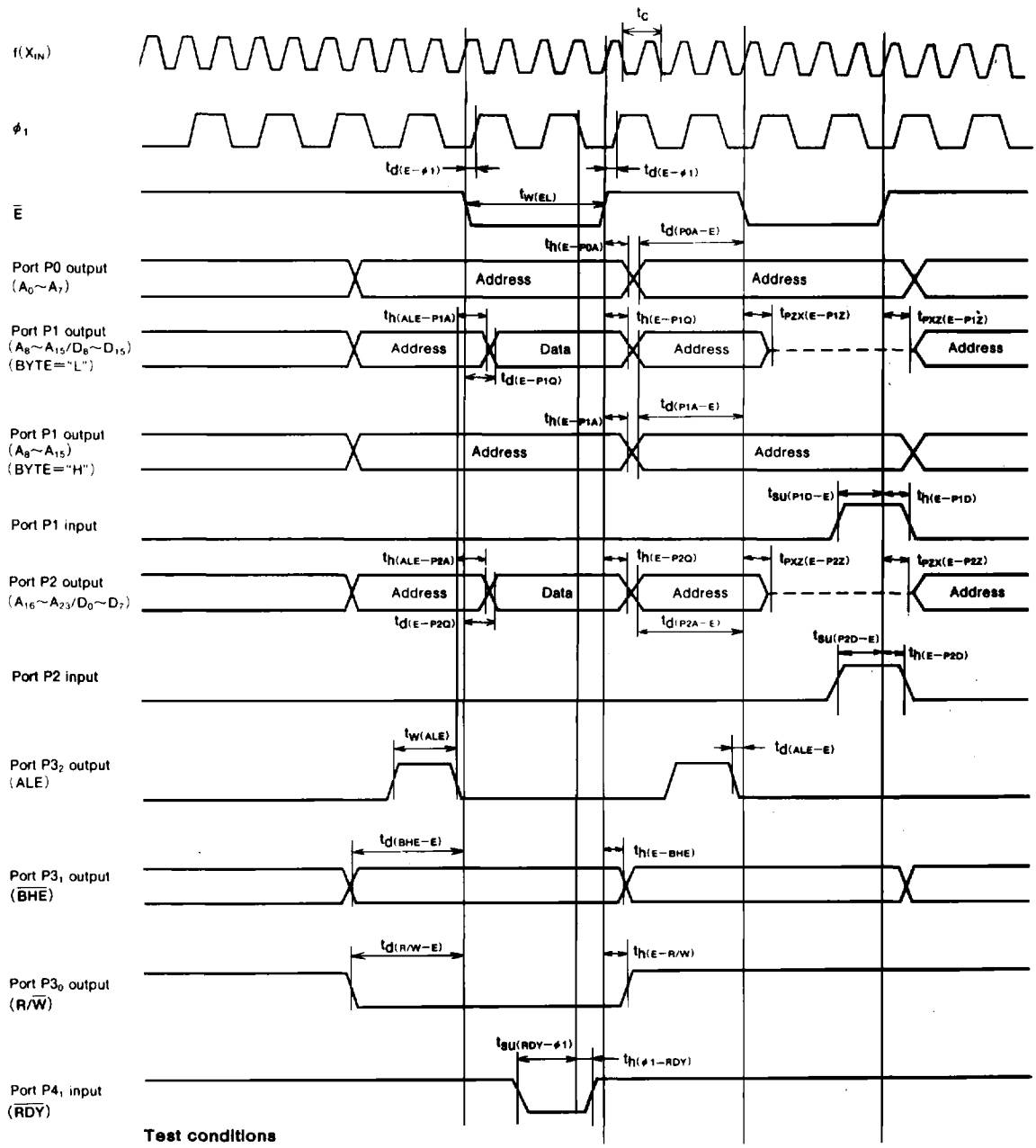
Memory expansion mode and microprocessor mode (When wait bit="1")



Test conditions

- V_{CC}= 5 V± 5 %
- Output timing voltage : V_{OL}=0.8V, V_{OH}=2.0V
- Ports P1,P2 input : V_{IL}=0.8V, V_{IH}=2.5V
- Port $P4_1$ input : V_{IL}=1.0V, V_{IH}=4.0V

Memory expansion mode and microprocessor mode(when wait bit="0", and external memory area is accessed)



Test conditions

- V_{CC}= 5 V± 5 %
- Output timing voltage : V_{OL}=0.8V, V_{OH}=2.0V
- Ports P1,P2 input : V_{IL}=0.8V, V_{IH}=2.5V
- Port $P4_1$ input : V_{IL}=1.0V, V_{IH}=4.0V