

# SANYO Semiconductors DATA SHEET

## Monolithic Linear IC

## **LA5677M** — Dual Switching Regulator Control IC

#### Overview

The LA5677M supports single-input control of the outputs of two converters of arbitrary types, including step up, step down and inverting. Since the LA5677M supports low voltage (3.6 to 18V) and high frequency (1 to 500kHz) operation, it is ideal for use in power supplies in battery powered portable equipment.

#### **Functions**

- Operates at low voltages (3.6 to 18V).
- Can be used with high frequency oscillators (1 to 500kHz).
- Built-in low input malfunction prevention circuit.
- Built-in timer-latch short circuit protection circuit

#### **Specifications**

#### **Maximum Ratings** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		20	V
Error amplifier input voltage	VI		20	V
Collector output voltage	V <sub>O</sub>		20	V
Collector output current	I <sub>O</sub>		21	mA
Allowable power dissipation	Pd max		330	mW
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

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## **LA5677M**

## Operating Conditions at $Ta = 25^{\circ}C$

Danamatan	Symbol	Conditions	Ratings			11.3
Parameter			min	typ	max	Unit
Recommended supply voltage	VCC		3.6		18	V
Error amplifier input voltage	VI		1.05		1.45	V
Collector output voltage	V <sub>O</sub>		-0.3		+18	V
Collector output current	IO				20	mA
Feedback pin current	I <sub>FT</sub>				45	μΑ
Feedback resistance	R <sub>NF</sub>		100			kΩ
Timing capacitance	C <sub>T</sub>		150		15000	pF
Timing resistance	R <sub>T</sub>		5.1		100	kΩ
Oscillator frequency	fosc		1		500	kHz

#### **Electrical Characteristics** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
Faiametei	Symbol	Conditions	min	typ	max	Oill
Reference voltage block						
Output voltage	Vref	I <sub>OR</sub> = 1mA	2.40	2.50	2.60	V
Line regulation	V <sub>line</sub>	V <sub>CC</sub> = 3.6 to 18V		2	10	mV
Load regulation	V <sub>load</sub>	I <sub>OR</sub> = 0.1 to 1mA		1	7.5	mV
Output voltage temperature variation				±0.2		%
Short circuit output current	losc	Vref = 0V	3	10	30	mA
Low input malfunction prevent	ion block					
High level threshold voltage	V <sub>tH</sub>	I <sub>OR</sub> = 0.1mA		2.70		V
Low level threshold Voltage	V <sub>tL</sub>	I <sub>OR</sub> = 0.1mA		2.58		V
Hysteresis	Vhys	I <sub>OR</sub> = 0.1mA	80	120		mV
Reset voltage	Vr	I <sub>OR</sub> = 0.1mA	1.5	1.9		V
Protection circuit block	-			•		
Input threshold voltage	Vtpc		1.02	1.16	1.30	V
Input standby voltage	Vstby	No pull-up		0.78		V
Input latch voltage	VI	No pull-up		0.74		V
Input source current	Ibpc		12	18	27	μА
Comparator threshold voltage	Vtc			1.2		V
Oscillator block	1			W.		
Oscillator frequency	fosc	$C_T = 330 pF, R_T = 10 k\Omega$		200		kHz
fOSC standard deviation	ΔfA	All values agree		10		%
Frequency variation 1 (V <sub>CC</sub> )	Δfγ			1		%
Frequency variation 2 (Ta)	Δft			±0.4		%
Idle period adjustment circuit I	olock			W.		
Input bias current	lbdt				1	μΑ
Latch mode source current	ldt			230		μΑ
Latch input voltage	Vdt	Idt = 40μA	2.3			V
Input threshold voltage	Vt0	With a duty cycle of 0%		2.05	2.25	V
	Vt100	f <sub>OSC</sub> = 10kHz, With a duty cycle of 100%	1.20	1.45		V
Error amplifier block	1			W.		
Input offset voltage	V <sub>IO</sub>	With V (pins 5, 12) = 1.25V	-6		+6	mV
Input offset current	I <sub>IO</sub>	With V (pins 5, 12) = 1.25V	-100		+100	nA
Input bias current	IB	With V (pins 5, 12) = 1.25V		160	500	nA
Common mode input voltage range	VICR	V <sub>CC</sub> = 3.6 to 18V	1.05		1.45	V
Open loop gain	A <sub>V</sub>	R <sub>NF</sub> = 200kΩ		80		dB
Unity gain bandwidth	G <sub>B</sub>			1.5		MHz
Common mode rejection ratio	CMMR			80		dB

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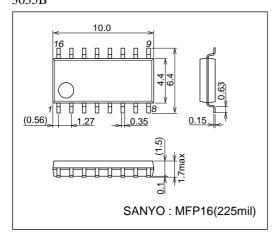
## LA5677M

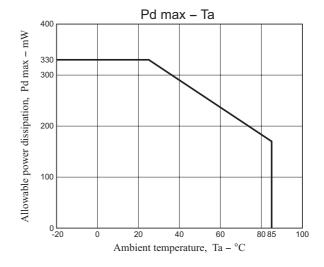
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Development	Symbol	Conditions	Ratings			Unit	
Parameter			min	typ	max	Unit	
Maximum output voltage amplitude (1)	V <sub>O</sub> +m		Vref-0.1			V	
Maximum output voltage amplitude (2)	voltage V <sub>O</sub> -m				1.0	>	
Output sink current (pins 5, 12)	$I_{O}^{+}m$ $V_{ID} = -0.1V, V_{O} = 1.25V$ 1.6		1.6		mA		
Output source current (pins 5, 12)	$I_{O}^{-m}$ $V_{ID} = 0.1V, V_{O} = 1.25V$		-70		μΑ		
Output block							
Output leakage current	I <sub>leak</sub>	V <sub>O</sub> = 18V			10	μА	
Output saturation voltage	Vsat	I <sub>O</sub> = 10mA		1.0	2	V	
Short circuit output current	los	V <sub>O</sub> = 6V	60		mA		
PWM comparator block	PWM comparator block						
Input threshold voltage	Vt0	With a duty cycle of 0%		2.05	2.25	V	
	Vt100	f <sub>OSC</sub> = 10kHz, With a duty cycle of 100%	1.20	1.45		V	
Input sink current (pins 5, 12)	I <sub>IN</sub> +m	With V (pins 5, 12) = 1.25V		1.6		mA	
Input source current (pins 5, 12)	I <sub>IN</sub> -m	With V (pins 5, 12) = 1.25V		-70		μΑ	
Whole device							
Standby current	I <sub>CC</sub> 1	Output off state		1.6	2.2	mA	
Average supply current	I <sub>CC</sub> 2	$R_T = 10k\Omega$		1.9	2.6	mA	

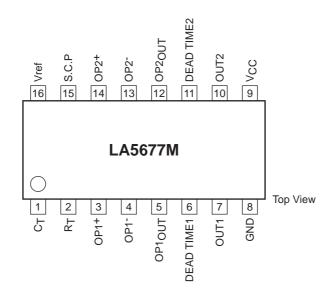
## **Package Dimensions**

unit : mm (typ) 3035B





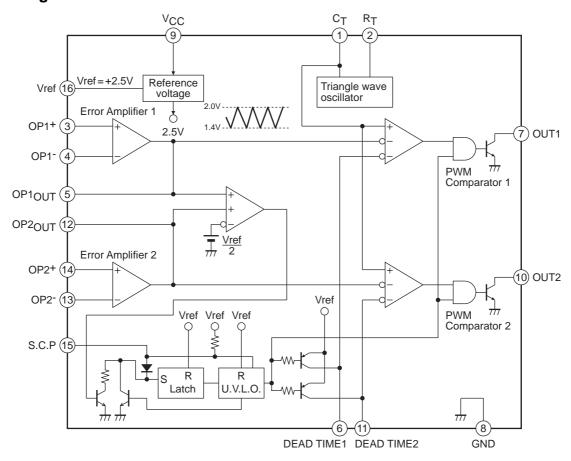
## **Pin Assignment**



#### **Pin Function**

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	C <sub>T</sub>	Triangle wave oscillator capacitor connection	9	VCC	Power supply input
2	RT	Triangle wave oscillator resistor connection	10	OUT2	Output 2
3	OP1 <sup>+</sup>	Error amplifier 1 + input	11	DEAD TIME2	Dead time 2 control
4	OP1 <sup>-</sup>	Error amplifier 1 - input	12	OP2 <sub>OUT</sub>	Error amplifier 2 output
5	OP1 <sub>OUT</sub>	Error amplifier 1 output	13	OP2 <sup>-</sup>	Error amplifier 1 - input
6	DEAD TIME1	Dead time 1 control	14	OP2 <sup>+</sup>	Error amplifier 1 + input
7	OUT1	Output 1	15	S.C.P	Short circuit protection circuit connection
8	GBD	Ground connection	16	Vref	Reference voltage (2.5V)

## **Block Diagram**



#### **Operation Overview**

#### 1. Reference Voltage Block

The reference voltage block uses a 2.5V reference voltage. This voltage is made available to external circuits from pin 16, and at the same time is used as the reference power supply by internal circuits.

#### 2. Low Input Malfunction Prevention Circuit Block

The low input malfunction prevention circuit prevents incorrect operation when the power supply is brought up or during brief voltage drops. After power is applied and the reference voltage reaches Vbe, the output transistors are held off until the power supply voltage becomes 2.72V (typical). The dead time control pin voltage is held at the high level (Vref) and the short circuit protection pin is held low (the initial state). Since this circuit has a hysteresis of 120mV (typical) chattering due to power supply ripple can be prevented to a certain extent.

#### 3. Timer-Latch Short Circuit Protection Circuit

During output overload, the timer-latch short circuit protection circuit's short circuit protection comparator turns off Q86 when the error amplifier inputs a low level signal (a voltage less than Vref/2) to one or both of the short circuit protection comparator's two non-inverting inputs. At this time the pin 15 voltage increases from about 0.75V (steady state) towards Vref as the external capacitor is charged from Vref through resistor R41 ( $80k\Omega$ ). When the capacitor is charged to about 1.2V, the protection latch is set, the output transistors are turned off, and the idle time becomes 100%. This also turns on Q97 which resets the protection enable state. The latch circuit reset voltage is under 1.9V (typical).

```
VpE1 = Vref \{1 - exp (-t1/R41 \times CpT)\}
VpE2 = Vref \{1 - exp (-t2/R41 \times CpT)\}
0.75 = 2.5 \{1 - exp (-t1/80k \times CpT)\}
1.20 = 2.5 \{1 - exp (-t2/80k \times CpT)\}
t1 = 28.56k \times CpT
t2 = 52.31k \times CPT
tpT = t2 - t1 = 23.75k \times CpT
CPT = 42.1 \times tpT [\mu F]
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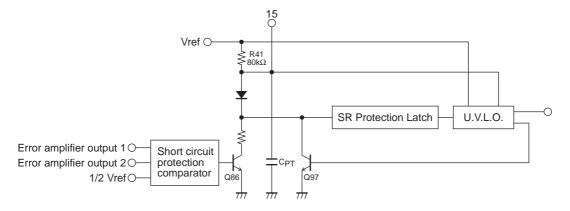


Figure 1 Timer-Latch Short Circuit Protection Circuit

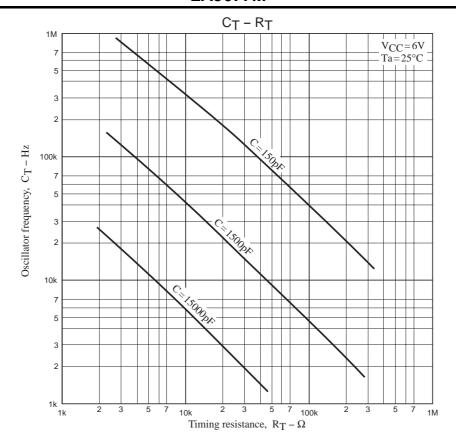


Figure 2 Timing Resistance/Oscillator Frequency Characteristics

#### 4. Triangle Wave Oscillator Block

The triangle wave oscillator generates an essentially symmetric triangle wave using a timing capacitor and resistor attached to the  $C_T$  pin (pin 1) and the  $R_T$  pin (pin 2), respectively. The voltage amplitude is between 1.4 and 2.0V with pin 2 stabilized at 1V. The oscillator frequency is determined by the external capacitor and resistor.

#### 5. Idle Period Adjustment Circuit Block

The idle period adjustment circuit consists of PWM comparators 1 and 2, each of which has one non-inverting and two inverting inputs. The output pulse width (on time) is controlled according to the input voltage. Pins 6 and 11 are dead time control pins, and are used to limit the maximum value of the pulse width. A pin voltage of 2.05V (Typical) or over results in the output being off for the whole period, and a pin voltage of 1.45V (Typical) or lower results in the output being on for the whole period.

#### 6. Error Amplifier Block

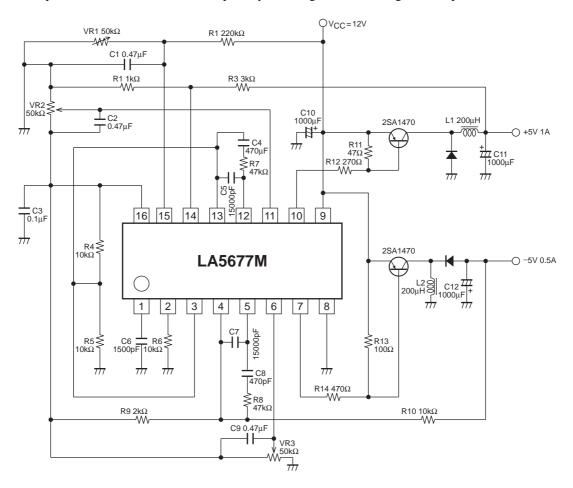
Error amplifiers 1 and 2 are amplifiers for detecting the output voltages, i.e., the LA5677M application system output voltages. Since the common mode input voltage range is 1.05 to 1.45V, we recommend setting their input voltages to Vref/2. Pins 5 and 12 are the output pins, and the gain is set and the frequency characteristics adjusted with a resistor and a capacitor connected between the outputs and the non-inverting inputs of each amplifier. The outputs are also connected to the short circuit protection circuit detection circuit.

#### 7. Output Block

The outputs are single end open collector outputs with an NPN Darlington pair structure.

#### **Application Circuit Example**

+5V, 1A step-down converter and -5V, 0.5A polarity inverting converter using a 12V input.



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