



Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT 7132SA/LA
IDT 7142SA/LA

FEATURES:

- High-speed access
 - Military: 25/30/35/45/55/70/90/100/120ns (max.)
 - Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
 - IDT7132/42SA
 - Active: 325mW (typ.)
 - Standby: 5mW (typ.)
 - IDT7132/42LA
 - Active: 325mW (typ.)
 - Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- BUSY output flag on IDT7132; BUSY input on IDT7142
- Battery backup operation -2V data retention
- TTL-compatible, single 5v ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD, Class B
- Standard Military Drawing # 5962-87002

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

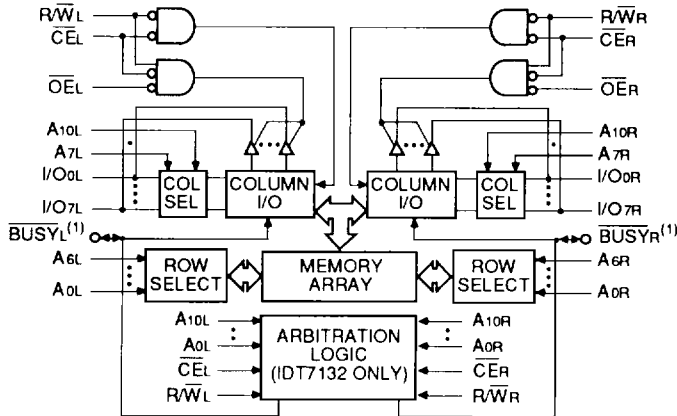
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by \overline{CE} permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200μW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and a 48-lead flatpacks.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2692 drw 01

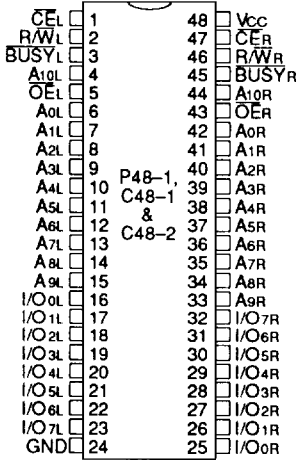
NOTE:

1. IDT7132 (MASTER): \overline{BUSY} is open output and requires pullup resistor.
IDT7142 (SLAVE): \overline{BUSY} is input.
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

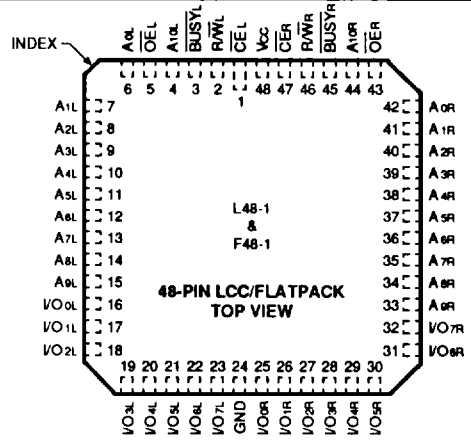
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PIN CONFIGURATIONS

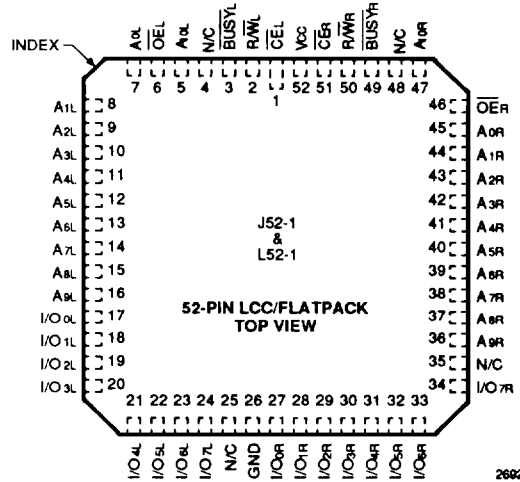


2692 drw 02

DIP
TOP VIEW



2692 drw 03



2692 drw 04

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:

2692 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED
DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

2692 tbl 02

- V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING
TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2692 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	IDT7132SA IDT7142SA		IDT7132LA IDT7142LA		Unit
			Min.	Max.	Max.	Max.	
I _{LI}	Input Leakage Current	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	—	5	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	—	5	μA
V _{OL}	Output Low Voltage (I/O0-I/O7)	I _{OL} = 4mA	—	0.4	—	0.4	V
V _{OL}	Open Drain Output Low Voltage (BUSY)	I _{OL} = 16mA	—	0.5	—	0.5	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2692 b1 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽¹⁾ ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	Version	7132 x 20 ^(2,6) 7142 x 20 ^(2,6)		7132 x 25 ⁽⁶⁾ 7142 x 25 ⁽⁶⁾		7132 x 30 ⁽⁶⁾ 7142 x 30 ⁽⁶⁾		7132 x 35 ⁽⁷⁾ 7142 x 35 ⁽⁷⁾		Unit	
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = f_{MAX}^{(4)}$	Mil. SA LA	—	—	75	300	75	290	75	280	75	230
			Com'l. SA LA	75	260	75	250	75	240	75	195	75	190
				75	190	75	180	75	170	75	155	75	145
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$ $f = f_{MAX}^{(4)}$	Mil. SA LA	—	—	25	75	25	75	25	75	25	65
			Com'l. SA LA	25	65	25	65	25	65	25	65	25	65
				25	45	25	45	25	45	25	45	25	45
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	\overline{CE}_L or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil. SA LA	—	—	50	180	46	175	40	170	40	135
			Com'l. SA LA	50	180	50	170	46	155	40	130	40	120
				50	130	50	120	46	110	40	95	40	85
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(5)}$	Mil. SA LA	—	—	1.2	40	1.2	40	1.2	35	1.0	30
			Com'l. SA LA	1.2	15	1.2	15	1.2	15	1.0	15	1.0	15
				0.4	4	0.4	4	0.4	4	0.2	4	0.2	4
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs $f = 0^{(5)}$)	One Port \overline{CE}_L or $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil. SA LA	—	—	50	170	45	160	45	150	40	125
			Com'l. SA LA	50	160	50	150	45	137	40	115	40	105
				46	125	46	115	42	105	35	90	35	80

2692 b1 05

NOTES:

- x in part numbers indicates power rating (SA or LA).
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- At $f = f_{MAX}$, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/ t_{RC} , and using "AC TEST CONDITIONS" of input levels of GND to 3V.
- f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- Not available in DIP packages — see 7032/7042 data sheet.
- DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽¹⁾ (Continued) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	Version	7132 x 55	7132 x 70	7132 x 90	7132 x 100	7132 x 120 ⁽³⁾	Unit
				7142 x 55 Typ. Max.	7142 x 70 Typ. Max.	7142 x 90 Typ. Max.	7142 x 100 Typ. Max.	7142 x 120 Typ. Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = f_{MAX}$	Mil. SA	65 230	65 225	65 200	65 190	65 190	mA
				LA	65 185	65 180	65 160	65 155	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\overline{CEL} and $\overline{CER} \geq V_{IH}$ $f = f_{MAX}^{(4)}$	Mil. SA	25 65	25 65	25 65	25 65	25 65	mA
				LA	25 55	25 55	25 45	25 45	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	\overline{CEL} or $\overline{CER} \geq V_{IH}$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil. SA	40 135	40 135	40 125	40 125	40 125	mA
				LA	40 110	40 110	40 100	40 100	
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CEL} and $\overline{CER} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(5)}$	Mil. SA	1.0 30	1.0 30	1.0 30	1.0 30	1.0 30	mA
				LA	0.2 10	0.2 10	0.2 10	0.2 10	
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs, $f = 0^{(5)}$)	One Port \overline{CEL} or $\overline{CER} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil. SA	40 120	40 115	40 110	40 110	40 110	mA
				LA	35 90	35 85	35 80	35 80	
			Com'l. SA	40 100	40 100	40 95	40 95	— —	mA
				LA	35 75	35 75	35 70	35 70	

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NOTES:

- x in part numbers indicates power rating (SA or LA).
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- At $f = f_{MAX}$, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
- $f = 0$ means no address or control lines change. Applies only to inputs at CMOS level standby.
- Not available in DIP packages — see 7032/7042 data sheet.
- DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions	IDT7132LA/IDT7142LA			Unit	
			Min.	Typ.	Max.		
V _{DR}	V _{CC} for Data Retention		2.0	—	0	V	
I _{CCDR}	Data Retention Current	$V_{CC} = 2.0V, \overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Mil.	—	100	4000	μA
			Com'l.	—	100	1500	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	ns	
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	ns	

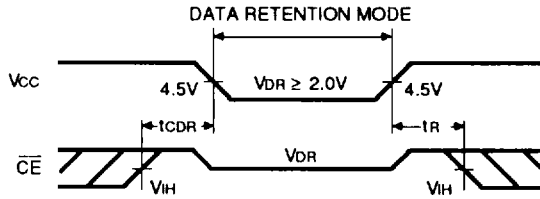
2692 bl 07

NOTES:

- V_{CC} = 2V, T_A = +25°C
- t_{RC} = Read Cycle Time
- This parameter is guaranteed but not tested.

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DATA RETENTION WAVEFORM



2692 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, 3 & 4

2692 tbl 08

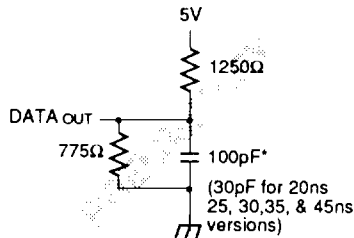


Figure 1. Output Load

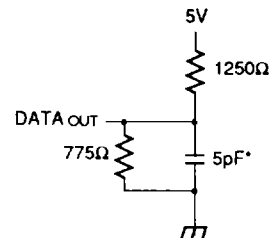


Figure 2. Output Load (for thv, tLZ, twZ, and tOw)

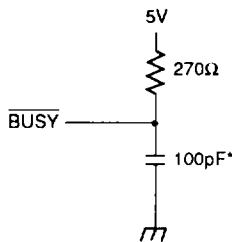


Figure 3. Busy Output Load (IDT7132 only)

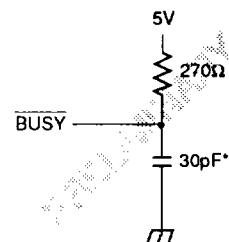


Figure 4. BUSY Output Load (for 20ns, 25ns and 30ns versions)

* Including scope and jig

2692 drw 06

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (5)

Symbol	Parameter	7132 x 20 ^(2,8) 7142 x 20 ^(2,6)		7132 x 25 ⁽⁶⁾ 7142 x 25 ⁽⁶⁾		7132 x 30 ⁽⁶⁾ 7142 x 30 ⁽⁶⁾		7132 x 35 ⁽⁷⁾ 7142 x 35 ⁽⁷⁾		7132 x 45 7142 x 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
t _{ACE}	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
t _{AOE}	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
t _{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
t _{LZ}	Output Low Z Time ^(1, 4)	0	—	0	—	0	—	5	—	5	—	ns
t _{HZ}	Output High Z Time ^(1, 4)	—	8	—	10	—	12	—	15	—	20	ns
t _{PU}	Chip Enable to Power Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽⁴⁾	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 09

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (5) (Continued)

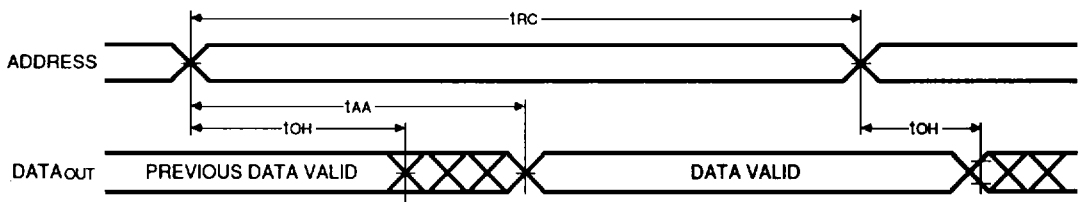
Symbol	Parameter	7132 x 55 7142 x 55		7132 x 70 7142 x 70		7132 x 90 7142 x 90		7132 x 100 7142 x 100		7132 x 120 ⁽³⁾ 7142 x 120 ⁽³⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
t _{AA}	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
t _{ACE}	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
t _{AOE}	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
t _{OH}	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
t _{LZ}	Output Low Z Time ^(1, 4)	5	—	5	—	5	—	5	—	5	—	ns
t _{HZ}	Output High Z Time ^(1, 4)	—	30	—	35	—	40	—	40	—	40	ns
t _{PU}	Chip Enable to Power Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽⁴⁾	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 10

NOTES:

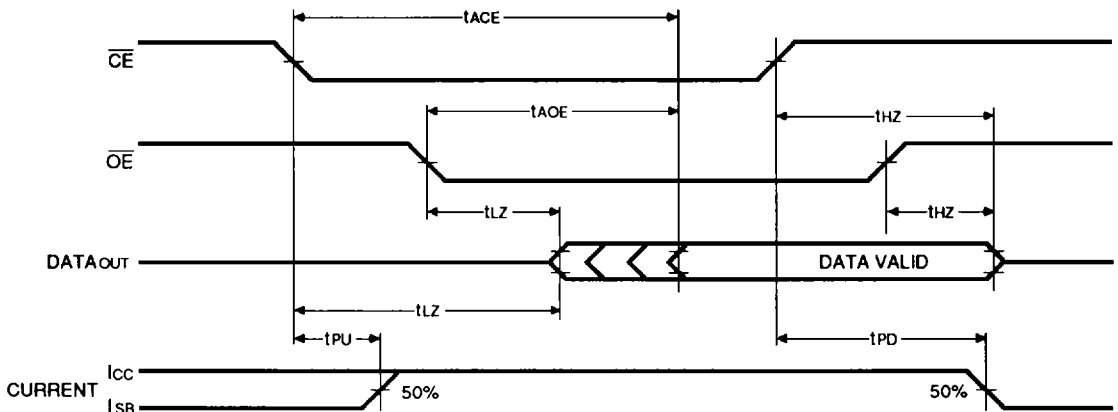
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. *x* in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1,2,4)



2692 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2692 drw 08

NOTES:

1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with \overline{CE} transition low.
4. $\overline{OE} = V_{IL}$.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (7)

Symbol	Parameter	7132 x 20 ^(2,8)		7132 x 25 ⁽⁸⁾		7132 x 30 ⁽⁸⁾		7132 x 35 ⁽⁹⁾		7132 x 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time ⁽⁵⁾	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽⁶⁾	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time ^(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z ^(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write ^(1,4)	0	—	0	—	0	—	0	—	0	—	ns

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NOTES:

1. Transition is measured $\pm 500mV$ from low or high impedance voltage with load (Figures 1, 2, 3 and 4).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $tWC = tBAA + tWP$.
6. Specified for \overline{OE} at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages — see 7032/7042 data sheet.
9. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

**AC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ⁽⁷⁾** (Continued)

Symbol	Parameter	7132 x 55	7132 x 70	7132 x 90	7132 x 100	7132 x 120 ⁽³⁾	Unit
		7142 x 55 Min. Max.	7142 x 70 Min. Max.	7142 x 90 Min. Max.	7142 x 100 Min. Max.	7142 x 120 ⁽³⁾ Min. Max.	
Write Cycle							
tWC	Write Cycle Time ⁽⁵⁾	55 —	70 —	90 —	100 —	120 —	ns
tEW	Chip Enable to End of Write	40 —	50 —	85 —	90 —	100 —	ns
tAW	Address Valid to End of Write	40 —	50 —	85 —	90 —	100 —	ns
tAS	Address Set-up Time	0 —	0 —	0 —	0 —	0 —	ns
tWP	Write Pulse Width ⁽⁶⁾	40 —	50 —	55 —	55 —	65 —	ns
tWR	Write Recovery Time	0 —	0 —	0 —	0 —	0 —	ns
tDW	Data Valid to End of Write	20 —	30 —	40 —	40 —	40 —	ns
tHZ	Output High Z Time ^(1,4)	— 30	— 35	— 40	— 40	— 40	ns
tDH	Data Hold Time	0 —	0 —	0 —	0 —	0 —	ns
twZ	Write Enabled to Output in High Z ^(1,4)	— 30	— 35	— 40	— 40	— 50	ns
tOW	Output Active From End of Write ^(1,4)	0 —	0 —	0 —	0 —	0 —	ns

2692 tbl 12

NOTES:

1. Transition is measured $\pm 500\text{mV}$ from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BA} + t_{WP}$.
6. Specified for OE at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).

CAPACITANCE ($T_A = +25^\circ\text{C}, f = 1.0\text{MHz}$)

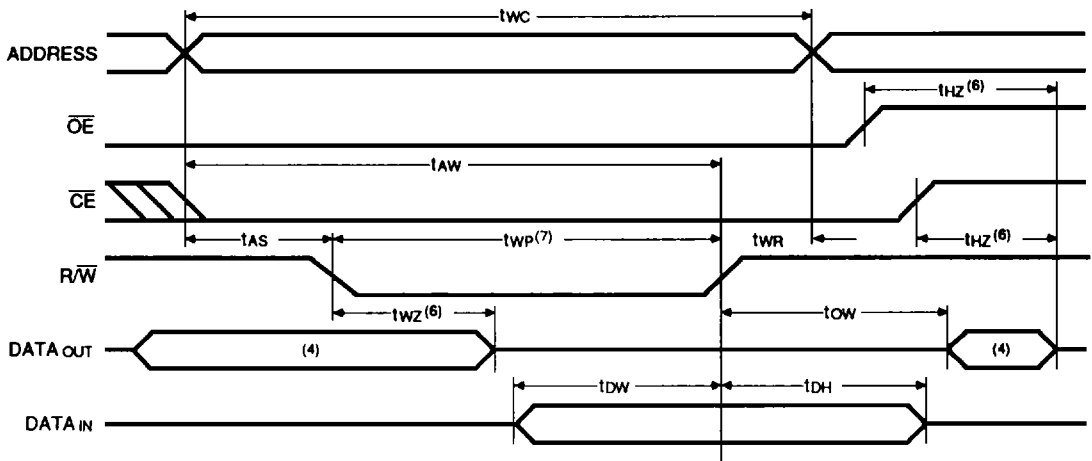
Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	11	pF
C _{OUT}	Output Capacitance	V _{IN} = 0V	11	pF

2692 tbl 13

NOTE:

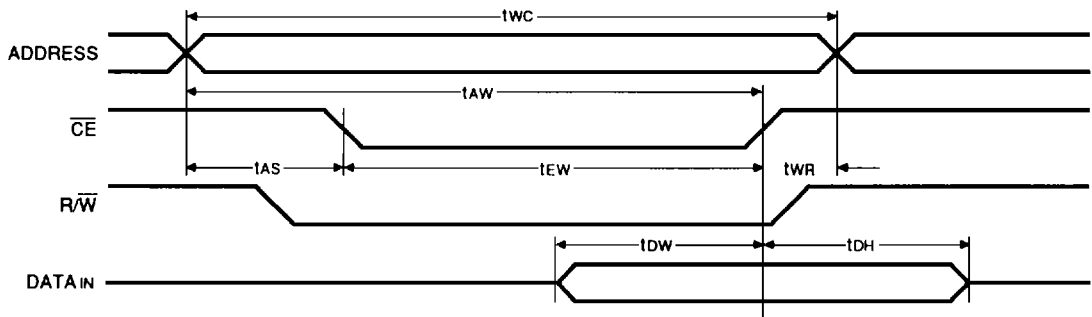
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{R/\overline{W}}$ CONTROLLED TIMING)^(1,2,3,7)



2892 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, (\overline{CE} CONTROLLED TIMING)^(1,2,3,5)



2892 drw 10

NOTES:

1. $\overline{R/\overline{W}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low \overline{CE} and a low $\overline{R/\overline{W}}$.
3. t_{WR} is measured from the earlier of \overline{CE} or $\overline{R/\overline{W}}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CE} low transition occurs simultaneously with or after the $\overline{R/\overline{W}}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state with a 5pF load (including scope and jig).
7. If \overline{OE} is low during a $\overline{R/\overline{W}}$ controlled write cycle, the write pulse width must be larger of t_{WP} or $(t_{WZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is high during an $\overline{R/\overline{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁸⁾

Symbol	Parameter	7132 x 20 ^(1,10)		7132 x 25 ⁽¹⁰⁾		7132 x 30 ⁽¹⁰⁾		7132 x 35 ⁽¹¹⁾		7132 x 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing (For Master IDT7132 Only)												
tBAA	BUSY Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	BUSY Disable Time to Address	—	18	—	20	—	25	—	30	—	35	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	BUSY Disable Time to Chip Enable	—	18	—	20	—	25	—	25	—	25	ns
twDD	Write Pulse to Data Delay ⁽³⁾	—	45	—	50	—	55	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay ⁽³⁾	—	30	—	33	—	33	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽⁵⁾	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to BUSY Input ⁽⁶⁾	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁷⁾	12	—	15	—	20	—	20	—	20	—	ns
twDD	Write Pulse to Data Delay ⁽⁹⁾	—	45	—	50	—	55	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay ⁽⁹⁾	—	30	—	35	—	40	—	35	—	45	ns

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁸⁾

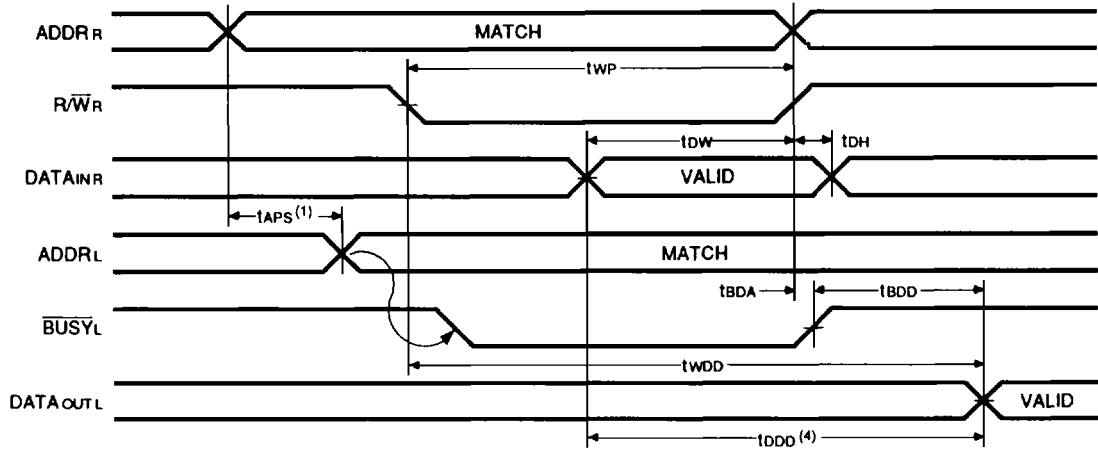
Symbol	Parameter	7132 x 55		7132 x 70		7132 x 90		7132 x 100		7132 x 120 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing (For Master IDT7132 Only)												
tBAA	BUSY Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	BUSY Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	BUSY Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	BUSY Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
twDD	Write Pulse to Data Delay ⁽³⁾	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay ⁽³⁾	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽⁵⁾	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to BUSY Input ⁽⁶⁾	—	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁷⁾	20	—	20	—	20	—	20	—	20	—	ns
twDD	Write Pulse to Data Delay ⁽⁹⁾	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay ⁽⁹⁾	—	55	—	70	—	90	—	100	—	120	ns

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NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY (For Master IDT7132 only)".
- To ensure that the earlier of the two ports wins.
- tBDD is a calculated parameter and is the greater of 0, twDD - tWP (actual) or tDDD - tDW (actual)
- To ensure that the write cycle is inhibited during contention.
- To ensure that a write cycle is completed after contention.
- "x" in part numbers indicates power rating (SA or LA).
- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7142 Only)".
- Not available in DIP packages — see 7032/7042 data sheet.
- DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

TIMING WAVEFORM OF READ WITH $\overline{\text{BUSY}}$ (1,2,3) (FOR MASTER IDT7132 ONLY)

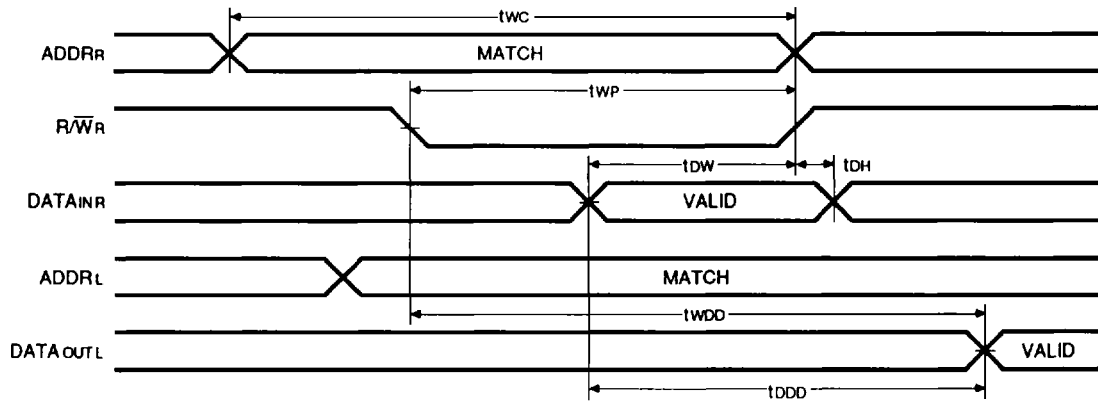


NOTES:

1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{\text{OE}}$ at LO for the reading port.

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TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7142 ONLY)



NOTES:

1. Assume $\overline{\text{BUSY}}$ input at HI for the writing port, and $\overline{\text{OE}}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

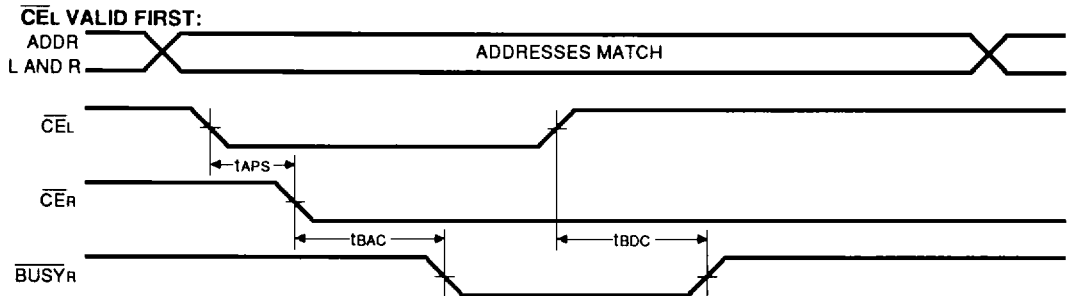
2692 drw 12

TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7142 ONLY)



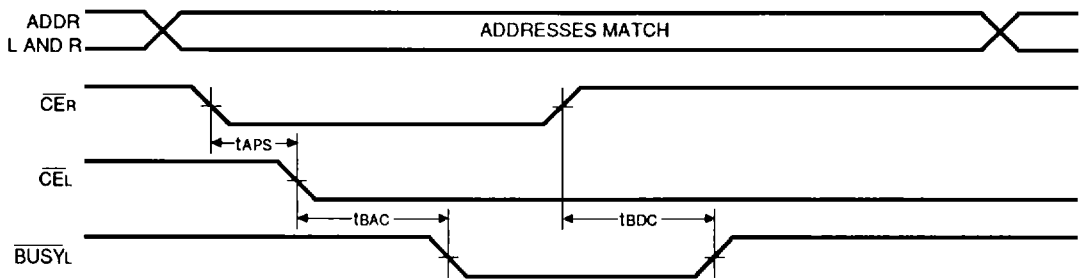
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TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, \overline{CE} ARBITRATION



2692 drw 14

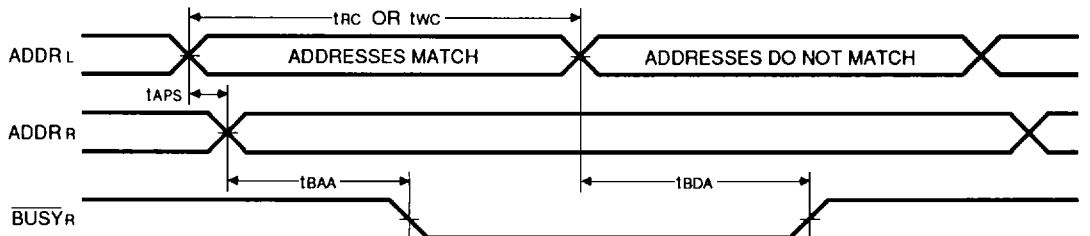
\overline{CE}_R VALID FIRST:



2692 drw 15

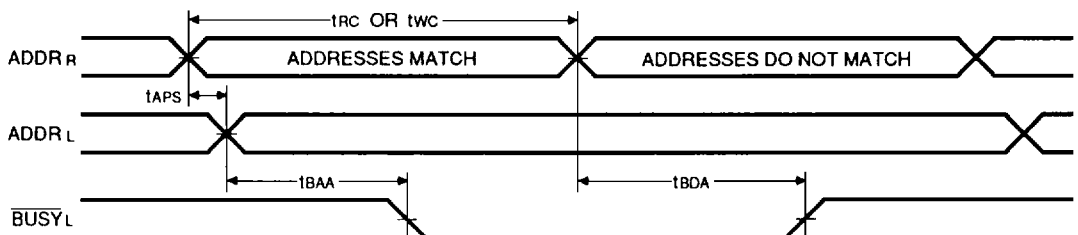
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION ⁽¹⁾

LEFT ADDRESS VALID FIRST:



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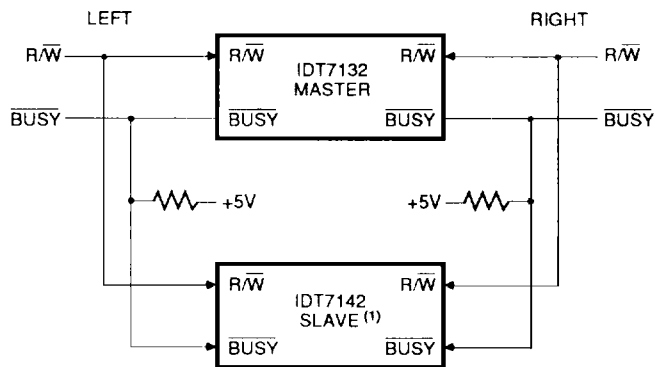
RIGHT ADDRESS VALID FIRST:



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NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2692 drw 18

NOTE:

1. No arbitration in IDT7142 (SLAVE). $\overline{\text{BUSY}}\text{-IN}$ inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{\text{OE}}$). In the read mode, the port's $\overline{\text{OE}}$ turns on the output drivers when set LOW. Non-contention READ/ WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{\text{BUSY}}$ flag will be set for the delayed port.

The $\overline{\text{BUSY}}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{\text{BUSY}}$ flag. $\overline{\text{BUSY}}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the operation is invalid for the port that has $\overline{\text{BUSY}}$ set LOW. The delayed port will have access when $\overline{\text{BUSY}}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{\text{CE}}$, on-chip control logic arbitrates between $\overline{\text{CEL}}$

and $\overline{\text{CER}}$ for access; or (2) if the $\overline{\text{CE}}$ s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{\text{BUSY}}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{\text{BUSY}}\text{L}$ while another activates its $\overline{\text{BUSY}}\text{R}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has $\overline{\text{BUSY}}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{\text{BUSY}}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{\text{BUSY}}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{\text{BUSY}}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION
READ/WRITE CONTROL (4)

Left Or Right Port (1)				Function
R/W	CE	OE	D0-7	
X	H	X	Z	Port Disabled and in Power Down Mode ISB2 or ISB4
X	H	X	Z	CE _R = CE _L = H, Power Down Mode, ISB1 or ISB3
L	L	X	DATA _{IN}	Data on Port Written into Memory(2)
H	L	L	DATA _{OUT}	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance

2692 tbl 16

NOTES:

1. A_{0L} – A_{10L} ≠ A_{0R} – A_{10R}
2. If BUSY = L, data is not written
3. If BUSY = L, data may not be valid, see twdd and tddo timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – ARBITRATION (1,2)

Left Port		Right Port		Flags		Function
CE _L	A _{0L} – A _{10L}	CE _R	A _{0R} – A _{10R}	BUSY _L	BUSY _R	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A _{0R} - A _{10R}	L	≠ A _{0L} - A _{10L}	H	H	No Contention
Address Arbitration With CE Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
CE Arbitration With Address Match Before CE						
LL5R	= A _{0R} - A _{10R}	LL5R	= A _{0L} - A _{10L}	H	L	L-Port Wins
RL5L	= A _{0R} - A _{10R}	RL5L	= A _{0L} - A _{10L}	L	H	R-Port Wins
LW5R	= A _{0R} - A _{10R}	LW5R	= A _{0L} - A _{10L}	H	L	Arbitration Resolved
LW5R	= A _{0R} - A _{10R}	LW5R	= A _{0L} - A _{10L}	L	H	Arbitration Resolved

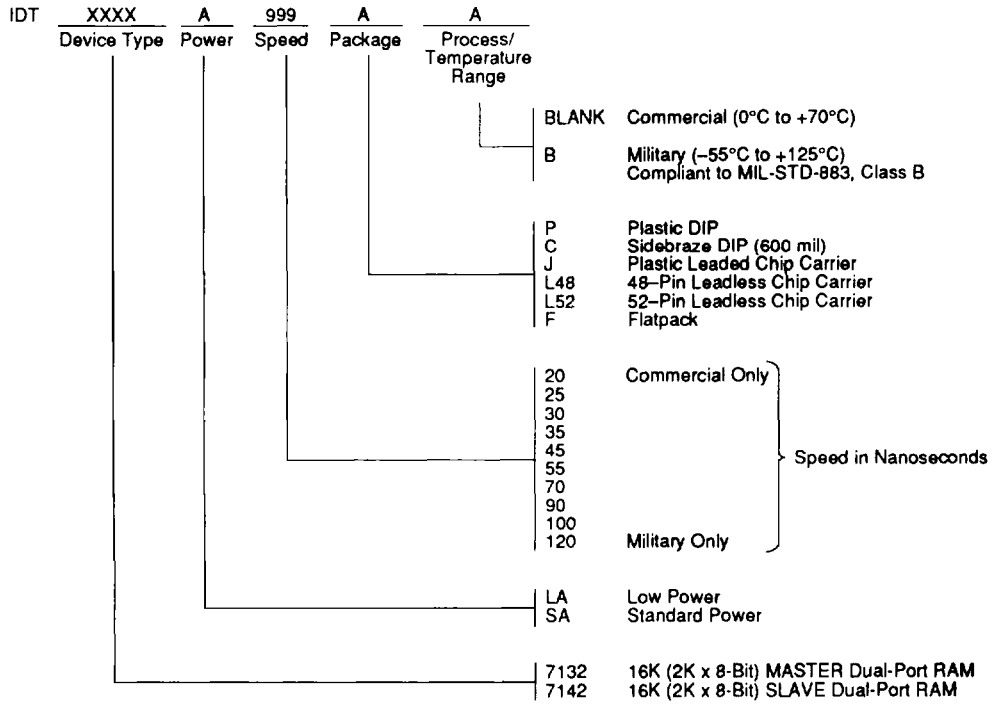
2692 tbl 17

NOTES:

1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid ≥ 5ns before right address.
RV5L = Right Address Valid ≥ 5ns before left address.
Same = Left and Right Addresses match within 5ns of each other.
LL5R = Left CE = LOW ≥ 5ns before Right CE.
RL5L = Right CE = LOW ≥ 5ns before Left CE.
LW5R = Left and Right CE = LOW within 5ns of each other.

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ORDERING INFORMATION



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