FAIRCHILD
A Schlumberger Company

93Z458/93Z459
16 x 48 x 8 Field Programmable Logic Array

Memory and High Speed Logic

Description

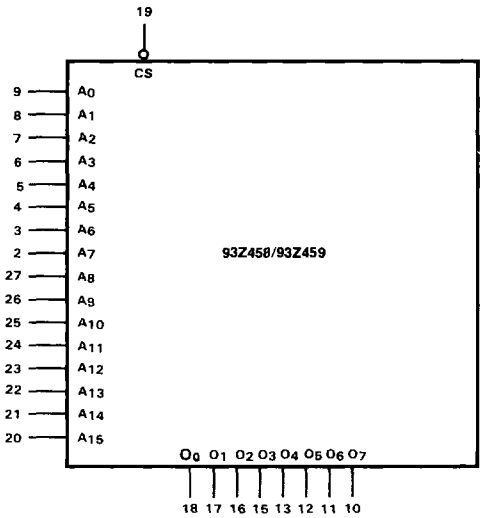
The 93Z458 and 93Z459 are bipolar Field Programmable Logic Arrays (FPLAs) organized with 16 inputs, 48 product terms and eight outputs. The 16 inputs and their complements can be fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates can be fuse linked to eight 48-input OR gates (eight summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93Z458 has open-collector outputs; the 93Z459 has three-state outputs. In either case, the outputs are enabled when CS is LOW.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 65 ns Max**
- **Fully Programmable Product Array, Summing Array and Output Polarity**
- **Available with Open collector (93Z458) or Three State (93Z459) Outputs**

Pin Names

A_0–A_{15}	Address Inputs
$\overline{CS}$	Chip Select Input
O_0–O_7	Data Outputs
V_P	Programming Pin

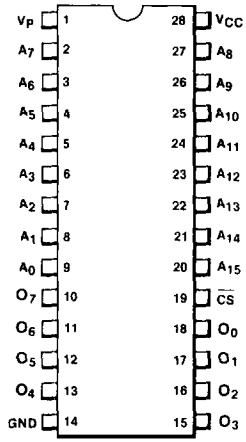
Logic Symbol



V_{CC} = Pin 28
GND = Pin 14

Connection Diagram

28-Pin DIP (Top View)



Note

The 28-pin Flatpak and the 28-pin Leadless Chip Carrier have the same pinout (Connection Diagram) as the 28-pin DIP

93Z458LC

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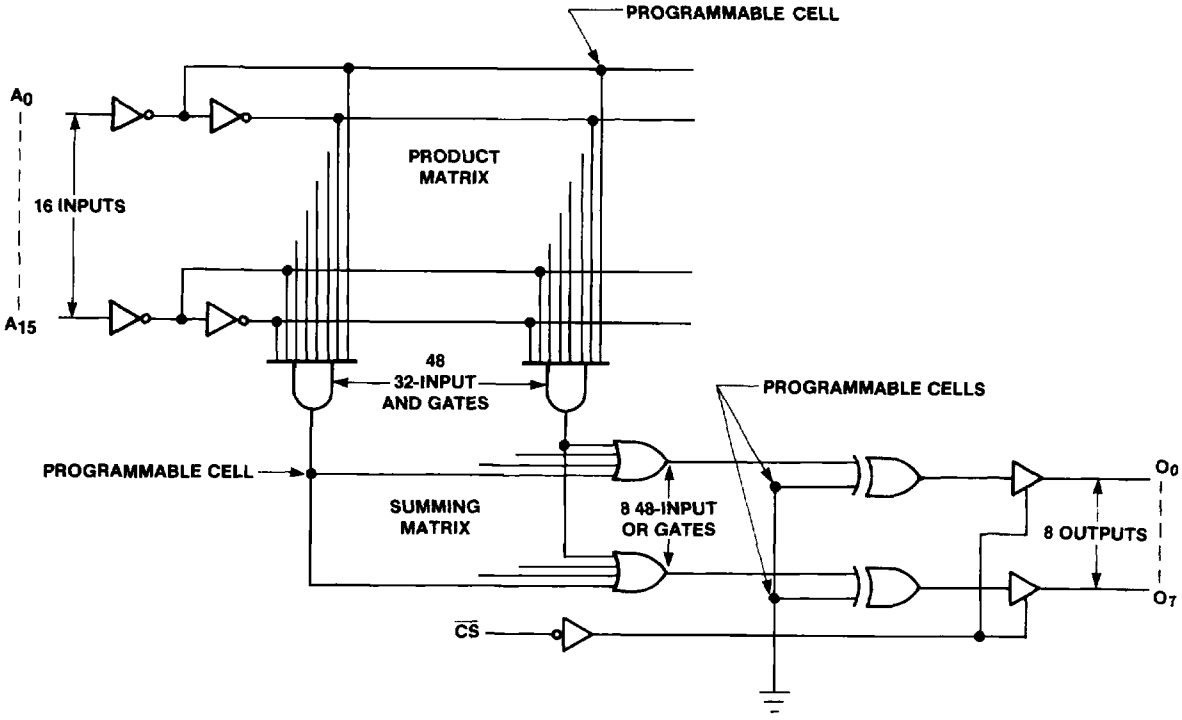
Logic Diagram



Functional Description

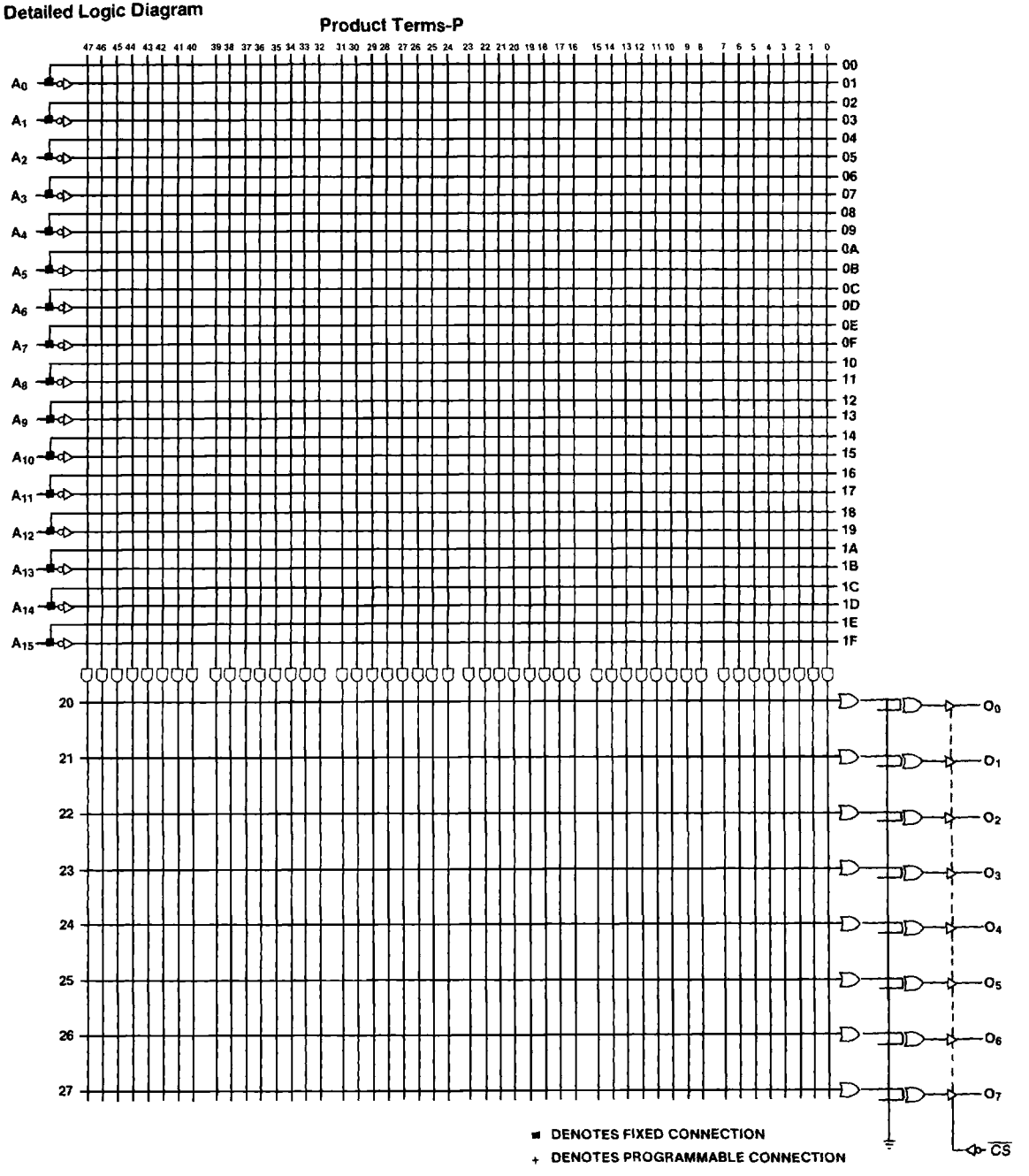
The 93Z458 and 93Z459 are bipolar Field Programmable Logic Arrays (FPLAs) organized 16 inputs by 48 product terms by eight outputs. Open-Collector outputs are provided on the 93Z458 for use in wired-OR systems. The 93Z459 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices is active LOW, i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The 93Z458 and 93Z459 both contain a test input line, two test product term lines and a test output line. These test fuses are accessed during both wafer sort and final test and used to assure high programmability and to guarantee DC parameters and AC performance.

The read function is identical to that of a conventional bipolar PLA. That is, a binary address is applied to inputs A_0 through A_{15}, the chip is selected, and the data is valid at the outputs after t_{AA}.

Programming is accomplished by following the sequence outlined in the *Programming Specifications* table.

Detailed Logic Diagram



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Logic Relationships

Input Term

A_n — n = 0, . . . , 15, one of 16 inputs

Product Term

$P_m = \pi_0^{15} (i_n A_n + j_n \overline{A}_n)$ — m = 0, ... 47, one of 48 product terms

where:

a) $i_n = j_n = 1$ (both true and false programmed)

b) $i_n \neq j_n$ for programmed input (true or false line programmed)

c) $i_n = j_n = 0$ for Don't Care input (unprogrammed input)

$F_r = \Sigma_0^{47} P_m$ — r = 0, . . . , 7, the OR function of the 48 product terms

Summing Term

$S_r = \Sigma_0^{47} k_m P_m$ — where $k_m = 0$ for product term inactive

$k_m = 1$ for product term active

				Output	
Mode	$\overline{CS}$	F_r	S_r	**Active HIGH**	**Active LOW**
Read	L	H	L	L	H
	L	H	H	H	L
	L	L	X	L	H
Disable	H	X	X	H (93Z458) High-Z (93Z459)	H (93Z458) High-Z (93Z459)
	H	X	X		

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Don't Care

By programming, the eight outputs of an FPLA can be made to relate to the 16 inputs as given by the following example:

8 outputs total

$O_1 = A_0 \overline{A}_6 A_{14} + \overline{A}_2 \overline{A}_{15} + \overline{A}_0 A_1 \ldots A_{15} + \overline{A}_8 A_{10} \overline{A}_{13}$

One Product Term
16 input terms max

One Output
48 product terms max

$O_2 = A_0 \overline{A}_6 A_{14} + \overline{A}_2 \overline{A}_{15}$
(Output polarity programmed, active HIGH)

$O_7 = \overline{(\overline{A}_8 A_{10} \overline{A}_{13} + A_4 \overline{A}_7 \overline{A}_9 A_{11} \overline{A}_{12})}$
(Output polarity not programmed, active LOW)

Programming
The 93Z458 and 93Z459 are delivered in an unprogrammed state, characterized by:

- **All vertical cells intact**
- **All 8 output buffers in active LOW state**
- **All outputs read HIGH**

Programming and verifying the Product Matrix, the Summing Matrix, and the Output Polarity are outlined below.

Program Product Matrix

In the initial unprogrammed state the 48 AND gates of the product matrix are not connected. Programming the vertical cell located by the selection of an input line, An, and the mth AND gate includes the input term in the logic expression for the mth AND gate. If all vertical cells were programmed, the resulting logic expression for the AND gates would be $A_0\overline{A}_0A_1\overline{A}_1...A_{15}\overline{A}_{15}$. In the unprogrammed state, the logic expression for each AND gate is "1".

- **Program one input at a time.**
- **All unused inputs of programmed product terms are not required to be programmed.**
- **Inputs of unused product lines are not required to be programmed.**
- **Pin 18 (0_0) is in the read mode (open collector). Care must be taken so that this pin is either left open, grounded, or loaded such that the current flowing into the pin does not exceed 16 mA.**

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V.
3. Apply TTL levels to pins 10 through 13, 15, and 16 (0_7 through 0_2) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed (0_7 = LSB and 0_2 = MSB).
4. Apply +12.0 V to all input pins (A_0 through A_{15}).
5. Apply the proper TTL level to an A_n input pin as follows (program one input at a time):
   a. If the product term to be programmed contains the input term A_n (where n = 0 through 15), lower the A_n pin to a TTL LOW level.
   b. If the product term to be programmed contains the input term $\overline{A}_n$, lower the $\overline{A}_n$ to a TTL HIGH level.
6. Connect pin 19 ($\overline{CS}$) to 20V.
7. Apply a programming current ramp to pin 1 (V_p) according to the Programming Specifications table.
8. Repeat steps 4 through 7 for each input of the selected product term.
9. Repeat steps 3 through 8 for all other product terms to be programmed.

Verify Product Matrix

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V or 4.5 V[1].
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 10 through13, 15, and 16 (0_7 through 0_2) to address an on-chip 1-of-48 decoder to select the product line to be read (0_7 = LSB and 0_2 = MSB).
5. Apply +12.0 V to all input pins (A_0 through A_{15}).
6. Test the state of the A_n input as follows:
   a. Lower the A_n pin to a TTL HIGH level and sense the voltage on pin 18 (0_0).
   b. Lower the A_n pin to a TTL LOW level and sense the voltage on pin 18 (0_0).
7. The state of the A_n input is determined as follows:

	A_n = TTL HIGH	A_n = TTL LOW	Condition of A_n for Selected Product Term
	H	H	Unprogrammed
Level at	H	L	A_n in P-Term
Output 0	L	H	$\overline{A}_n$ in P-Term
(notes 2, 3,4)	L	L	Both A_n and $\overline{A}_n$ in P-Term

8. Repeat steps 5 through 7 for each input of the selected product term.
9. Repeat steps 4 through 8 for all other product terms.

Notes

1. When verifying each cell immediately after applying the current ramp, V_{CC} can be held at 6.5V.
   The verification cycle (blank check or pattern check) must consist of two passes, one at V_{CC} = 6.5 V, one at V_{CC} = 4.5 V
2. 0_0 in this mode functions as an open-collector output
3. The table above is valid regardless of the polarity (active HIGH or active LOW) of 0_0
4. Pin 1 (V_P) should be either floating or grounded.

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Program Summing Matrix

The inputs to the eight OR gates of the summing matrix are not connected in the unprogrammed state. Programming the vertical cell located by the selection of the mth AND gate and the nth summing line includes the product term P_m (the term programmed into the mth AND gate) in the logic expression for the nth OR gate. The nth summing line is selected by the selection of the nth output buffer where n = 0 through seven. If all the cells in the OR matrix were programmed, the resulting logic expression (sum of products) for the OR gates would be $P_0 + P_1 + P_2 ... + P_{47}$.

- **Program one output pin at a time.**
- **All unused product lines are not required to be programmed.**

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V.
3. Apply TTL levels to pins 4 through 9 (A_5 through A_0) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed (A_0 = LSB and A_5 = MSB).
4. Apply TTL HIGH level to pins 20 and 21 (A_{15} and A_{14}).
5. Connect the remaining input pins to + 12.0 V.
6. Connect pin 19 ($\overline{CS}$) to 20 V.
7. Apply a current ramp (see Programming Specifications table) at the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.
8. Repeat for all outputs that are to be programmed.

Verify Summing Matrix

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V or 4.5 V.
3. Connect pin 19 ($\overline{CS}$) to TTL LOW level.
4. Apply TTL levels to pins 4 through 9 (A_5 through A_0) to address an on-chip 1-of-48 decoder to select the AND gate to be verified (A_0 = LSB and A_5 = MSB).
5. Apply a TTL HIGH level to pins 20 and 22 (A_{15} and A_{13}).
6. Connect the remaining input pins to +12.0 V.
7. Sense the voltage on the output pin to be verified. The programming of the selected product line to the output line can be determined as follows:

Output Reads (Note)	Vertical Cell
L	Unprogrammed (inactive)
H	Programmed (active)

Note
The condition of the vertical cell can be determined from the table above regardless of the polarity (active HIGH or active LOW) of the output buffer being verified.

8. Repeat step 7 for all outputs to be verified.
9. Repeat for all product terms programmed.

Program Output Polarity

The initial unprogrammed state of all eight output buffers is active LOW or inverting. To program an output buffer into the active HIGH or non-inverting state, follow the steps shown below:

- **Program one output at a time.**

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V.
3. Apply a TTL HIGH level to pins 4 through 9 (A_5 through A_0).
4. Apply a TTL HIGH level to pin 20 (A_{15}).
5. Connect the remaining input pins to +12.0 V.
6. Connect pin 19 ($\overline{CS}$) to 20V.
7. Apply a programming current ramp (see Programming Specifications table) to the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

Verify Output Polarity

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V or 4.5 V.
3. Connect pin 19 ($\overline{CS}$) to a TTL LOW level.
4. Apply a TTL HIGH level to pins 4 through 9 (A_5 through A_0).
5. Apply a TTL HIGH level to pins 21 and 22 (A_{14} and A_{13}).
6. Connect the remaining input pins to + 12.0 V.
7. Sense the voltage on the pin of the output buffer to be verified. The condition of the output can be determined as follows:

Output Reads	Output State
H	Active LOW
L	Active HIGH

8. Repeat step 7 with V_{CC} at the LOW V_{CC} Read recommended value.

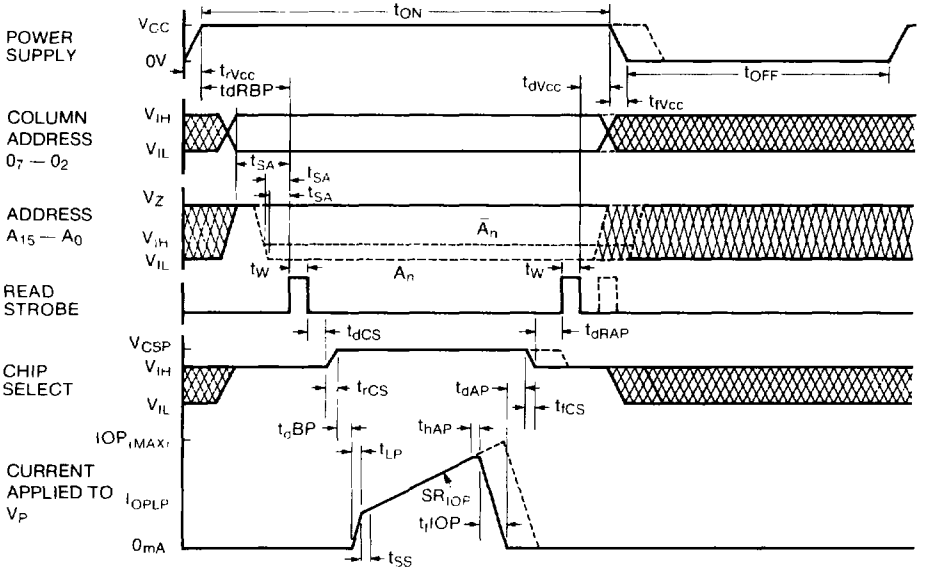
The table given below summarizes the full programming and verifying procedures.

Summary of Pin Voltages (Volts)

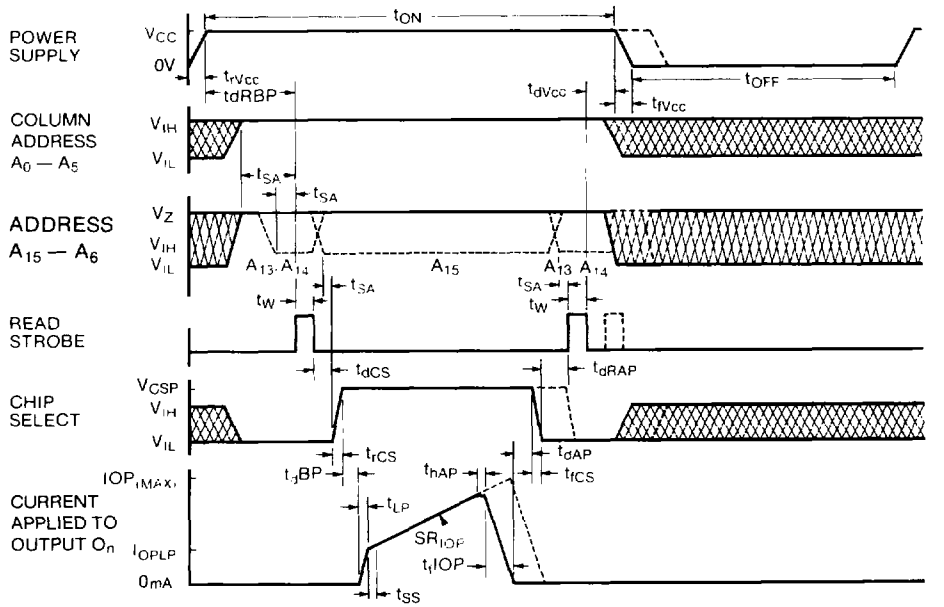
	Read	Program Product Matrix	Verify Product Matrix	Program Summing Matrix	Verify Summing Matrix	Program Output Polarity	Verify Output Polarity
Pin 1 (V_P)	***	*****	***	***	***	***	***
Pin 2 (A_7)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 3 (A_6)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 4 (A_5)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 5 (A_4)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 6 (A_3)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 7 (A_2)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 8 (A_1)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 9 (A_0)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 10 (O_7)	READ	TTL	TTL	****	READ	****	READ
Pin 11 (O_6)	READ	TTL	TTL	****	READ	****	READ
Pin 12 (O_5)	READ	TTL	TTL	****	READ	****	READ
Pin 13 (O_4)	READ	TTL	TTL	****	READ	****	READ
Pin 14 (GND)	GND	GND	GND	GND	GND	GND	GND
Pin 15 (O_3)	READ	TTL	TTL	****	READ	****	READ
Pin 16 (O_2)	READ	TTL	TTL	****	READ	****	READ
Pin 17 (O_1)	READ	**	**	****	READ	****	READ
Pin 18 (O_0)	READ		READ	****	READ	****	READ
Pin 19 ($\overline{CS}$)	TTL LOW	20.0	TTL HIGH	20.0	TTL LOW	20.0	TTL LOW
Pin 20 (A_{15})	TTL	12.0*	12.0*	TTL HIGH	TTL HIGH	TTL HIGH	12.0
Pin 21 (A_{14})	TTL	12.0*	12.0*	TTL HIGH	12.0	12.0	TTL HIGH
Pin 22 (A_{13})	TTL	12.0*	12.0*	12.0	TTL HIGH	12.0	TTL HIGH
Pin 23 (A_{12})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 24 (A_{11})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 25 (A_{10})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 26 (A_9)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 27 (A_8)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 28 (V_{CC})	5.0	6.5	6.5	6.5	6.5	6.5	6.5

*For selection of input apply TTL HIGH or TTL LOW
**Left open or TTL HIGH
***Left open or grounded
****Left open, TTL HIGH, or programming current ramp
*****Programming current ramp

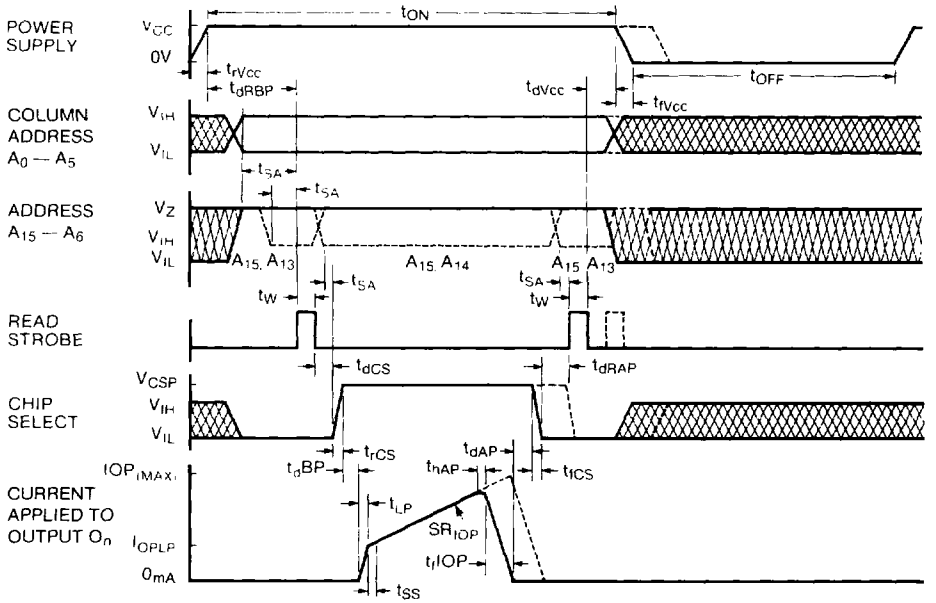
Product Matrix
Programming Timing Diagram



Output Polarity
Programming Timing Diagram



Summing Matrix
Programming Timing Diagram



Note: Current Pulse programming may be used in place of Current Ramp programming. See pages 7-20 and 7-21

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Programming Specifications(4)

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Power Supply						
V_{CC}	Power Supply Voltage	6.4	6.5	6.6	V	Typical I_{CC} at 6.5 V = 250 mA
t_{rVcc}	Power Supply Rise Time(3)	0.2	2.0		μs	
t_{fVcc}	Power Supply Fall Time	0.2	2.0		μs	
t_{ON}	V_{CC} On Time	(1)				See Programming Timing Diagram
t_{OFF}	V_{CC} Off Time	(2)				
	Duty Cycle for V_{CC}			50	%	$t_{ON}/(t_{OFF} + t_{ON})$

Programming Specifications (4) (Cont'd)

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Read Strobe						
t_{dRBP}	Read Delay before Programming		3.0		μs	Initial Check
t_w	Fuse Read Time		1.0		μs	
t_{dVcc}	Delay to V_{CC} Off		1.0		μs	
t_{dRAP}	Delay to Read after Programming		3.0		μs	Verify
V_Z	Input Level during Program & Verify	11.0	12.0	12.0	V	
Chip Select						
V_{CSP}	Chip Select Programming Voltage	19.5	20.0	20.5	V	
I_{CSP}	Chip Select Program Current Limit	175	180	185	mA	
V_{IL}	Input Voltage LOW	0	0	0.4	V	
V_{IH}	Input Voltage High	2.4	5.0	5.0	V	
t_{dCS}	Delay to Chip Deselect		1.0		μs	
t_{rCS}	Chip Select Pulse Rise Time	3.0	4.0		μs	
t_{dAP}	Delay to Chip Select Time	0.2	1.0		μs	
t_{fCS}	Chip Select Pulse Fall Time	0.1	0.1	1.0	μs	
Current Ramp						
I_{OPLP}	Programming Current Linear Point		10	20	mA	Point after which the programming current ramp must rise at a linear slew rate
$I_{OP(max)}$	Output Programming Current Point	155	160	165	mA	Apply current ramp to selected output
$V_{OP(max)}$	Output Programming Voltage Limit	24	25	26	V	
SR_{IOP}	Current Slew Rate	0.9	1.0	1.1	mA/μs	Constant after Linear Point
V_{PS}	Blow Sense Voltage	0.7			V	
t_{dBP}	Delay to Programming Ramp	2.0	3.0		μs	V_{CSP} must be at minimum specification
t_{LP}	Time to Reach Linear Point	0.2	1.0	10	μs	
t_{SS}	Program Sense Inhibit	2.0	3.0	10	μs	
t_{tP}	Time to Program Fuse	3.0		150	μs	
t_{hAP}	Programming Ramp Hold Time	1.4	1.5	1.6	μs	After fuse programs
t_{flOP}	Program Ramp Fall Time		0.1	0.2	μs	
t_{SA}	Time to Address Setup	0.3	0.5		μs	

Notes

1. Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.
2. T_{OFF} is equal to or greater than t_{ON}
3. Rise and fall times are from 10% to 90%
4. Reccommended programming temp. $T_A = +25°C \pm 10°C$.

16 x 48 x 8 FPLA Program Table

This Portion to be Completed by Fairchild

Customer Name _____ CF (XXXX) _____

Purchase Order # _____ Customer Symbolized Part # _____

Fairchild Device # _____ Date Received _____

Total Number of Parts _____ Comments _____

Program Table # _____ Rev _____ Date _____

Program Table Entries						
Input Variable			Output Function		Output Active Level	
A_n	$\overline{A}_n$	Immaterial	Product Term Present in F_r	Product Term Not Present in F_r	Active HIGH	Active LOW
H	L	- (dash)	A	- (period)	H	L
Note Enter (—) for *unused* inputs of *used* P terms			**Notes** 1) Entries independent of output polarity 2) Enter (A) for *unused* outputs of *used* P terms		**Notes** 1) Polarity programmed once only 2) Enter (L) for all *unused* outputs	

	Product Term*																Active Level							
	Input Variable																							
No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Output Function*							
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*Input and Output fields of *unused* P-terms can be left blank

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DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min. I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93Z459 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA	
I_{IL}	Input LOW Current		−120	−250	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93Z459 only)			50 −50	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93Z459 only)			100 −100	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93Z458 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V. 0° C to +75° C Chip Deselected	
I_{CEX}	Output Leakage Current (93Z458 only)			150	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V. −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93Z459 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2	
I_{CC}	Power Supply Current			170	mA	V_{CC} = Max, Chip Selected,	
C_{IN}	Input Pin Capacitance (3)		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 2.0 V, f = 1.0 MHz, $\overline{CS}$ = V_{IH}	
C_O	Output Pin Capacitance (3)		7.0		pF	V_{CC} = 5.0V, V_O = 2.0 V, f = 1.0 MHz, $\overline{CS}$ = V_{IH}	

Commercial

AC Performance Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_C = 0° C to + 75° C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	45	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	30	ns	See AC Output Load
t_{CD}	Chip Select to Output Disable Time	30	ns	See AC Output Load

Notes on following page

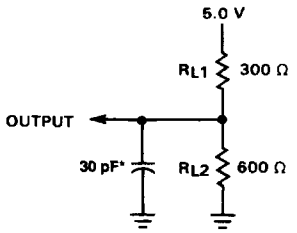
Military

AC Performance Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_C = -55°C to +125°C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	65	ns	See AC Test Output Load
t_{ACS}	Chip Select to Output Access Time	30	ns	See AC Test Output Load
t_{CD}	Chip Select to Output Disable Time	30	ns	See AC Test Output Load

1. Typical values are at V_{CC} = 5.0 V, T_C = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second
3. These parameters are not 100% tested, but are checked during initial design and during design changes.

Fig. 1 AC Test Loads



*Includes jig and scope capacitance

Fig. 3 Read Mode Timing

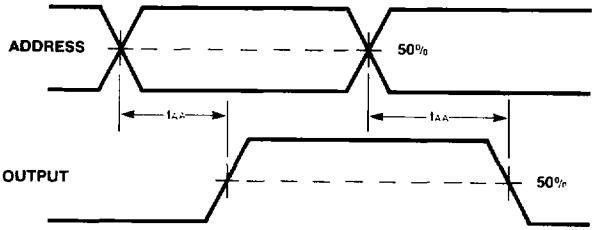
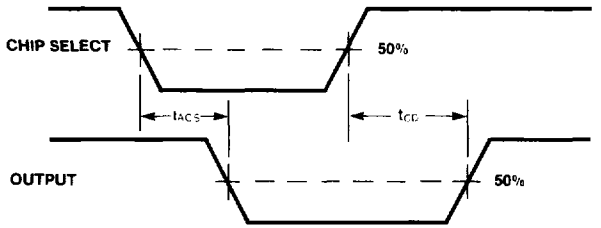
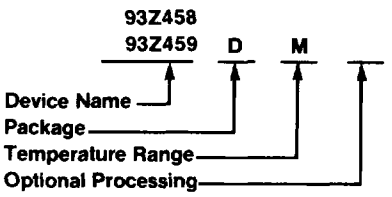


Fig. 2 Chip Select Timing



Ordering Information



Packages
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier
- P = Plastic DIP

Temperature Ranges
- C = 0°C to +75°C
- M = -55°C to +125°C

Optional Processing
- QB = Mil Std 883 Method 5004 & 5005, Level B
- QR = Commercial Device with 160 Hour Burn In or Equivalent

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