VLSI TECHNOLOGY, INC.

PRELIMINARY **VT2KF9**

2,064 x 9 FIFO MEMORY

FEATURES

- First-in, first-out dual-port memory
- Low-power 2.0-micron CMOS process
- Fully asynchronous operation
- Simultaneous read and write
- Fully expandable in depth and width
- Access time: 50 ns
- Dependable empty, half-full, and full warning flags
- Rate buffer applications
- Multi-processing master/slave applications
- 28-pin, 600-mil dual in-line package
- 32-pin PLCC package

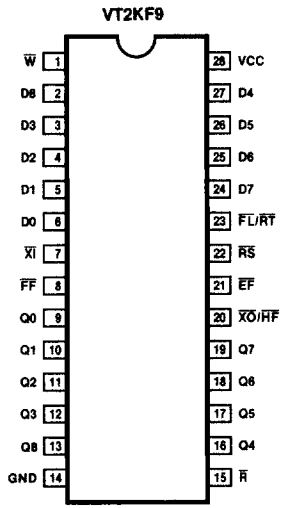
DESCRIPTION

The VT2KF9 is a first-in, first-out (FIFO) memory that uses a high-performance static RAM array with internal logic to ensure totally asynchronous operation. Full, half-full, and empty flags are provided to allow the device to operate without external logic. The VT2KF9 also contains logic that allows for unlimited expansion in both word size and depth.

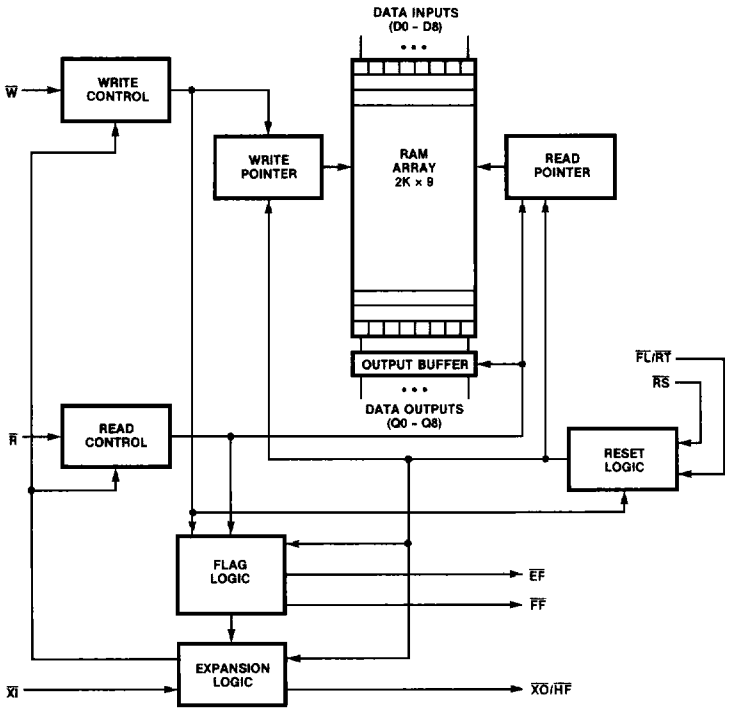
Although the VT2KF9 uses a static RAM array as its memory element, a system of read and write pointers has been included to sequence through the array. Data is toggled in and out of the device by means of the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) signals. The VT2KF9 has an access time of 50 ns and a read/write cycle time of 65 ns (15 MHz). Its 2,064 x 9 organization permits the use of control or parity bits at the option of the user, and also allows a 2,064-deep word structure without the need for expansion.

The VT2KF9 is fabricated using VLSI Technology's high-performance 2-micron CMOS process. Its design is ideally suited to asynchronous and simultaneous reading and writing in multi-processing and rate buffer applications. The FIFO is available in both plastic dual in-line and plastic leaded chip carrier packages.

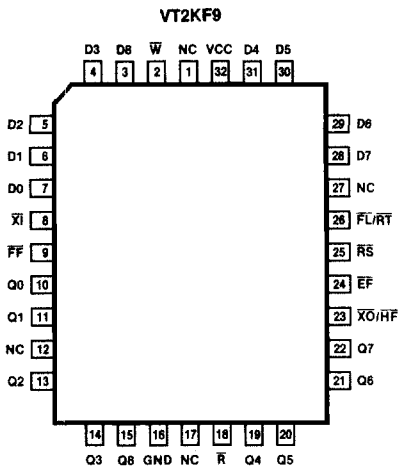
PIN DIAGRAM



BLOCK DIAGRAM



PIN DIAGRAM



PIN NAMES

D0-D8	Data Inputs
Q0-Q8	Data Outputs
$\overline{RS}$	Reset
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{FL}/\overline{RT}$	First Load/Retransmit
$\overline{XI}$	Expansion-In
$\overline{XO}/\overline{HF}$	Expansion-Out/Half-Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
VCC	Power (5 V)
GND	Ground (0 V)

FUNCTIONAL DESCRIPTION

The VT2KF9 is a first-in, first-out (FIFO) memory that is organized 2,064 words by 9 bits. It uses a high-performance static RAM as its memory array element. A system of read and write pointers sequences through the array, with data being toggled in and out by the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) signals. The VT2KF9 can operate in one of several modes.

It should be noted that a reset cycle is required after power-on.

OPERATING MODES

SINGLE-DEVICE MODE

When only one VT2KF9 is used, up to 2,064 9-bit words may be written into it and retrieved on a first-in, first-out basis. In this mode, the $\overline{XO}/\overline{HF}$ pin is a half-full flag and the Expansion-In ($\overline{XI}$) pin should be grounded.

WIDTH EXPANSION MODE

Word width may be expanded in 9-bit increments simply by connecting the input and output control signals to multiple devices and paralleling the data inputs and outputs. In this mode, the flags of any one VT2KF9 may be used (the flag outputs should not be wired together).

DEPTH EXPANSION MODE (DAISY CHAIN)

Multiple VT2KF9s can be interconnected to produce a single FIFO of greater than 2,064 words. This daisy chaining is accomplished by:

1. Connecting the First-Load ($\overline{FL}$) pin of the first FIFO to ground.
2. Pulling $\overline{FL}$ HIGH on all the other FIFOs.
3. Connecting the Expansion-Out ($\overline{XO}$) pin of each FIFO to the Expansion-In ($\overline{XI}$) pin of the next FIFO. The $\overline{XO}$ pin of the last (or deepest) FIFO is connected to the $\overline{XI}$ pin of the first device (the one with $\overline{FL}$ grounded).

Externally ORing all Empty Flag ($\overline{EF}$) pins produces a valid Empty flag. The same is true for the Full Flag ($\overline{FF}$) pins. The Retransmit ($\overline{RT}$) capability and Half-Full ($\overline{HF}$) flag are not available in this mode.

COMPOUND EXPANSION MODE

The width and depth expansion modes may be combined to produce larger FIFO arrays.

SIGNAL DESCRIPTIONS

INPUTS

Reset ($\overline{RS}$)

A reset cycle is required after power-on.

Holding the Reset ($\overline{RS}$) input signal LOW for the minimum reset pulse width initiates a reset cycle, during which both the read and write pointers are moved to the first location in the FIFO memory. Immediately after the cycle, the Empty Flag ($\overline{EF}$) is asserted (goes LOW), and the Full Flag ($\overline{FF}$) and Half-Full Flag ($\overline{HF}$) are disasserted (go HIGH).

Both Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) must be HIGH (inactive) during the reset cycle.

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Write Enable ($\overline{W}$)
The falling edge of the Write Enable ($\overline{W}$) signal initiates a write cycle if the Full Flag is not set. Data set-up and hold times, however, must be met relative to the rising edge of $\overline{W}$. Data is stored in the FIFO memory independently of any read actions.

Each write cycle increments the write pointer. When the memory becomes half full, the Half-Full Flag ($\overline{HF}$) is asserted (goes LOW) and remains in that state until the FIFO becomes less than half full. When $\overline{HF}$ is disasserted (goes HIGH), it changes on the rising (trailing) edge of the Read Enable ($\overline{R}$) signal.

When the VT2KF9 becomes full, $\overline{FF}$ is asserted and further write operations are inhibited until one or more words of data are read from the FIFO. The Full Flag is then disasserted following the next valid read cycle.

Read Enable ($\overline{R}$)
The falling edge of the Read Enable ($\overline{R}$) signal initiates a read cycle if the Empty Flag is not set. Data is read out on a first-in, first-out basis, and is not affected by concurrent write operations.

When the last word of data is read out of the FIFO, $\overline{EF}$ is asserted (goes LOW). The Empty Flag is disasserted (goes HIGH) following the next valid write cycle. If $\overline{R}$ has not been asserted, the data outputs are in the high-impedance state.

Expansion-In ($\overline{XI}$)
The Expansion-In ($\overline{XI}$) input is used in the depth expansion mode to produce a FIFO of greater than 2,064 words. The $\overline{XI}$ pin of one device in a daisy chain configuration is connected to the Expansion-Out ($\overline{XO}$) pin of the previous device. In single-device mode, the $\overline{XI}$ pin is grounded.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)
The function of the First Load/Retransmit ($\overline{FL}/\overline{RT}$) input depends upon the device operating mode.

In depth expansion mode, the $\overline{FL}/\overline{RT}$ pin is grounded on the first device to be loaded. It is pulled HIGH on all the other devices in the daisy chain, and the filling sequence for those devices is determined by the Expansion-In ($\overline{XI}$) and Expansion-Out ($\overline{XO}$) signals.

In single-device mode, a LOW applied to the $\overline{FL}/\overline{RT}$ input resets the read pointer to the beginning of the FIFO memory so that data can be re-read. The Write Enable ($\overline{W}$) and the Read Enable ($\overline{R}$) inputs must be HIGH while $\overline{FL}/\overline{RT}$ is low.

Data In (D0–D8)
Data inputs.

OUTPUTS

Empty Flag ($\overline{EF}$)
The Empty Flag ($\overline{EF}$) output is asserted (goes LOW) when the FIFO is empty. This inhibits read operations until one or more write operations are completed, or until the FIFO is set to retransmit.

Full Flag ($\overline{FF}$)
The Full Flag ($\overline{FF}$) output is asserted (goes LOW) when the FIFO is full. This inhibits write operations until one or more read operations are completed, or until the FIFO is reset.

Expansion-Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)
The function of the $\overline{XO}/\overline{HF}$ output depends on how the device is used. In the single-device mode, the $\overline{HF}$ signal is asserted (goes LOW) when the FIFO is half full (or more). It remains in that state until the FIFO becomes less than half full. When $\overline{HF}$ is disasserted (goes HIGH), it changes on the rising (trailing) edge of the Read Enable ($\overline{R}$) signal.

In the depth expansion mode, this pin must be connected to the Expansion-In ($\overline{XI}$) pin of the next device. The $\overline{XO}$ pin of the last (deepest) FIFO is connected to the $\overline{XI}$ pin of the first FIFO. Note that the first FIFO is the one that has its First Load ($\overline{FL}$) input grounded. This allows devices to be daisy chained. The Half-Full Flag ($\overline{HF}$) is not available in multiple device mode.

Data Out (Q0–Q8)
Data outputs. When the Read Enable ($\overline{R}$) signal is not asserted, Q0–Q8 are in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Voltage on Any Terminal Relative to Ground	-0.5 V to +7.0 V
Applied Output Voltage	-0.5 V to +7.0 V
Applied Input Voltage	-0.5 V to +7.0 V
Short Circuit Current	30 mA
Power Dissipation	1.0 W

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of this device under these or any other conditions above those listed in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	Input HIGH Voltage	2.2		VCC +1	V	Note 2
VIL	Input LOW Voltage	-1.0		0.8	V	Note 3
VOH	Output HIGH Voltage	2.4			V	IOUT = -1 mA
VOL	Output LOW Voltage			0.4	V	IOUT = 4 mA
IIL	Input Leakage Current (Any Input)	-1		1	μA	0.4 V ≤ VIN ≤ VOUT
IOL	Output Leakage Current	-10		10	μA	$\overline{R} \geq$ VIH, 0.4 V ≤ VOUT
ICC1	Power Supply Current			80	mA	Average operating current
ICC2	Power Supply Current			8	mA	$\overline{R} \approx \overline{W} \approx \overline{RS} \approx \overline{FL} \approx$ VIH
ISB	Standby Current			5	mA	

CAPACITANCE TA = 25°C, f = 1 MHz

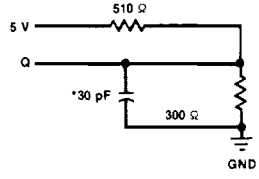
Symbol	Parameter	Typ	Max	Unit	Conditions
CIN	Input Capacitance	7	10	pF	
COUT	Output Capacitance	8	10	pF	

AC TEST CONDITIONS

Input Voltage Levels	0 V to 3 V
Input Transition Times	5 ns
Input Reference Level	1.5 V
Output Reference Level	1.5 V
Output Load	Figures 1 and 2

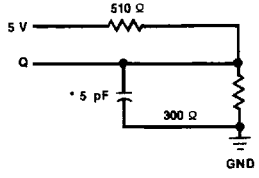
AC TESTING LOAD CIRCUITS

FIGURE 1. OUTPUT LOAD CIRCUIT A



*INCLUDES SCOPE AND TEST JIG.

FIGURE 2. OUTPUT LOAD CIRCUIT B



*INCLUDES SCOPE AND TEST JIG.

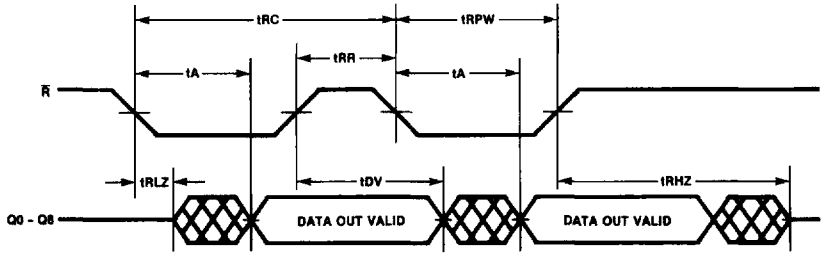
Notes:
1. Operation across temperature range is guaranteed with 400 feet per minute of air flow.
2. All input pins are diode-clamped to VCC. Some testers may not have enough drive capability to reach maximum input voltage.
3. VIL min. is -2.0 V for pulse widths of less than 20 ns.

TIMING CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$, Note 1

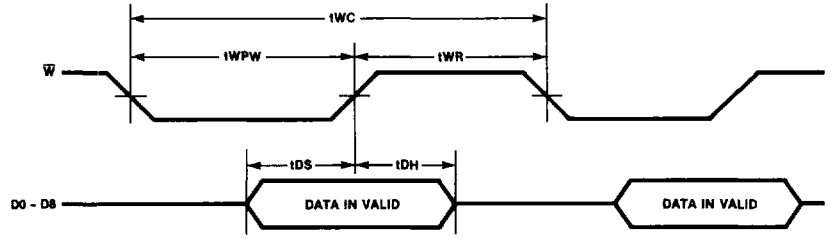
Symbol	Parameter	VT2KF9-50		VT2KF9-65		VT2KF9-80		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
READ CYCLE									
tRC	Read Cycle Time	65		80		100		ns	
tA	Access Time		50		65		80	ns	
tRR	Read Recovery Time	15		15		20		ns	
tRPW	Read Pulse Width	50		65		80		ns	
tRLZ	Read Pulse LOW to Data Outputs Low Z	10		10		10		ns	Note 2
tRHZ	Read Pulse HIGH to Data Outputs High Z		30		30		30	ns	Note 2
tDV	Data Valid from Read Pulse HIGH	5		5		5		ns	
WRITE CYCLE									
tWC	Write Cycle Time	65		80		100		ns	
tWR	Write Recovery Time	15		15		20		ns	
tWPW	Write Pulse Width	50		65		80		ns	Note 2
tDS	Data Set-Up Time	30		30		40		ns	
tDH	Data Hold Time	5		10		10		ns	

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



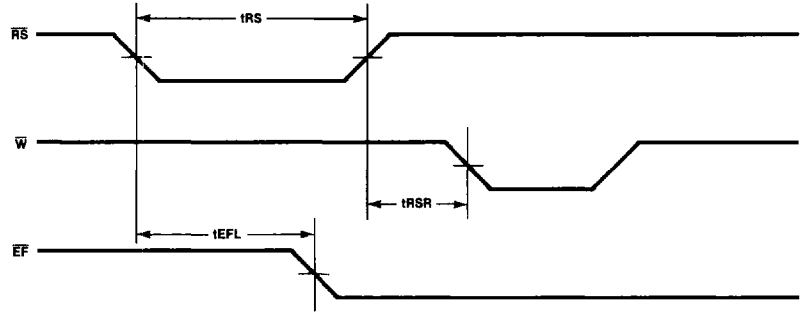
Notes:
1. Timing referenced as in "AC Test Conditions."
2. Values guaranteed by design; not currently tested.

TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

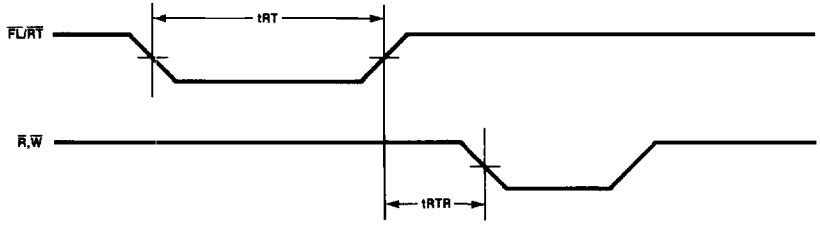
Symbol	Parameter	VT2KF9-50		VT2KF9-65		VT2KF9-80		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
RESET CYCLE, Note 2									
tRSC	Reset Cycle Time	65		80		100		ns	
tRS	Reset Pulse Width	50		65		80		ns	
tRSR	Reset Recovery Time	15		15		20		ns	
tEFL	Reset to Empty Flag LOW		65		80		100	ns	
RETRANSMIT CYCLE									
tRTC	Retransmit Cycle Time	65		80		100		ns	
tRT	Retransmit Pulse Width	50		65		80		ns	
tRTR	Retransmit Recovery Time	15		15		20		ns	

TIMING DIAGRAMS

RESET CYCLE , Note 2



RETRANSMIT CYCLE



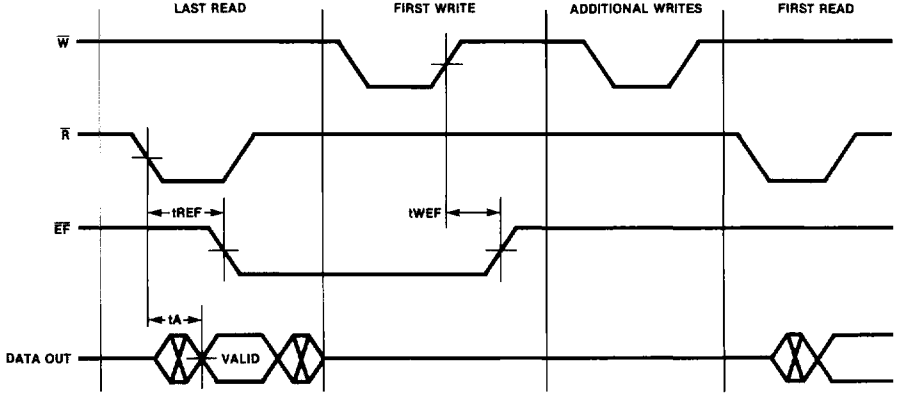
Notes:
1. Timing referenced as in "AC Test Conditions."
2. $\overline{W}$ and $\overline{R}$ = VIH during reset.

TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

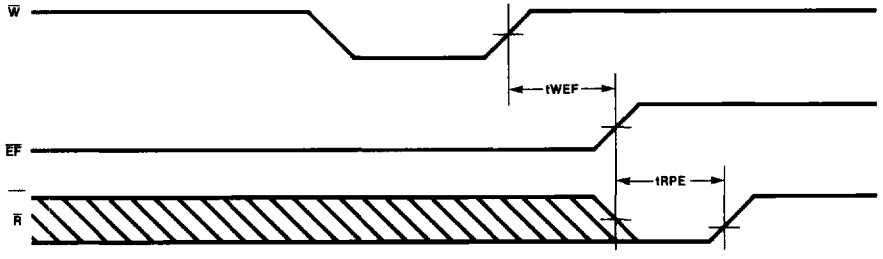
Symbol	Parameter	VT2KF9-50		VT2KF9-65		VT2KF9-80		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
FLAG TIMING									
tEFL	Reset to $\overline{EF}$ LOW	65		80		100		ns	
tREF	Read LOW to $\overline{EF}$ LOW	45		60		70		ns	
tRFF	Read HIGH to $\overline{FF}$ HIGH	45		60		70		ns	
tWEF	Write HIGH to $\overline{EF}$ HIGH	45		60		70		ns	
tWFF	Write LOW to $\overline{FF}$ LOW	45		60		70		ns	
tWHF	Write LOW to $\overline{HF}$ LOW	65		80		100		ns	
tRHF	Read HIGH to $\overline{HF}$ HIGH	65		80		100		ns	

TIMING DIAGRAMS

EMPTY FLAG TIMING: Empty Flag from Last Read to First Write



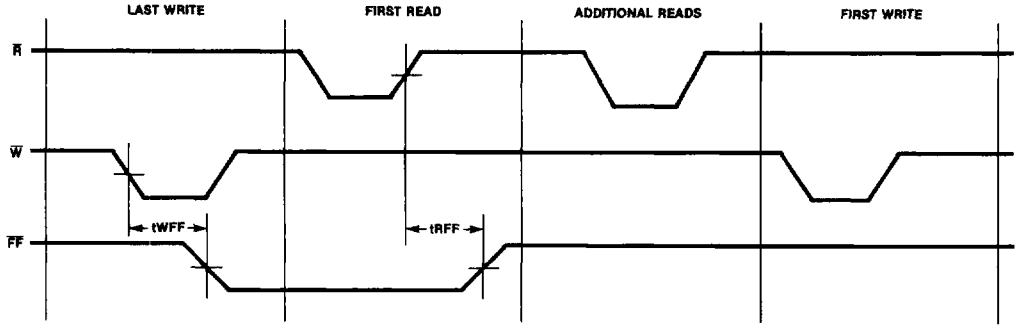
EMPTY FLAG TIMING: Effective Read Pulse Width after $\overline{EF}$ HIGH, Note 2



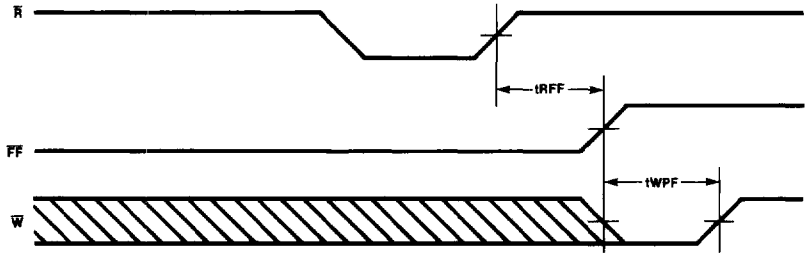
Notes:
1. Timing referenced as in "AC Test Conditions."
2. tRPE = tRPW.

TIMING DIAGRAMS

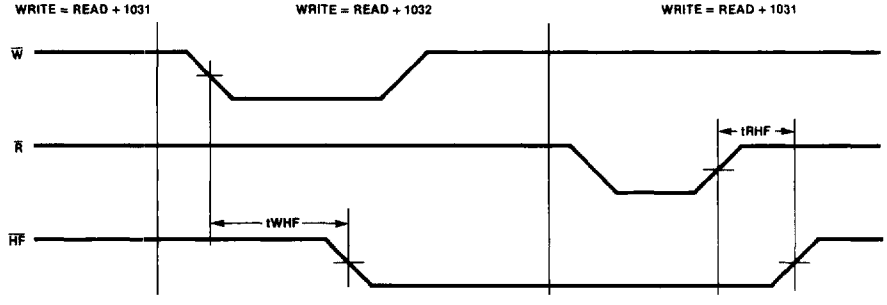
FULL FLAG TIMING: Full Flag from Last Write to First Read



FULL FLAG TIMING: Effective Write Pulse Width after $\overline{FF}$ HIGH (tWPF = tWPW)



HALF-FULL FLAG TIMING



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POWER DISTRIBUTION AND TRACE LINE TERMINATION CONSIDERATIONS

To achieve full compatibility with TTL-based devices, CMOS memories are typically designed to convert TTL input levels to the CMOS levels required for internal operation. Greater power efficiency is achieved, however, when an entire design takes advantage of the lower consumption capabilities of CMOS technology. When CMOS levels are used throughout a design and not only in the memory, lower current specifications can be achieved, resulting in a lower overall power requirement.

The operating margins of all devices on a board using very-high-speed memory can best be maintained by providing a quiet environment that is free of noise spikes, undershoot, and excessive ringing. Key elements in creating such an atmosphere are observing proper power distribution techniques and proper termination of TTL drive lines.

POWER DISTRIBUTION

A power distribution scheme that effectively maintains wide operating margins combines power trace layout with decoupling capacitor placement to minimize the series impedance in the decoupling path. This path runs from the power pin of a memory device through its decoupling capacitor to the ground pin.

The total impedance of this path is established by the power line impedance and the impedance of the capacitor itself. In practice, the capacitive effects of the decoupling path are minimal because of the very-high-frequency components of the current transients associated with memory operation. This makes the line inductance the dominant impedance factor.

The preferred technique for reducing power line impedance and improving the quality of VCC and ground is to use separate power and ground planes.

A somewhat-less-effective approach is to grid the power and ground traces. If this is done, the ground grid should extend to the TTL driver peripheral circuitry, providing a solid ground reference for the TTL drivers.

The decoupling capacitor, which provides energy for the high-frequency transients, should be placed as near the memory device as possible in order to have the shortest practical lead lengths. This capacitor should be of a low inductance type and, at a minimum, be 0.1 μF. For the greatest efficiency, it should be placed between the power supply and ground pins of each device.

Low-frequency current transients can be handled by larger tantalum capacitors placed near the memory board edge connector, where the power traces meet the backplane power distribution system. Such large capacitors provide bulk energy storage that prevents voltage drops caused by the long inductive path between the memory board and the power supply.

TRACE TERMINATION

On a memory board, trace lines have the appearance of shorted transmission lines to TTL-level driver signals. This can cause reflections of TTL signals propagating down the lines, particularly LOW-going signals. These reflections can be reduced or eliminated by proper line termination. Proper termination also reduces RFI emissions.

Trace line termination can be either series or parallel, although series termination is recommended. This type of termination has the advantage of drawing no dc current, and also requires the smallest number of components to implement. It simply calls for placing a series resistor in the signal line to dampen reflections. The resistor is placed at the output of the TTL driver, as close as possible to the driver package. The driver/termination combination should be placed close to the memory array to minimize lead length.

In most applications, a series resistor of between 10 ohms and 33 ohms is sufficient to dampen reflections. However, because the characteristic impedance of each layout is different, some experimentation may be necessary to determine the optimum value for a specific configuration.

SIGNAL FIDELITY

When the layout is complete and the power distribution and line termination requirements have been met, it is good procedure to verify signal fidelity by observation with a wideband (300 MHz or faster) oscilloscope and probe.