

## 9.0 ELECTRICAL CHARACTERISTICS

### 9.1 Absolute Maximum Ratings†

Ambient temperature under bias.....	-55°C to +125°C
Storage temperature.....	-65°C to +150°C
Voltage on VDD with respect to VSS.....	0 to +7.5V
Voltage on MCLR with respect to VSS.....	0 to +14V
Voltage on all other pins with respect to VSS.....	-0.6V to VDD + 0.6V
Total power dissipation (Note 1).....	800 mW
Max. current out of VSS pin.....	150 mA
Max. current into VDD pin.....	50 mA
Max. current into an input pin (TOCKI only).....	±500 µA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD).....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD).....	±20 mA
Max. output current sunk by any I/O pin.....	25 mA
Max. output current sourced by any I/O pin.....	20 mA
Max. output current sourced by a single I/O port (PORTA, B or C).....	40 mA
Max. output current sunk by a single I/O port (PORTA, B or C).....	50 mA

**Note 1:** Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 9-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

OSC	16C5X-04	16C5X-10	16C5X-20	16LC5X-04
RC	VDD: 3.0V to 6.25V IDD: 2.4 mA Max. at 5.5V IPD: 4 µA Max. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 4.5V to 5.5V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 4.5V to 5.5V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 2.5V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 4 µA Max. at 2.5V WDT dis Freq: 2 MHz Max.
XT	VDD: 3.0V to 6.25V IDD: 2.4 mA Max. at 5.5V IPD: 5 µA Max. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 4.5V to 5.5V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 4.5V to 5.5V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 2.5V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 4 µA Max. at 2.5V WDT dis Freq: 4 MHz Max.
HS	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 0.3 µA typ. at 3.0V WDT dis Freq: 4 MHz Max.	VDD: 4.5V to 5.5V IDD: 8 mA Max. at 5.5V IPD: 4 µA Max. at 3.0V WDT dis Freq: 10 MHz Max.	VDD: 4.5V to 5.5V IDD: 16 mA Max. at 5.5V IPD: 4 µA Max. at 3.0V WDT dis Freq: 20 MHz Max.	Do not use in HS mode
LP	VDD: 4.5V to 5.5V IDD: 17 µA typ. at 32 kHz, 3.0V IPD: 0.3 µA typ. at 3.0V WDT dis Freq: 200 kHz typ.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.25V IDD: 11 µA typ. at 32 kHz, 2.5V IPD: 0.25 µA typ. at 2.5V WDT dis Freq: 200 kHz typ.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that guarantees the specifications required.

**TABLE 9-2: DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (COMMERCIAL)**

DC Characteristics Power Supply Pins		Standard Operating Conditions Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ , unless otherwise stated. Operating Voltage $V_{DD} = 3.0\text{V}$ to $5.5\text{V}$ , unless otherwise stated.				
Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
<b>Supply Voltage</b> PIC16C5X-XT PIC16C5X-RC PIC16C5X-HS PIC16C5X-LP	$V_{DD}$	3.0 3.0 4.5 2.5		6.25 6.25 5.5 6.25	V V V V	$F_{OSC} = \text{DC}$ to 4 MHz $F_{OSC} = \text{DC}$ to 4 MHz $F_{OSC} = \text{DC}$ to 20 MHz $F_{OSC} = \text{DC}$ to 40 kHz
<b>RAM Data Retention Voltage (Note 3)</b>	$V_{DR}$		1.5		V	Device in SLEEP mode
<b><math>V_{DD}</math> start voltage to guarantee Power-On Reset</b>	$V_{POR}$		$V_{SS}$		V	See Section 7.4 for details on Power-On Reset
<b><math>V_{DD}</math> rise rate to guarantee Power-On Reset</b>	$SV_{DD}$	0.05*			V/ms	See Section 7.4 for details on Power-On Reset
<b>Supply Current (Note 2)</b> PIC16C5X-XT PIC16C5X-RC (Note 5) PIC16C5X-HS PIC16C5X-LP	$I_{DD}$		1.8 1.8 4.8 9.0 15	3.3 3.3 10 20 32	mA mA mA mA $\mu\text{A}$	$F_{OSC} = 4\text{ MHz}$ , $V_{DD} = 5.5\text{V}$ $F_{OSC} = 4\text{ MHz}$ , $V_{DD} = 5.5\text{V}$ $F_{OSC} = 10\text{ MHz}$ , $V_{DD} = 5.5\text{V}$ $F_{OSC} = 20\text{ MHz}$ , $V_{DD} = 5.5\text{V}$ $F_{OSC} = 32\text{ kHz}$ , $V_{DD} = 3.0\text{V}$ , WDT disabled
<b>Power Down Current (Note 4)</b> PIC16C5X	$I_{PD}$		4 0.6	12 9	$\mu\text{A}$ $\mu\text{A}$	$V_{DD} = 3.0\text{V}$ , WDT enabled $V_{DD} = 3.0\text{V}$ , WDT disabled

\* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at  $25^{\circ}\text{C}$ . This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all  $I_{DD}$  measurements in active operation mode are:  
 $OSC1$  = external square wave, from rail to rail; all I/O pins tristated, pulled to  $V_{DD}$ ,  $T_{OCKI} = V_{DD}$ ,  
 $MCLR = V_{DD}$ ; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

3: This is the limit to which  $V_{DD}$  can be lowered in SLEEP mode without losing RAM data.

4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to  $V_{DD}$  and  $V_{SS}$ .

5: Does not include current through  $R_{EXT}$ . The current through the resistor can be estimated by the formula:  
 $I_R = V_{DD}/2R_{EXT}$  (mA) with  $R_{EXT}$  in kOhm.

**TABLE 9-3: DC CHARACTERISTICS: PIC16C5XI-RC, XT, HS, LP (INDUSTRIAL)**

DC Characteristics Power Supply Pins		Standard Operating Conditions Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise stated. Operating Voltage $V_{DD} = 3.5\text{V}$ to $5.5\text{V}$ , unless otherwise stated.				
Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
<b>Supply Voltage</b> PIC16C5XI-XT PIC16C5XI-RC PIC16C5XI-HS PIC16C5XI-LP	$V_{DD}$	3.0 3.0 4.5 2.5		6.25 6.25 5.5 6.25	V V V V	Fosc = DC to 4 MHz Fosc = DC to 4 MHz Fosc = DC to 20 MHz Fosc = DC to 40 kHz
<b>RAM Data Retention Voltage (Note 3)</b>	$V_{DR}$		1.5		V	Device in SLEEP mode
<b><math>V_{DD}</math> start voltage to guarantee Power-On Reset</b>	$V_{POR}$		$V_{SS}$		V	See Section 7.4 for details on Power-On Reset
<b><math>V_{DD}</math> rise rate to guarantee Power-On Reset</b>	$SV_{DD}$	0.05*			V/ms	See Section 7.4 for details on Power-On Reset
<b>Supply Current (Note 2)</b> PIC16C5XI-XT PIC16C5XI-RC (Note 5) PIC16C5XI-HS PIC16C5XI-LP	$I_{DD}$		1.8 1.8 4.8 9.0 19	3.3 3.3 10 20 40	mA mA mA mA $\mu\text{A}$	Fosc = 4 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 4 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 10 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 20 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 32 kHz, $V_{DD} = 3.0\text{V}$ , WDT disabled
<b>Power Down Current (Note 4)</b> PIC16C5XI	$I_{PD}$		5 0.6	14 12	$\mu\text{A}$ $\mu\text{A}$	$V_{DD} = 3.0\text{V}$ , WDT enabled $V_{DD} = 3.0\text{V}$ , WDT disabled

\* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at  $25^{\circ}\text{C}$ . This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all  $I_{DD}$  measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to  $V_{DD}$ ,  $TOCKI = V_{DD}$ ,  $MCLR = V_{DD}$ ; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

3: This is the limit to which  $V_{DD}$  can be lowered in SLEEP mode without losing RAM data.

4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to  $V_{DD}$  and  $V_{SS}$ .

5: Does not include current through  $R_{EXT}$ . The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{EXT}$  (mA) with  $R_{EXT}$  in kOhm.

**TABLE 9-4: DC CHARACTERISTICS: PIC16C5XE-RC, XT, HS, LP (AUTOMOTIVE)**

DC Characteristics Power Supply Pins		Standard Operating Conditions Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise stated. Operating Voltage $V_{DD} = 3.5\text{V}$ to $5.5\text{V}$ , unless otherwise stated.				
Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
<b>Supply Voltage</b> PIC16C5XE-XT PIC16C5XE-RC PIC16C5XE-HS PIC16C5XE-LP	$V_{DD}$	3.25 3.25 4.5 2.5		6.0 6.0 5.5 6.0	V V V V	Fosc = DC to 4 MHz Fosc = DC to 4 MHz Fosc = DC to 20 MHz Fosc = DC to 40 kHz
<b>RAM Data Retention Voltage (Note 3)</b>	$V_{DR}$		1.5		V	Device in SLEEP mode
<b><math>V_{DD}</math> Start Voltage to Guarantee Power-On Reset</b>	$V_{POR}$		$V_{SS}$		V	See Section 7.4 for details on Power-On Reset
<b><math>V_{DD}</math> rise rate to guarantee Power-On Reset</b>	$SV_{DD}$	0.05*			V/ms	See Section 7.4 for details on Power-On Reset
<b>Supply Current (Note 2)</b> PIC16C5XE-XT PIC16C5XE-RC (Note 5) PIC16C5XE-HS  PIC16C5XE-LP	$I_{DD}$		1.8 1.8 4.8 9.0 25	3.3 3.3 10 20 55	mA mA mA mA $\mu\text{A}$	Fosc = 4 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 4 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 10 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 16 MHz, $V_{DD} = 5.5\text{V}$ Fosc = 32 kHz, $V_{DD} = 3.25\text{V}$ , WDT disabled
<b>Power Down Current (Note 4)</b> PIC16C5XE	$I_{PD}$		5 0.8	22 18	$\mu\text{A}$ $\mu\text{A}$	$V_{DD} = 3.25\text{V}$ , WDT enabled $V_{DD} = 3.25\text{V}$ , WDT disabled

\* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at  $25^{\circ}\text{C}$ . This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all  $I_{DD}$  measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to  $V_{DD}$ ,  $T_{OCLK} = V_{DD}$ ,  $MCLR = V_{DD}$ ; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

3: This is the limit to which  $V_{DD}$  can be lowered in SLEEP mode without losing RAM data.

4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to  $V_{DD}$  and  $V_{SS}$ .

5: Does not include current through  $R_{ext}$ . The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{ext}$  (mA) with  $R_{ext}$  in kOhm.

**TABLE 9-5: DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (COMMERCIAL)  
PIC16C5XI-RC, XT, HS, LP (INDUSTRIAL)**

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions Operating Temperature -40°C ≤ TA ≤ +85°C (for industrial) 0°C ≤ TA ≤ +70°C (for commercial) Operating Voltage VDD range is described in Section 9.1 and Section 9.2.				
Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
<b>Input Low Voltage</b> I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	VSS VSS VSS VSS VSS		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance    PIC16C5X-RC only (Note 5) PIC16C5X-XT, HS, LP
<b>Input High Voltage</b> I/O ports  MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIH	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all VDD (Note 6) 4.0V < VDD ≤ 5.5V (Note 6) VDD > 5.5V    PIC16C5X-RC only (Note 5) PIC16C5X-XT, HS, LP
<b>Input Leakage Current (Notes 3,4)</b> I/O ports  MCLR MCLR T0CKI OSC1	IIL	-1 -5  -3 -3	0.5  0.5 0.5 0.5	+1 +5 +3 +3	μA μA μA μA	<b>For VDD ≤ 5.5V</b> VSS ≤ VPIN ≤ VDD, Pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD PIC16C5X-XT, HS, LP
<b>Output Low Voltage</b> I/O ports OSC2/CLKOUT (PIC16C5X-RC)	VOL			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V
<b>Output High Voltage</b> I/O ports (Note 4) OSC2/CLKOUT (PIC16C5X-RC)	VOH	VDD-0.7 VDD-0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V

- Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.
- 2: Total power dissipation as stated under absolute maximum ratings must not be exceeded.
- 3: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- 4: Negative current is defined as coming out of the pin.
- 5: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- 6: The user may use the better of the two specifications.

**TABLE 9-6: DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (AUTOMOTIVE)**

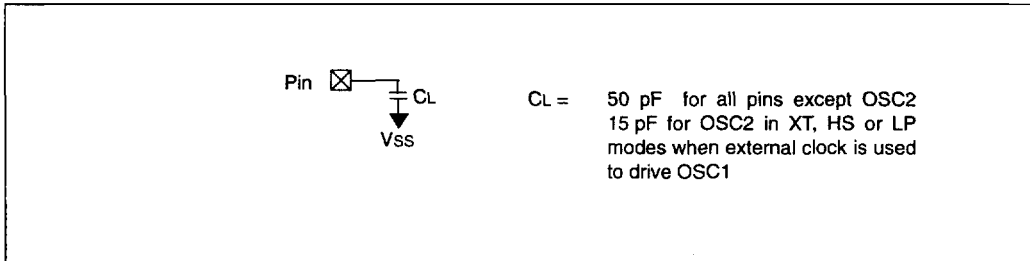
DC Characteristics		Standard Operating Conditions				
All Pins Except Power Supply Pins		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ Operating Voltage $V_{DD}$ range is described in Section 9.1 and Section 9.2.				
Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
<b>Input Low Voltage</b> I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	$V_{IL}$	$V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$		$0.15 V_{DD}$ $0.15 V_{DD}$ $0.15 V_{DD}$ $0.15 V_{DD}$ $0.3 V_{DD}$	V V V V V	Pin at hi-impedance    PIC16C5X-RC only (Note 5) PIC16C5X-XT, HS, LP
<b>Input High Voltage</b> I/O ports   MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	$V_{IH}$	$0.45 V_{DD}$ 2.0 $0.36 V_{DD}$ $0.85 V_{DD}$ $0.85 V_{DD}$ $0.85 V_{DD}$ $0.7 V_{DD}$		$V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$	V V V V V V V	For all $V_{DD}$ (Note 6) $4.0\text{V} < V_{DD} \leq 5.5\text{V}$ (Note 6) $V_{DD} > 5.5\text{V}$  PIC16C5X-RC only (Note 5) PIC16C5X-XT, HS, LP
<b>Input Leakage Current (Notes 3,4)</b> I/O ports  MCLR MCLR T0CKI OSC1	$I_{IL}$	-1  -5  -3 -3	0.5  0.5 0.5 0.5	+1  +5 +3 +3	$\mu\text{A}$  $\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	<b>For <math>V_{DD} \leq 5.5\text{V}</math></b> $V_{SS} \leq V_{PIN} \leq V_{DD}$ , Pin at hi-impedance $V_{PIN} = V_{SS} + 0.25\text{V}$ $V_{PIN} = V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$ PIC16C5X-XT, HS, LP
<b>Output Low Voltage</b> I/O ports OSC2/CLKOUT (PIC16C5X-RC)	$V_{OL}$			0.6 0.6	V V	$I_{OL} = 8.7\text{ mA}$ , $V_{DD} = 4.5\text{V}$ $I_{OL} = 1.6\text{ mA}$ , $V_{DD} = 4.5\text{V}$
<b>Output High Voltage</b> I/O ports (Note 4) OSC2/CLKOUT (PIC16C5X-RC)	$V_{OH}$	$V_{DD}-0.7$ $V_{DD}-0.7$			V V	$I_{OH} = -5.4\text{ mA}$ , $V_{DD} = 4.5\text{V}$ $I_{OH} = -1.0\text{ mA}$ , $V_{DD} = 4.5\text{V}$

Note 1: Data in the column labeled Typical is based on characterization results at  $25^{\circ}\text{C}$ . This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

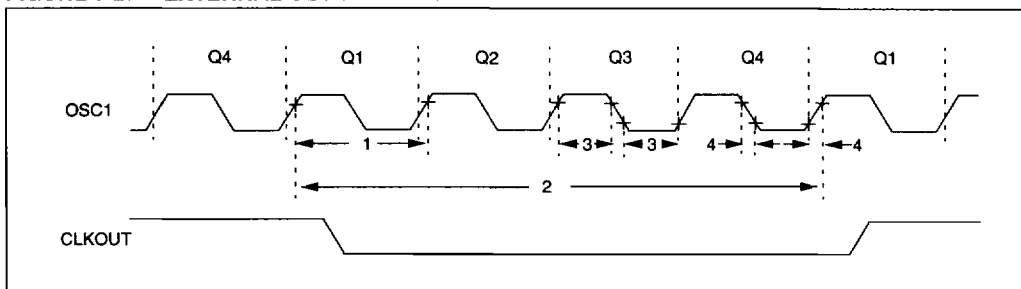
- Total power dissipation as stated under absolute maximum ratings must not be exceeded.
- The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- Negative current is defined as coming out of the pin.
- For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- The user may use the better of the two specifications.

## 9.2 Timing Diagrams and Specifications

**FIGURE 9-1: LOAD CONDITIONS**



**FIGURE 9-2: EXTERNAL CLOCK TIMING**



**TABLE 9-7: EXTERNAL CLOCK TIMING REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			DC	—	4	MHz	XT osc mode
			DC	—	20	MHz	HS osc mode (Comm/Indust)
			DC	—	16	MHz	HS osc mode (Automotive)
			DC	—	40	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode (Comm/Indust)
			4	—	16	MHz	HS osc mode (Automotive)
			5	—	40	kHz	LP osc mode
1	Tosc	External CLKIN Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			50	—	—	ns	HS osc mode
			100	—	—	μs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			62.5	—	250	ns	HS osc mode (Comm/Indust)
			50	—	250	ns	HS osc mode (Automotive)
2	Tcy	Instruction Cycle Time (Note 1)	1.0	—	DC	μs	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	25	—	—	ns	XT oscillator
			50	—	—	ns	LP oscillator
			15	—	—	ns	HS oscillator

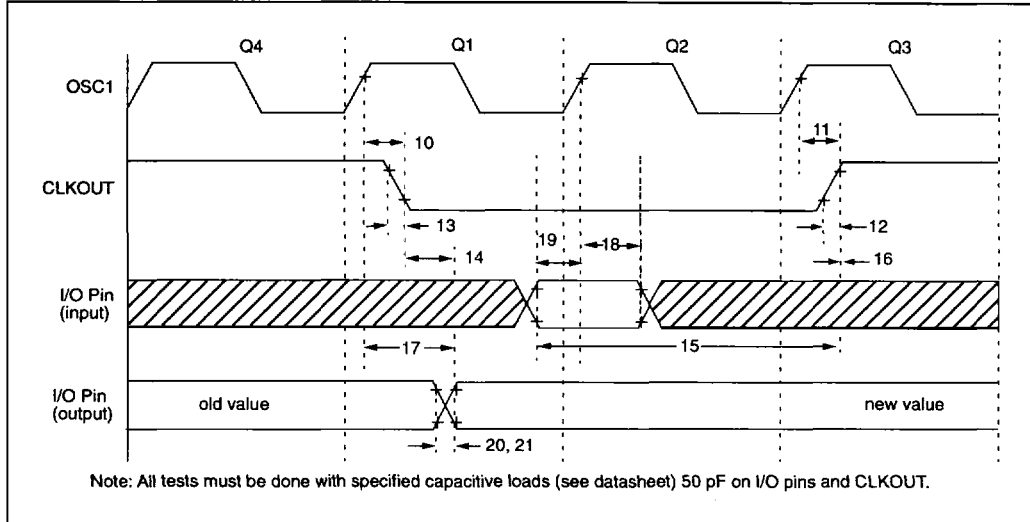
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.

When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.



**FIGURE 9-3: CLKOUT AND I/O TIMING**



**TABLE 9-8: CLKOUT AND I/O TIMING REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	Note 1
12	TckR	CLKOUT rise time	—	5	15	ns	Note 1
13	TckF	CLKOUT fall time	—	5	15	ns	Note 1
14	TckL2ioV	CLKOUT↓ to Port out valid	—	—	0.5 TCY+20	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	0.25 TCY+25	—	—	ns	Note 1
16	TckH2ioI	Port in hold after CLKOUT↑	0	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	80 - 100	ns	Note 2
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns	
20	TioR	Port output rise time	—	10	25	ns	Note 2
21	TioF	Port output fall time	—	10	25	ns	Note 2

\* These parameters are characterized but not tested.

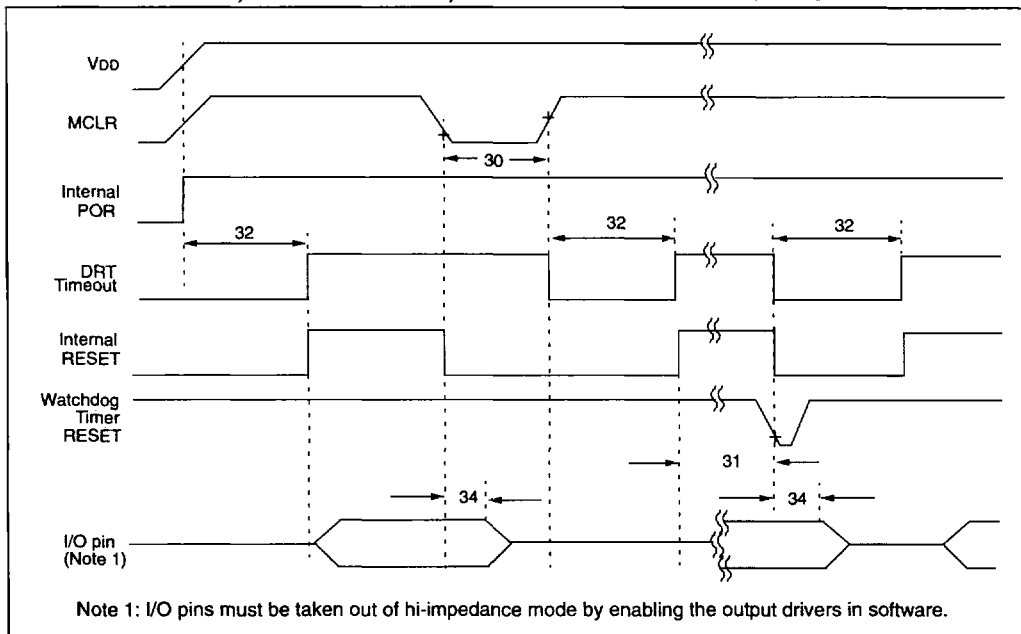
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: See Figure 9-1 for loading conditions.

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**FIGURE 9-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING**



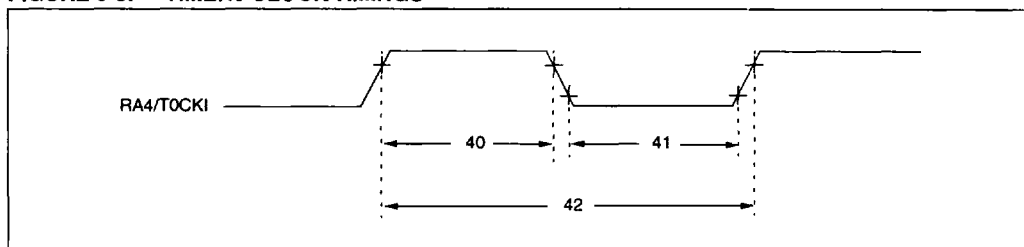
**TABLE 9-9: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +125°C
31	Twdt	Watchdog Timer Timeout Period (No Prescaler)	9*	18	30*	ms	VDD = 5V, -40°C to +125°C
32	TDRT	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low			100	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 9-5: TIMER0 CLOCK TIMINGS**



**TABLE 9-10: TIMER0 CLOCK REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 Tcy + 20*	—	ns	
			With Prescaler	10*	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 Tcy + 20*	—	ns	
			With Prescaler	10*	—	ns	
42	Tt0P	T0CKI Period	$\frac{Tcy + 40}{N}$ *		—	ns	N = prescale value (1, 2, 4, ..., 256)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.