10. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Test condition	Rating	Unit
Power supply voltage	V_{DD}		-0.3 to +7.0	V
Input voltage	V_I		-0.3 to V_{DD}+0.3	V
Output voltage	V_O		-0.3 to V_{DD}+0.3	V
Operation temperature	T_{opt}		-10 to +70	xC
Storage temperature	T_{stg}		-65 to +150	xC

DC Characteristics (Ta=-10 to +70°C, V_{DD}=5V±10%)

Parameter	Symbol	Test condition	MIN	TYP	MAX	Unit
Input high voltage	V_{IH1}	Except for SCK	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	SCK	$0.8V_{DD}$		V_{DD}	V
Input low voltage	V_{IL}		0		$0.3V_{DD}$	V
Input high leakage current	I_{LIH}	V_I=V_{DD}			10	uA
Input low leakage current	I_{LIL}	V=0V			-10	uA
Output high voltage	V_{OH1}	BUSY,D0-D3 I_{HO}=-400uA	V_{DD}-0.5			V
	V_{OH2}	SYNC, I_{OH}=-100uA	V_{DD}-0.5			V
Output low voltage	V_{OL1}	BUSY,D0-D3 I_{OL}=1.7mA			0.45	V
	V_{OL2}	SYNC, I_{OL}=100uA			0.45	V
Output high leakage current	I_{LOH}	V_O=V_{DD}			10	uA
Output low leakage current	I_{LOL}	V_I=0V			-10	uA
LCD drive voltage	V_{LCD}		3.0		V_{DD}	V
Row output impedance	R_{ROW}			4	8	k
Row/column output impedance	$R_{ROW/COL}$			5	10	k

Column output impedance	R_{COL}		10	15	k
Power supply current	I_{DDI}	Operation mode, f_C=400kHz	200	400	uA
	I_{DD2}	STOP mode, CLK=0V		20	uA

Capacitance (T_a=25°C, V_{DD}=0V)

Parameter	Symbol	Test condition	MIN	TYP	MAX	Unit
Input capacitance	C_{IN}	f=1MHz Unmeasured pins returned to 0V			10	pF
Output capacitance	C_{OUT}				25	pF
Input/output capacitance	C_{IO}				15	pF

AC Characteristics (Ta=-10 to +70°C, V_{DD}=+5V±10%)

Common operation:

Parameter	Symbol	Test condition	MIN	TYP	MAX	Unit
Clock operation frequency	f_{TC}		100		1100	kHz
High clock pulse width	t_{WHC}		350			ns
Low clock pulse width	t_{WLC}		350			ns
RESET high width	t_{HRS}		4			us
$\overline{CS}$↓–$\overline{BUSY}$ delay time	t_{DCSB}	C_L=50pF			2	us
$\overline{CS}$↑–$\overline{BUSY}$ float delay time	t_{DCSBF}	C_L=50pF			4	us
$\overline{CS}$ high width	t_{WHCS}		4			us
SYNC load capacitance	C_{LSY}				100	pF
Data setup time to RESET↓	t_{SDR}		0			us
Data hold time from RESET↓	t_{HRD}		4			us

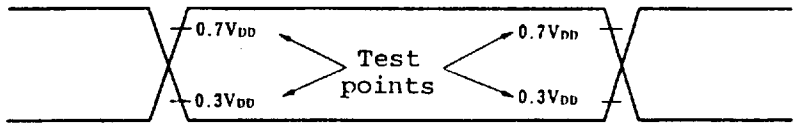
Serial Input/Output Operation:

Parameter	Symbol	Test condition	MIN	TYP	MAX	Unit
$\overline{SCK}$ period	t_{CYK}		0.9			us
High $\overline{SCK}$ pulse width	t_{WHK}		400			ns
Low $\overline{SCK}$ pulse width	t_{WLK}		400			ns
High $\overline{SCK}$ hold time from $\overline{BUSY}$ ↑	t_{HBK}		0			ns
SI setup time to $\overline{SCK}$ ↑	t_{SIK}		100			ns
SI hold time from $\overline{SCK}$ ↑	t_{HKI}		250			ns
$\overline{SCK}$ ↓-SO delay time	t_{DKO}	C_L=50pF			320	ns
Eighth $\overline{SCK}$ ↓-$\overline{BUSY}$ delay time	C_{DKB}	C_L=50pF			3	us
$\overline{BUSY}$ low time	t_{WLB}	C_L=50pF	18		64	$1/f_C$
C/$\overline{D}$ setup time to first $\overline{SCK}$ ↑	t_{SDK}		0			us
C/$\overline{D}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKD}		2			us
$\overline{CS}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKCS}		2			us

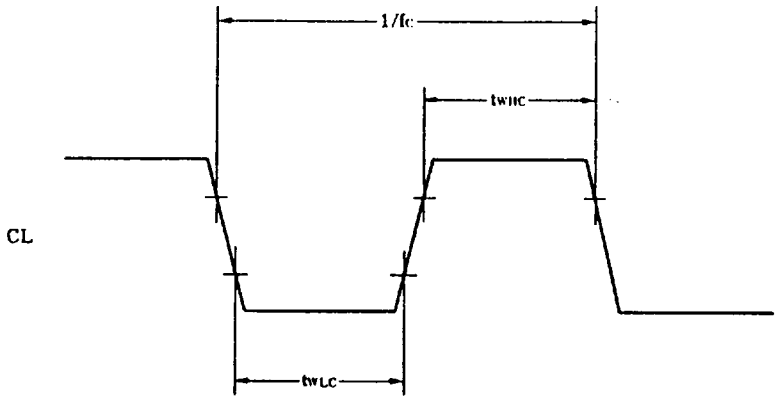
Parallel Input/Output Operation:

Parameter	Symbol	Test condition	MIN	TYP	MAX	Unit
Command input setup time to $\overline{STB}\downarrow$	t_A	C_L=80pF	100			ns
Command input hold time from $\overline{STB}\downarrow$	t_B	C_L=20pF	90			ns
Data input setup time to $\overline{STB}\downarrow$	t_C	C_L=80pF	230			ns
Data input hold time from $\overline{STB}\downarrow$	t_D	C_L=20pF	50			ns
Data output delay time	t_{ACC}	C_L=80pF	90		650	ns
Data output hold time	t_H	C_L=20pF	0		150	ns
$\overline{STB}$ pulse width	t_{SL}		700			ns
$\overline{STB}$ high time	t_{SH}		1			us
High $\overline{STB}$ hold time from $\overline{BUSY}\downarrow$	t_{HBS}		0			us
Second $\overline{STB}\downarrow$-$\overline{BUSY}\downarrow$ delay time	t_{DSB}				3	us
$\overline{BUSY}$ low time	t_{WLB}	C_L=50pF	18		64	$1/f_C$
C/$\overline{D}$ setup time to first $\overline{STB}\downarrow$	t_{SDS}		0			us
C/$\overline{D}$ hold time from second $\overline{STB}\downarrow$	t_{HSD}		2			us
$\overline{CS}$ hold time from second $\overline{STB}\downarrow$	t_{HSCS}		2			us

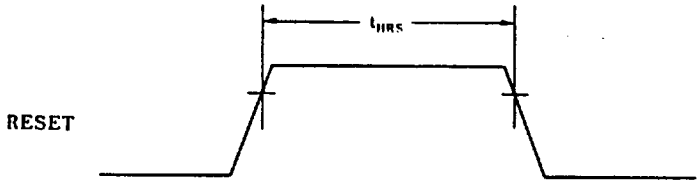
AC timing measurement voltages (except for $\overline{STB}$/$\overline{SCK}$ or $\overline{BUSY}$)



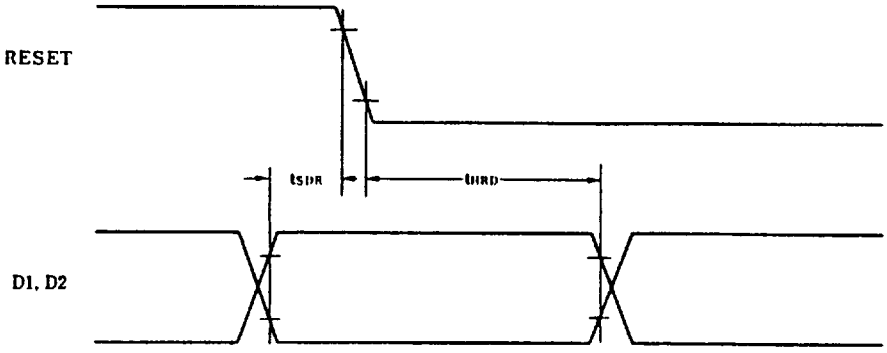
Clock timing



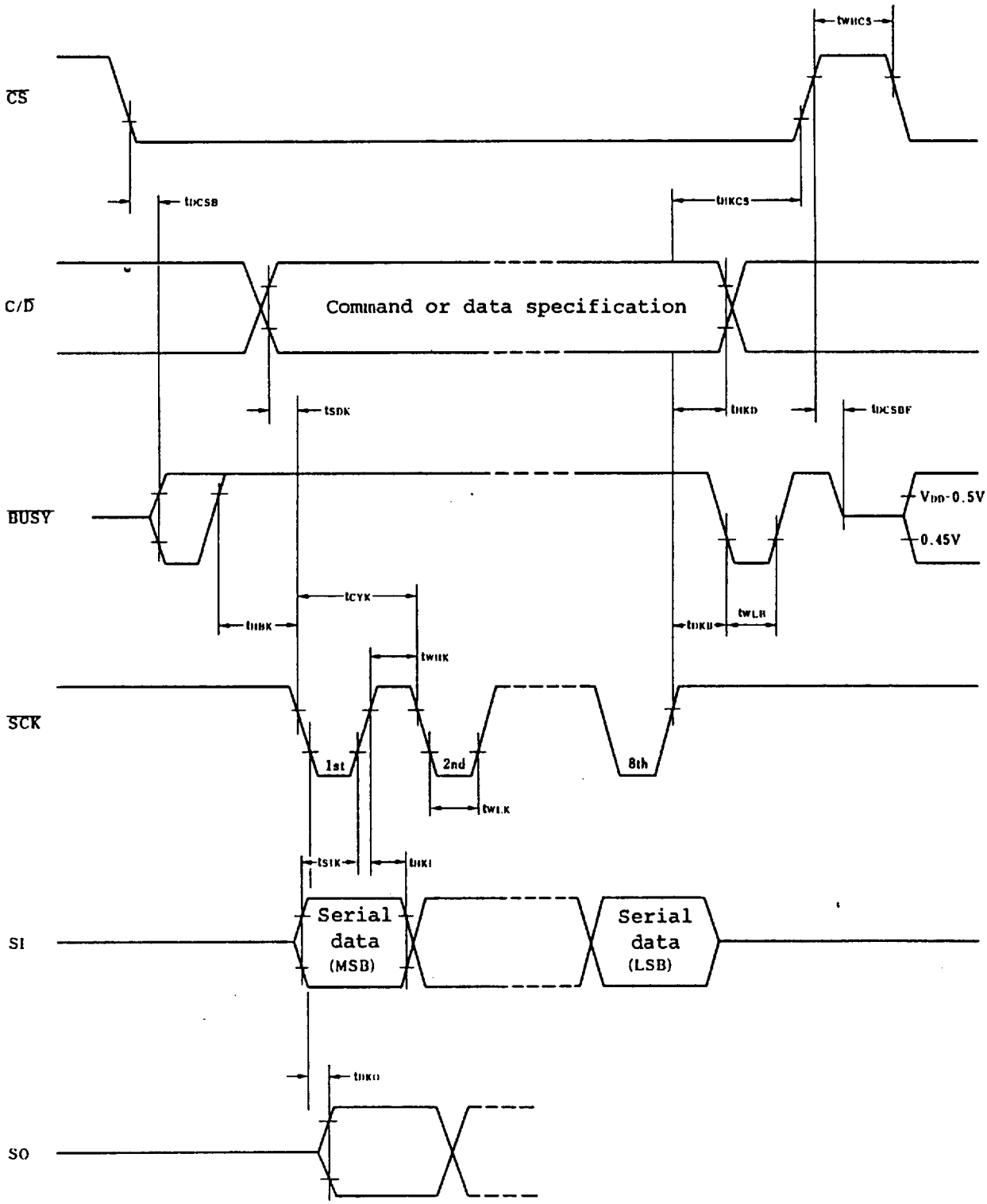
RESET input timing



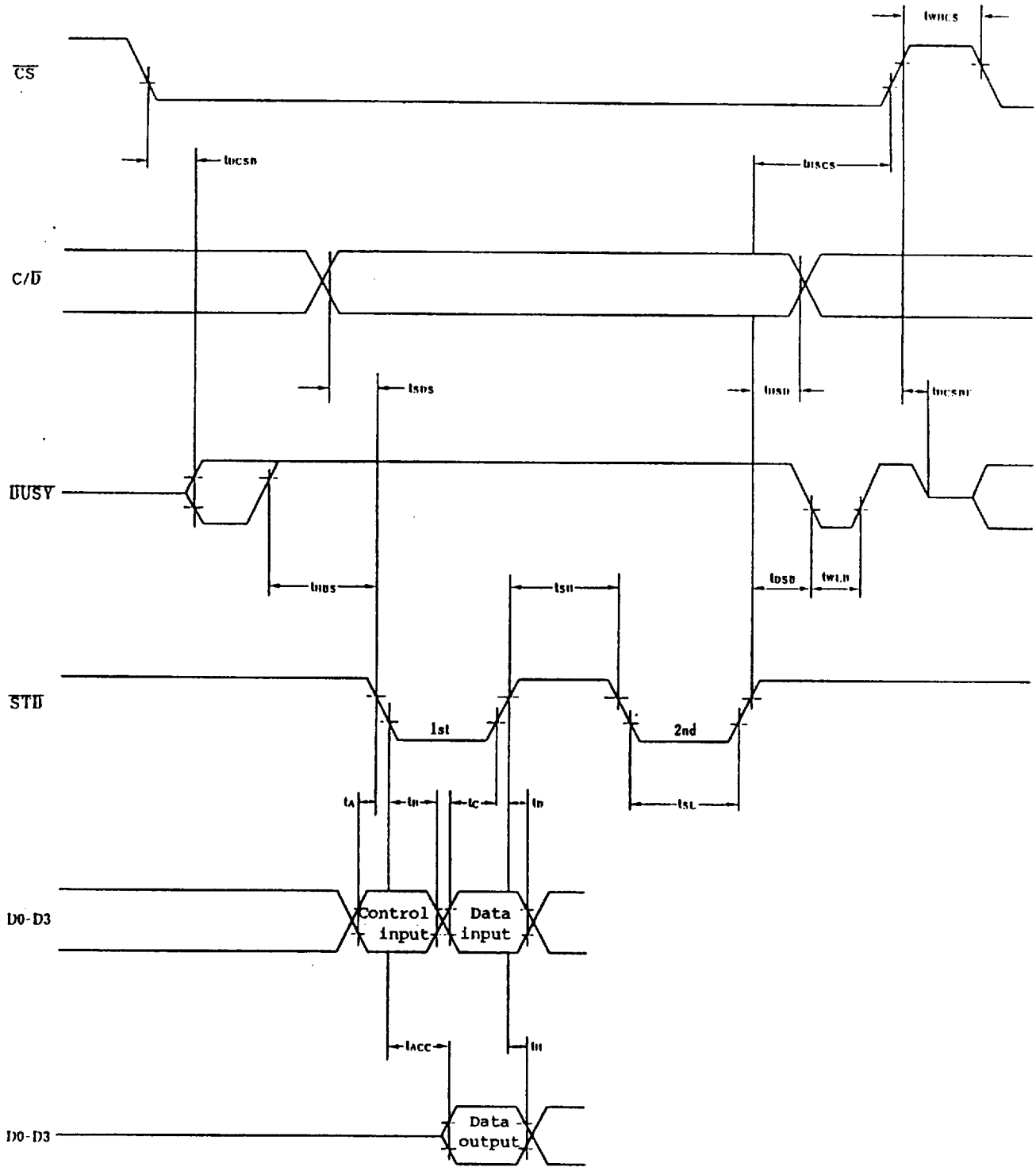
Interface specification timing



Serial input/output timing



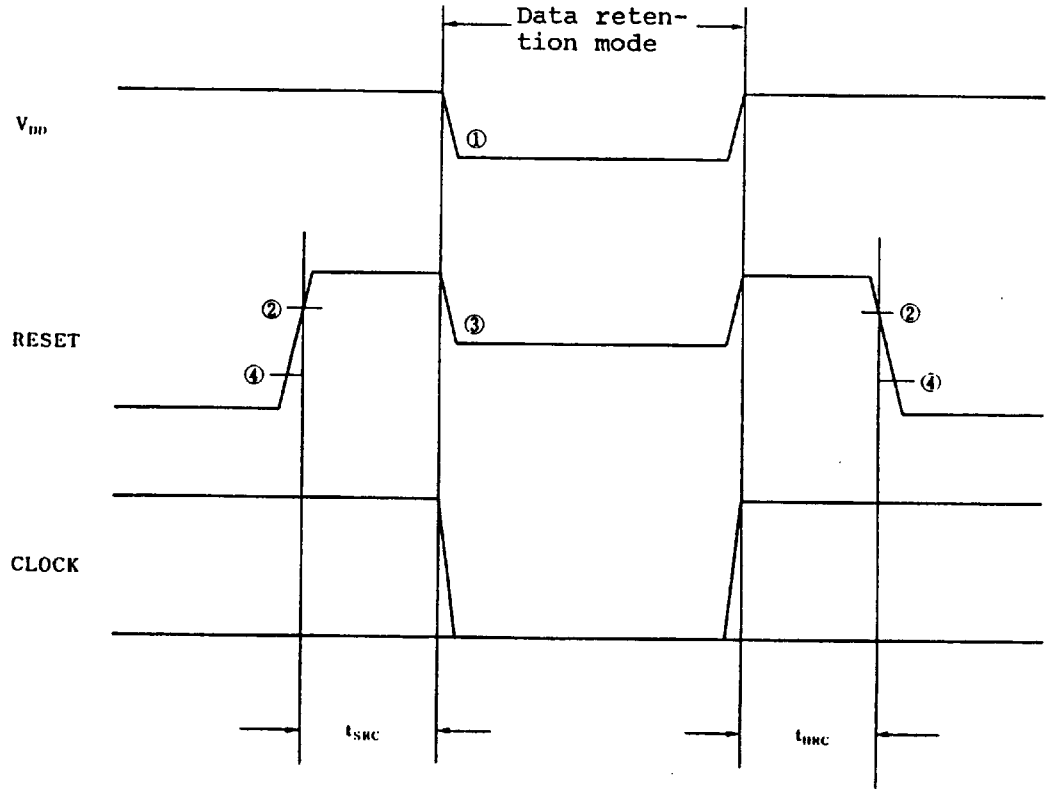
Parallel input/output timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Ta=-10 to +70°C)

Parameter	Symbol	Test condition	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}		2.0			V
Data retention supply current	I_{DDDR}	V_{DDDR}=2.0V			20	uA
Data retention high RESET input voltage	V_{IHDR}		$0.9V_{DDDR}$		V_{DDDR}-0.2	V
RESET, CLOCK setup time	t_{SRC}		10			us
RESET, CLOCK hold time	t_{HRC}		10			us

Data retention timing

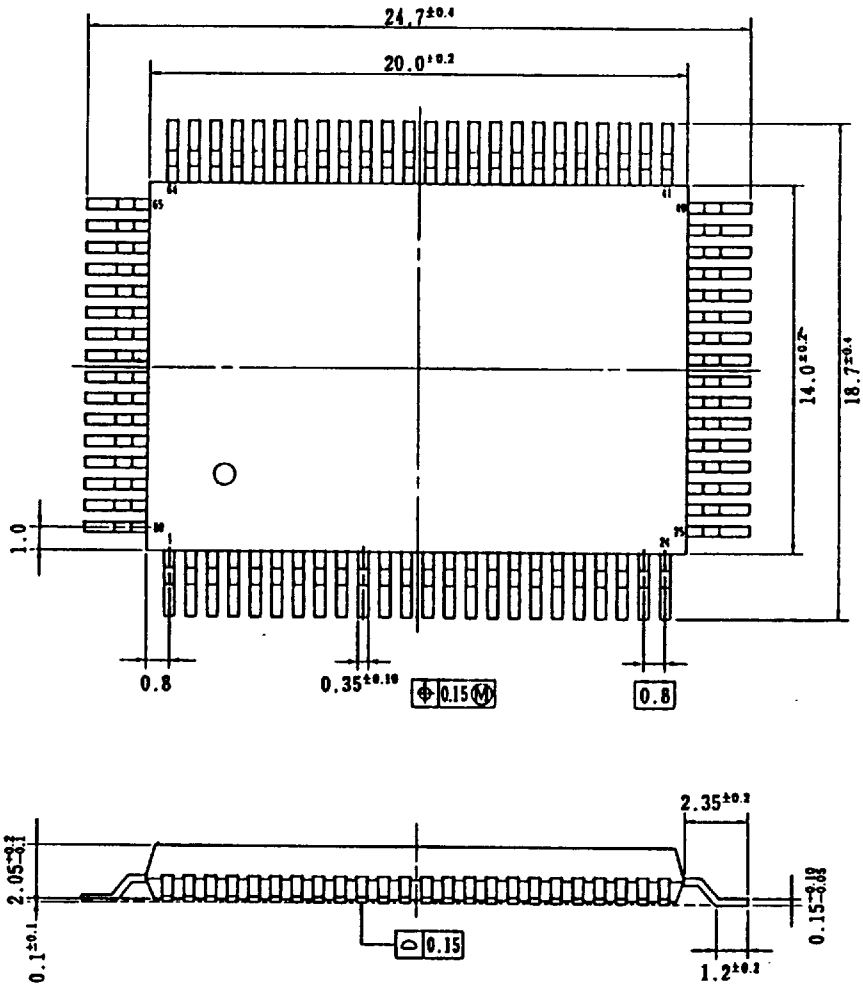


① V_{DDDR}
② V_{IHI}
③ V_{IHIDR}
④ V_{IL}

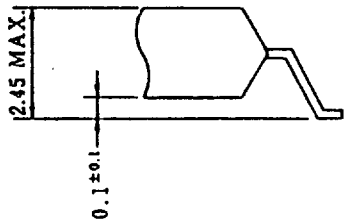
Caution: In the data retention mode, set all inputs to V_{DDDR} or less.

11. PACKAGE DIMENSION

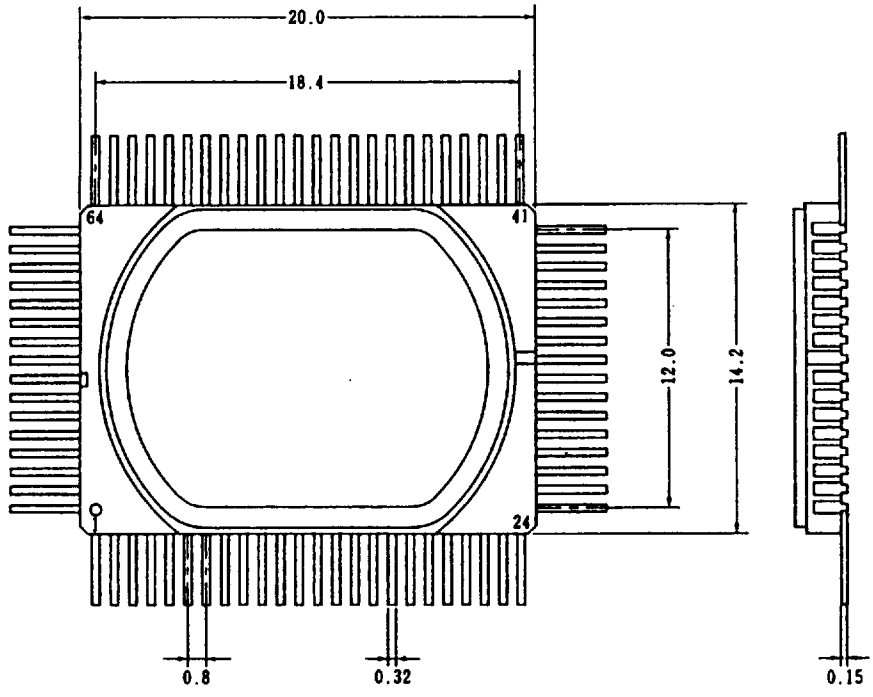
80-pin Plastic Quad-flat Package Dimension (unit: mm)

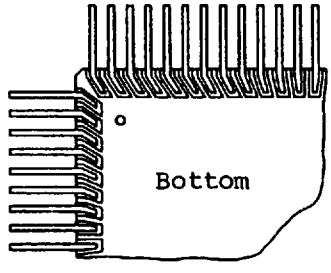


The pin edge configuration



ES 80-pin Ceramic Flat Package (for reference) (unit: mm)





Cautions:

1. Note that the metal cap that is connectedto pin 33 becomes the positive power supply level.
2. Note that bottom leads are formed aslant.
3. Since lead tip cut work is not processcontrolled, the lead length is not defined.