2-Input NOR Gate / CMOS Logic Level Shifter

with LSTTL–Compatible Inputs

MC74VHC1GT02

The MC74VHC1GT02 is a single gate 2–input NOR fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

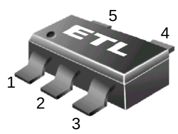
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high–voltage power supply.

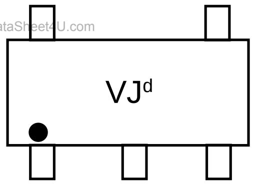
The MC74VHC1GT02 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT02 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: tPD = 4.7 ns (Typ) at VCC = 5 V
- Low Power Dissipation: ICC = 2 mA (Max) at TA = 25°C
- TTL–Compatible Inputs: VIL = 0.8 V; VIH = 2.0 V
- CMOS–Compatible Outputs: VOH > 0.8 VCC ; VOL < 0.1 VCC @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 65; Equivalent Gates = 14

MARKING DIAGRAMS



SC–88A / SOT–353/SC–70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code

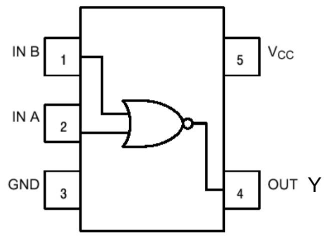
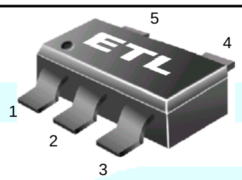
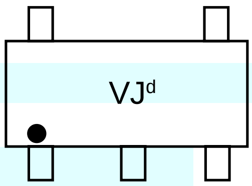


Figure 1. Pinout (Top View)



TSOP–5/SOT–23/SC–59
DT SUFFIX
CASE 483



Pin 1
d = Date Code

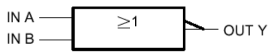


Figure 2. Logic Symbol

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1GT02

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage		– 0.5 to 7.0	V
V_{OUT}	DC Output Voltage	V_{CC}=0	– 0.5 to 7.0	V
		High or Low State	–0.5 to V_{CC} + 0.5	
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+ 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air	SC–88A, TSOP–5	200	mW
θ_{JA}	Thermal resistance	SC–88A, TSOP–5	333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2)	>2000	V
		Machine Model (Note 3)	> 200	
		Charged Device Model (Note 4)	N/A	
$I_{LATCH-UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		3.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage	V_{CC} = 0	0.0	5.5	V
		High or Low State	0.0	V_{CC}	
T_A	Operating Temperature Range		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3 ± 0.3 V	0	100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0	20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

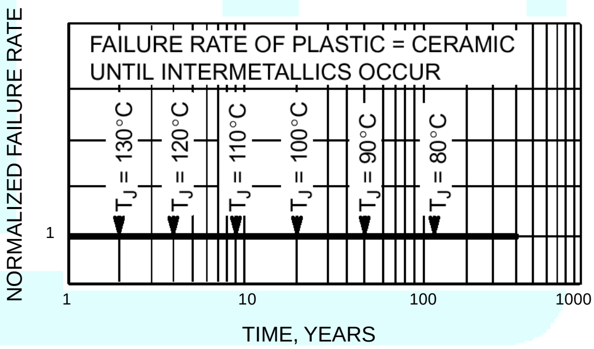


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \leq$ 85°C Min	$T_A \leq$ 85°C Max	−55°C ≤ T_A ≤ 125°C Min	−55°C ≤ T_A ≤ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = – 50 µA	3.0 4.5	2.9 4.4	3.0 4.0		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = –4 mA I_{OH} = –8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 50 µA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	µA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	µA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input $t_r = t_f$ = 3.0 ns

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \leq$ 85°C Min	$T_A \leq$ 85°C Max	−55°C ≤ T_A ≤ 125°C Min	−55°C ≤ T_A ≤ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Y	V_{CC} = 3.3± 0.3 V	C_L = 15 pF C_L = 50 pF		4.0 5.8	10.0 13.5		11.0 15.0		13.0 17.5	ns
		V_{CC} = 5.0± 0.5 V	C_L = 15 pF C_L = 50 pF		3.0 3.8	6.7 7.7		7.5 8.5		8.5 9.5	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}{}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

MC74VHC1GT02

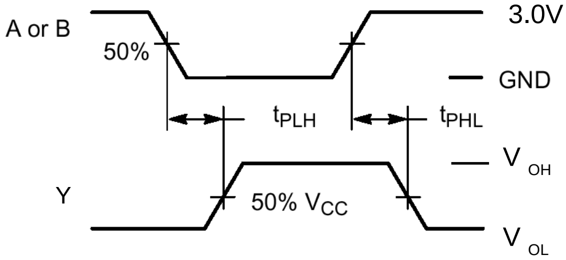
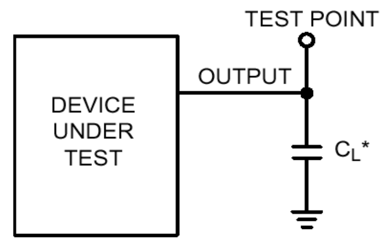


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT02DFT1	MC	74	VHC1G	T02	DF	T1	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
MC74VHC1GT02DFT2	MC	74	VHC1G	T02	DF	T2	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
MC74VHC1GT02DFT4	MC	74	VHC1G	T02	DF	T4	SC–70/SC–88A/ SOT–353	330 mm (13 in) 10,000 Unit
MC74VHC1GT02DTT1	MC	74	VHC1G	T02	DT	T1	SOT–23/TSOPS/ SC–59	178 mm (7 in) 3000 Unit
MC74VHC1GT02DTT3	MC	74	VHC1G	T02	DT	T3	SOT–23/TSOPS/ SC–59	330 mm (13 in) 10,000 Unit