August 1994
Edition 1.0

FUJITSU

DATA SHEET

MB81141623-010/-012/-015
CMOS 2 x 128K x 16 SYNCHRONOUS DRAM

CMOS 2 BANKS OF 131,072-WORDS x 16-BIT SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

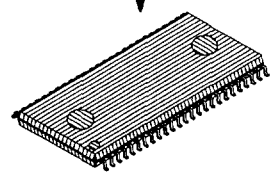
PRELIMINARY

The Fujitsu MB81141623 is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) containing 4,194,304 memory cells accessible in an 16-bit format. The MB81141623 features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81141623 SDRAM is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints, and may improve data bandwidth of memory as much as 5 times more than a standard DRAM.

The MB81141623 is ideally suited for supercomputers, workstations, laser printers, high resolution graphic adapters, accelerators and other applications where an extremery large memory and bandwidth are required and where a simple interface is needed.

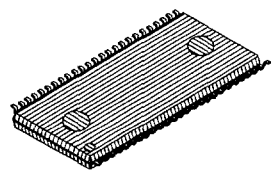
The MB81141623 has a special burst mode, down cownt, that is usefull for accelerating reverse BITBLT at graphics application.

Marking side



FPT–50P–M01
(Normal Bend)

Marking side



FPT–50P–M02
(Reverse Bend)

Plastic TSOP Packages

PRODUCT LINE & FEATURES

Parameters	MB81141623-010	MB81141623-012	MB81141623-015
Clock Frequency	100 MHz max	80 MHz max	67 MHz max
Burst Mode Cycle Time	10 ns min	12 ns min	15 ns min
$\overline{RAS}$ Access Time	58 ns max	67 ns max	75 ns max
$\overline{CAS}$ Access Time	28 ns max	32 ns max	35 ns max
Output Valid From Clock (CL=3)	8 ns max	9 ns max	10 ns max
Operating Current (Two banks active)	130mA max	120mA max	110mA max
Power Down Mode Current	1mA max		

- Single +3.3V Supply ±10% tolerance
- LVTTL compatible I/O
- 1,024 refresh cycles every 16.4 ms
- Dual bank operation
- Down count burst mode capability
- Programmable burst length
- Programmable CAS latency
- Auto and Self–refresh
- CKE power down mode
- Output Enable and Input Data Mask

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameters	Symbol	Value	Unit
Voltage of VCC supply relative to VSS	VCC	–0.5 to +4.6	V
Voltage at any pin relative to VSS	VIN/VOUT	–0.5 to +4.6	V
Short Circuit Output Current	IOUT	±50	mA
Power Dissipation	PD	1.3	W
Storage Temperature	TSTG	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package and Ordering Information

– 50–pin plastic (400mil) TSOP–II with normal bend leads, order as MB81141623–xxxPFTN

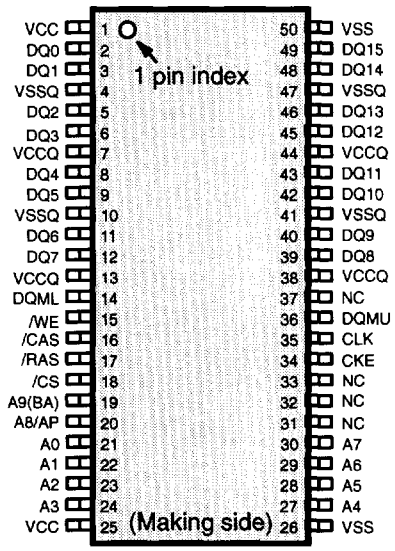
– 50–pin plastic (400mil) TSOP–II with reverse bend leads, order as MB81141623–xxxPFTR

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJMS1131

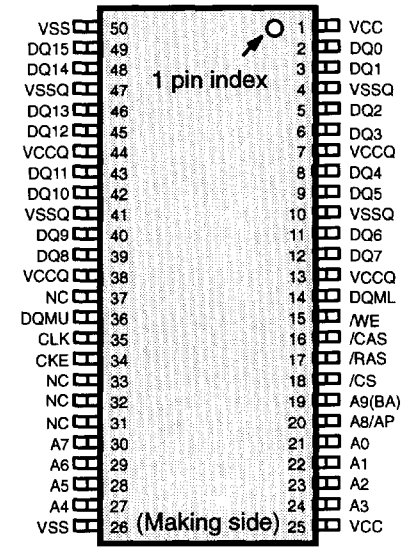
PIN ASSIGNMENTS AND DESCRIPTIONS

<Normal Bend : FPT–50P–Mxx>



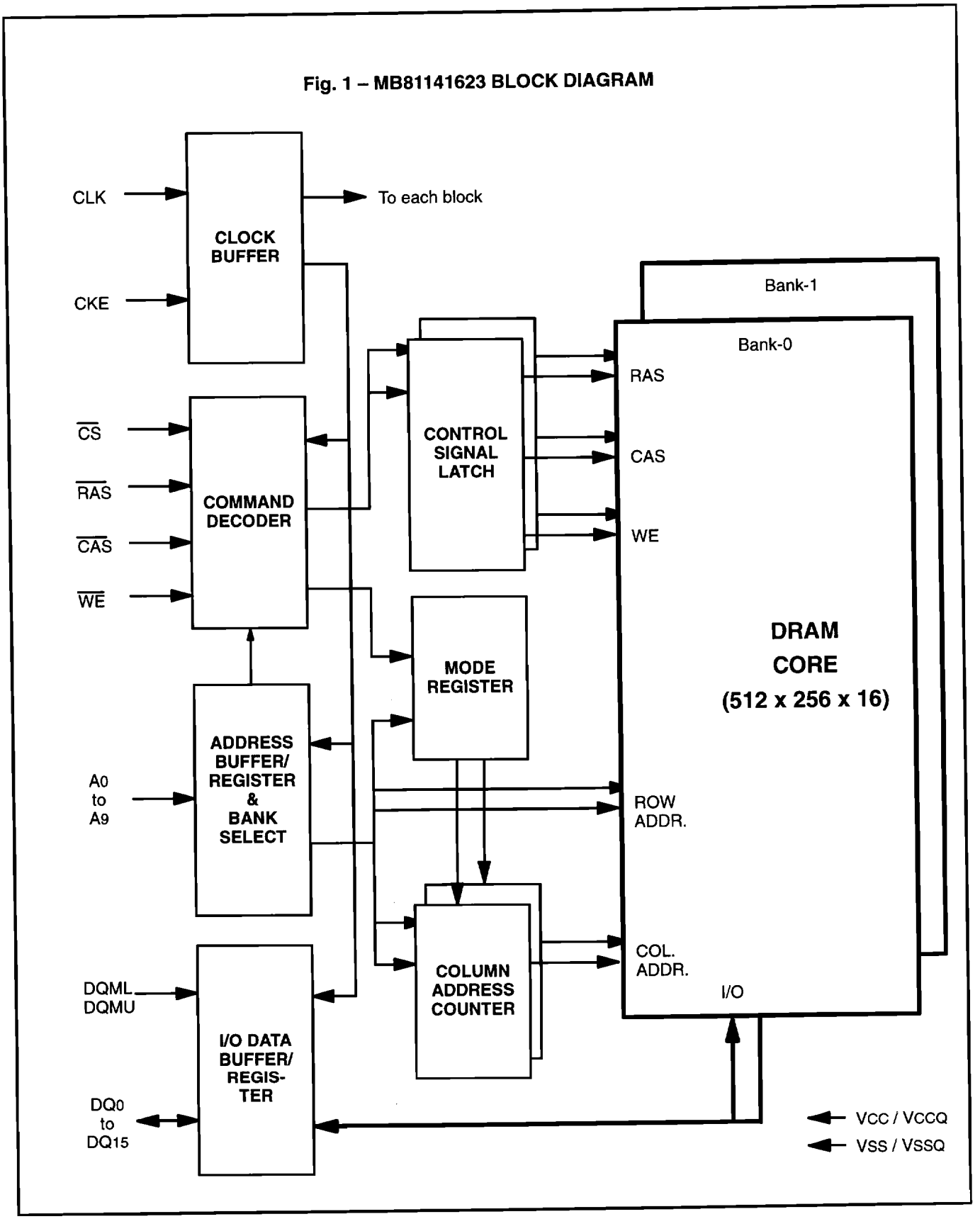
50–Pin TSOP
(TOP VIEW)

<Reverse Bend : FPT–50P–Mxx>



Pin Number	Symbol	Description
1, 7, 13, 25, 38, 44	VCC, VCCQ	Supply Voltage
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0 to DQ15	Data I/O
4, 10, 26, 41, 47, 50	VSS, VSSQ	Ground
14, 36	DQML, DQMU	Input/Output Mask
15	$\overline{WE}$	Write Enable
16	$\overline{CAS}$	Column Address Strobe
17	$\overline{RAS}$	Row Address Strobe
18	$\overline{CS}$	Chip Select
19	A9 (BA)	Bank Select
20	AP	Auto Precharge Enable
20, 21, 22, 23, 24, 27, 28, 29, 30	A0 to A7, A8	Address Input • Row :A0 to A8 • Column :A0 to A7
31, 32, 33	NC	No Connection
34	CKE	Clock Enable
35	CLK	Clock Input
37	NC	No Connection

Fig. 1 – MB81141623 BLOCK DIAGRAM



FUNCTION TRUTH TABLE

COMMAND TRUTH TABLE

Function	Notes	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7–A0
			n–1	n							
Device Deselect	5	DESL	H	X	H	X	X	X	X	X	X
No Operation	5	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	6	BST	H	X	L	H	H	L	X	X	X
Read	7	READ	H	X	L	H	L	H	V	L	V
Read With Auto Precharge	7	READA	H	X	L	H	L	H	V	H	V
Write	7	WRIT	H	X	L	H	L	L	V	L	V
Write With Auto Precharge	7	WRITA	H	X	L	H	L	L	V	H	V
Bank Active (RAS)	8	ACTV	H	X	L	L	H	H	V	V	V
Precharge Single Bank		PRE	H	X	L	L	H	L	V	L	X
Rrecharge All Banks		PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	9, 10	MRS	H	X	L	L	L	L	V	L	V

Note:

1. V = Valid, L = Logic Low, H = Logic High, X = either L or H.
2. All commands assumes no CSUS command on previous rising edge of clock.
3. All commands are assumed to be valid state transitions.
4. All inputs are latched on the rising edge of clock.
5. NOP and DESL commands have the same effect on the part.
6. BST command is effective only during full colmun burst read or write.
7. READ, READA, WRIT, and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to STATE DIAGRAM.
8. ACTV command should only be issued after corresponding bank has been precharged (PRE or PALL command).
9. Required after power up.
10. MRS command should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.

FUNCTION TRUTH TABLE ... Continued

DQM TRUTH TABLE

Function	Symbol	CKE		DQMU	DQML
		n–1	n		
Upper Byte Write Enable / Output Enable	ENBU	H	X	L	X
Lower Byte Write Enable / Output Enable	ENBL	H	X	X	L
Upper Byte Data Mask / Output Disable	MASKU	H	X	H	X
Lower Byte Data Mask / Output Disable	MASKL	H	X	X	H

CKE TRUTH TABLE

Current State	Function	Notes	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr
				n–1	n					
Bank Active	Clock Suspend Mode Entry	1	CSUS	H	L	X	X	X	X	X
Any	Clock Suspend Continue	1		L	L	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit			L	H	X	X	X	X	X
Idle	Auto–refresh Command	2	REF	H	H	L	L	L	H	X
Idle	Self–refresh Entry	2	SELF	H	L	L	L	L	H	X
Self Refresh	Self–refresh Exit		SELFX	L	H	L	H	H	H	X
				L	H	H	X	X	X	X
Idle	Power Down Entry	2	PD	H	L	L	H	H	H	X
				H	L	H	X	X	X	X
Power Down	Power Down Exit			L	H	L	H	H	H	X
				L	H	H	X	X	X	X

Note: 1. The CSUS command requires that at least one bank is active. Refer to STATE DIAGRAM.
2. REF, SELF and PD commands should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.

OPERATION COMMAND TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Symbol	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	X	X	NOP/BST	NOP	
	L	H	L	H	BA, CA, A8	READ/READA	Illeagal	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Illeagal	
	L	L	H	H	BA, RA	ACTV	Bank Active after tRCD	

FUNCTION TRUTH TABLE ... Continued

OPERATION COMMAND TABLE ... Continued

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Symbol	Function	Notes
Idle	L	L	H	L	BA, A8	PRE/PALL	NOP	
	L	L	L	H	X	REF/SELF	Auto–refresh or Self–refresh	
	L	L	L	L	MODE	MRS	Mode Register Set –> Idle	
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	X	X	NOP/BST	NOP	
	L	H	L	H	BA, CA, A8	READ/READA	Begin Read : Determine AP	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Begin Write : Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	Precharge	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End –> Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End –> Bank Active)	
	L	H	H	L	X	BST	Burst Stop –> Bank Active	
	L	H	L	H	BA, CA, A8	READ/READA	Terminate Burst, New Read : Determine AP	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Terminate Burst, Start Write : Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	Terminate Burst, Precharge	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

FUNCTION TRUTH TABLE ... Continued

OPERATION COMMAND TABLE ... Continued

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Symbol	Function	Notes
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End –> Write Recovering –> Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End –> Write Recovering –> Bank Active)	
	L	H	H	L	X	BST	Burst Stop –> Write Recovering –> Bank Active	
	L	H	L	H	BA, CA, A8	READ/READA	Terminate Burst, Start Read : Determine AP	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Terminate Burst, New Write : Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	Terminate Burst, Precharge	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Read With Auto Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End –> Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End –> Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, A8	READ/READA	Illegal	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE, PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

FUNCTION TRUTH TABLE ... Continued

OPERATION COMMAND TABLE ... Continued

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Symbol	Function	Notes
Write With Auto Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Write Recovering and Precharge -> Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Write Recovering and Precharge -> Idle)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, A8	READ/READA	Illegal	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Precharge	H	X	X	X	X	DESL	NOP (Idle after tRP)	
	L	H	H	H	X	NOP	NOP (Idle after tRP)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, A8	READ/READA	Illegal	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	NOP (PALL may affect other bank)	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

FUNCTION TRUTH TABLE ... Continued

OPERATION COMMAND TABLE ... Continued

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Symbol	Function	Notes
Bank Activating	H	X	X	X	X	DESL	NOP (Row Active after tRCD)	
	L	H	H	H	X	NOP	NOP (Bank Active after tRCD)	
	L	H	H	L	X	BST	NOP (Bank Active after tRCD)	
	L	H	L	H	BA, CA, A8	READ/READA	Illegal	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write Recovering	H	X	X	X	X	DESL	NOP (Bank Active after tWR)	
	L	H	H	H	X	NOP	NOP (Bank Active after tWR)	
	L	H	H	L	X	BST	NOP (Bank Active after tWR)	
	L	H	L	H	BA, CA, A8	READ/READA	Start Read, Determine AP	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	New Write, Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE, PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

FUNCTION TRUTH TABLE ... Continued

OPERATION COMMAND TABLE ... Continued

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Symbol	Function	Notes
Write Recovering at Auto Precharge	H	X	X	X	X	DESL	NOP (Precharge after tWR)	
	L	H	H	H	X	NOP	NOP (Precharge after tWR)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, A8	READ/READA	Illegal	
	L	H	L	L	BA, CA, A8	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, A8	PRE/PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after tRC)	
	L	H	H	X	X	NOP/BST	NOP (Idle after tRC)	
	L	H	L	X	X	READ/READA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF MRS	Illegal	
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after 2 clocks)	
	L	H	H	H	X	NOP	NOP (Idle after 2 clocks)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA	Illegal	
	L	L	X	X	X	ACTV PRE/PALL REF/SELF MRS	Illegal	

FUNCTION TRUTH TABLE ... Continued

COMMAND TRUTH TABLE FOR CKE

Current State	CKE n–1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Notes
Self Refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self Refresh, Idle after tRC	
	L	H	L	H	H	H	X	Exit Self Refresh, Idle after tRC	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
Self Refresh Recovery	H	H	H	X	X	X	X	Idel after tRC	
	H	H	L	H	H	X	X	Idel after tRC	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	L	H	X	X	X	X	Begin Clock Suspend next cycle	
	H	L	L	H	H	X	X	Begin Clock Suspend next cycle	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	X	X	X	Illegal	
	L	H	X	X	X	X	X	Exit Clock Suspend Next Cycle	
	L	L	X	X	X	X	X	Maintain Clock Suspend	
Power Down	H	X	X	X	X	X		Invalid	
	L	H	X	X	X	X	X	Exit Power Down Mode –> Idle	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	

FUNCTION TRUTH TABLE ... Continued

COMMAND TRUTH TABLE FOR CKE ... Continued

Current State	CKE n–1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Notes
Both Banks Idle	H	H	H	X	X	X		Refer to the Operation Command Table.	
	H	H	L	H	X	X		Refer to the Operation Command Table.	
	H	H	L	L	H	X		Refer to the Operation Command Table.	
	H	H	L	L	L	H	X	Auto–refresh	
	H	H	L	L	L	L	MODE	Refer to the Operation Command Table.	
	H	L	H	X	X	X		Refer to the Operation Command Table.	
	H	L	L	H	X	X		Refer to the Operation Command Table.	
	H	L	L	L	H	X		Refer to the Operation Command Table.	
	H	L	L	L	L	H	X	Self–refresh	
	H	L	L	L	L	L	MODE	Refer to the Operation Comand Table.	
	L	X	X	X	X	X	X	Power Down	
Any State Other Than Listed Above	H	H	X	X	X	X	X	Refer to the Operation Command Table.	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	Maintain Clock Suspend	

FUNCTION TRUTH TABLE ... Continued

COMMAND TRUTH TABLE FOR 2 BANK OPERATION

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7–0	Action	Current State	Next State
H	X	X	X	X	X	X	DESL	(I/A/RD/RDA/WR/WRA)=Any :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(I/A/RD/RDA/WR/WRA)=Any :B0 (I/A/RD/RDA/WR/WRA)=Any :B1
L	H	H	H	X	X	X	NOP	(I/A/RD/RDA/WR/WRA)=Any :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(I/A/RD/RDA/WR/WRA)=Any :B0 (I/A/RD/RDA/WR/WRA)=Any :B1
L	H	L	H	H	H	CA	Read	(A/RD/RDA/WR/WRA) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0	(RDA/RDA/RDA/RDA/RDA) :B1 (I/A/A/IP/A/IWP) :B0
				H	L	CA		(A/RD/RDA/WR/WRA) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0	(RD/RD/RD/RD/RD) :B1 (I/A/A/IP/A/IWP) :B0
				L	H	CA		(A/RD/RDA/WR/WRA) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(RDA/RDA/RDA/RDA/RDA) :B0 (I/A/A/IP/A/IWP) :B1
				L	L	CA		(A/RD/RDA/WR/WRA) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(RD/RD/RD/RD/RD) :B0 (I/A/A/IP/A/IWP) :B1
L	H	L	L	H	H	CA	Write	(A/RD/RDA/WR/WRA) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0	(WRA/WRA/WRA/WRA/WRA):B1 (I/A/A/IP/A/IWP) :B0
				H	L	CA		(A/RD/RDA/WR/WRA) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0	(WR/WR/WR/WR/WR) :B1 (I/A/A/IP/A/IWP) :B0
				L	H	CA		(A/RD/RDA/WR/WRA) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(WRA/WRA/WRA/WRA/WRA):B0 (I/A/A/IP/A/IWP) :B1
				L	L	CA		(A/RD/RDA/WR/WRA) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(RD/RD/RD/RD/RD) :B0 (I/A/A/IP/A/IWP) :B1
L	L	H	H	H	RA		Activate Bank	(I) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0	(A) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0
				L	RA			(I) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(A) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1
L	L	H	L	X	H	X	Precharge	(I/A/RD/RDA/WR/WRA)=Any :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(I/I/I/I/I) :B0 (I/I/I/I/I) :B1
				H	L	X		(I/A/RD/RDA/WR/WRA)=Any :B1 (I/A/RD/RDA/WR/WRA)=Any :B0	(I/I/I/I/I) :B1 (I/A/RD/RDA/WR/WRA)=Any :B0
				L	L	X		(I/A/RD/RDA/WR/WRA)=Any :B0 (I/A/RD/RDA/WR/WRA)=Any :B1	(I/I/I/I/I) :B0 (I/A/RD/RDA/WR/WRA)=Any :B1
L	L	L	H	X	X	X	Refresh	(I) :B0 (I) :B1	(IRC) :B0 (IRC) :B1
L	L	L	L	Refer to the Mode Register Table			MRS	(I):B0 (I):B1	(I):B0 (I):B1

Note:

1. L = Logic Low, H = Logic High, X = either L or H.
2. State Description

I	=	Idle	RDA	=	Read with Auto Precharge
IP	=	Idle after tRP	WR	=	Write
IWP	=	Idle after tWR+tRP	WRA	=	Write with Auto Precharge
A	=	Bank Active	B0	=	Bank0
RD	=	Read	B1	=	Bank1
IRC	=	Idle after tRC			

Example :

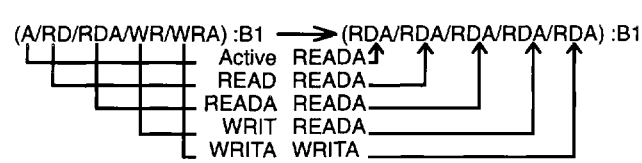
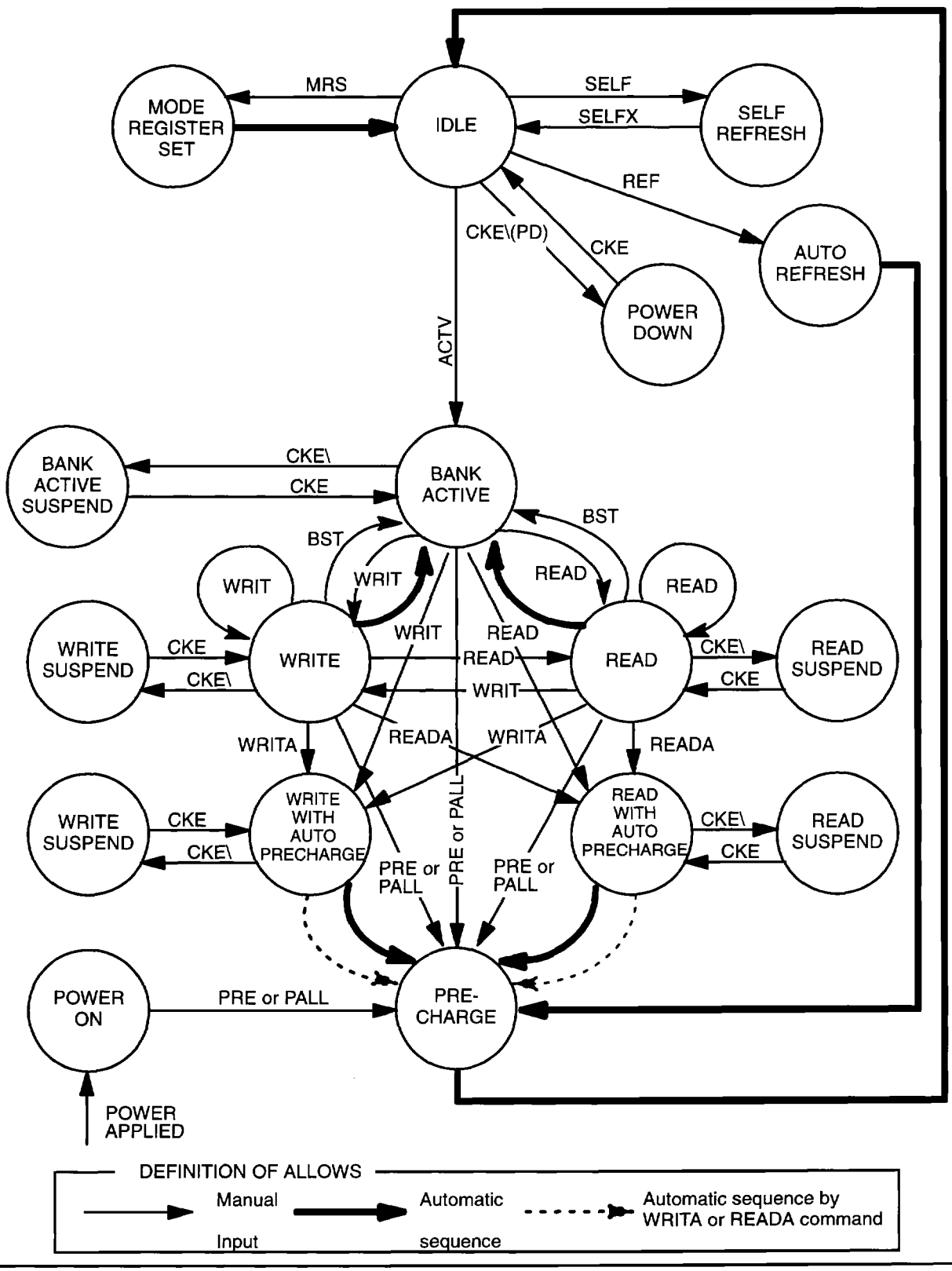


Fig. 2 - STATE DIAGRAM (Simplified State Diagram)



FUNCTIONAL DESCRIPTION

SDRAM BASIC FUNCTION

Three major differences between this SDRAM and conventional DRAMs are: synchronized operation, burst mode, and mode register.
The **synchronized operation** is the fundamental difference. An SDRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory even if it has been using two clocks, $\overline{RAS}$ and $\overline{CAS}$. Each operation of DRAM is determined by their timing phase difference while each operation of SDRAM is determined by commands and all operations are referenced by a positive clock edge. Fig 3 in page 19 show the basic timing diagram difference.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode register** is to justify the SDRAM operation and function into desired system conditions. Referenced in MODE REGISTER TABLE, if a system requires interleave for burst type and two clocks for CAS latency, SDRAM can be configured to those conditions by mode register programming.

CLOCK (CLK) and CLOCK ENABLE (CKE)

All input and output signals of SDRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), CKE = Low enters the Power Down mode(standby) and this will make extremely low standby current.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address input. When $\overline{CS}$ is high level, command signals are negated but internal operation such as burst cycle will not be suspended. In the small system $\overline{CS}$ can be tied to ground level.

COMMAND INPUT ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ do not directly imply SDRAM operation, such as Row address strobe by $\overline{RAS}$. Instead, each combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SDRAM operation. Refer to FUNCTION TRUTH TABLE.

ADDRESS INPUT (A0 to A8)

Address input selects an arbitrary location of a total of 131,072 words of each memory cell matrix. A total of twenty address input signals are required to decode such a matrix with nine Row and eight Column address format. SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), nine Row addresses are initially latched and the remainder of eight Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA).

BANK SELECT (A9)

This SDRAM has two banks and each bank is organized as 128K-words by 16-bit.
Bank selection by A9 occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and precharge command (PRE).

FUNCTIONAL DESCRIPTION ... Continued

DATA INPUT AND OUTPUT (DQ0 to DQ15)

Input data is latched and written into memory at the clock followed by a write command input. Data output is obtained by the following conditions followed by a read command input:

tRAC; from the bank active command when tRCD (min) is satisfied. (This parameter is reference only.)
tCAC; from the read command when tRCD is greater than tRCD (min).
tOVC; from the clock edge after tRAC and tCAC.

The polarity of the output data is identical to that of the input. Valid data time is between access time (determined by the three conditions above) and the next positive clock edge (tOH).

DATA I/O MASK (DQML and DQMU)

DQML and DQMU are an active high enable input and have an output disable and input mask function. During burst cycle and when DQML/U = H is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type.
The DQML controls lower byte of I/Os; DQ0 to DQ7, and DQMU controls upper byte of I/Os; DQ8 to DQ15.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobing column address. Access time and cycle time of Burst mode is specified as tOVC and tCLK, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length from 1 bits to full column of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read command	
Burst Read	Burst Write	1st Step	Mask command (Normally 3 clock cycles)
		2nd Step	Write command after IOWD
Burst Write	Burst Write	Write command	
Burst Write	Burst Read	1st Step	Mask command
		2nd Step	Read command after IWR
Burst Read	Precharge	Precharge command	
Burst Write	Precharge	1st Step	Mask command
		2nd Step	Precharge command after IWR
Burst Read	Bank Active	BST command	
Burst Write	Bank Active	BST command	

FUNCTIONAL DESCRIPTION ... Continued

BURST MODE OPERATION AND BURST TYPE (continued)

The burst stop command (BST) is applicable to stop the burst operation. If the BST command is excuted during ther burst operation, the burst operation is terminated immediately and bank state move to active. The BST command is valid with the full page burst only and is illegal during the burst operation with burst length of 1, 2, 4, and 8.

The burst type can be selected either sequential or interleave mode. The sequential mode is an incremental/decremental decoding scheme within a boundary address to be determined by count length, it assigns +1/–1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least/most significant address(=0).

Burst Length	Starting Column Address A2 A1 A0	Sequential Mode (Up Count)	Sequential Mode (Down Count)
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	3 – 2 – 1 – 0
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 1 – 0 – 3
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 7 – 6 – 5 – 4 – 3 – 2 – 1
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 7 – 6 – 5 – 4 – 3 – 2
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 1 – 0 – 7 – 6 – 5 – 4 – 3
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 3 – 2 – 1 – 0 – 7 – 6 – 5
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 3 – 2 – 1 – 0 – 7 – 6
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 5 – 4 – 3 – 2 – 1 – 0 – 7
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SDRAM memory is the same as DRAM, requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by Precharge command (PRE). With the precharge command, SDRAM will automatically be in standby state after precharge time (tRP).
The precharged bank is selected by combination of A8 and A9 when Precharge command is asserted.
If A8 = H, both banks are precharged regardless of A9 (PALL). If A8 = L, a bank to be selected by A9 is precharged (PRE).
The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion. This auto precharge is entered by A8=H when a read or write command is asserted. Refer to FUNCTION TABLE.

FUNCTIONAL DESCRIPTION ... Continued

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SDRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 16μs or a total 1,024 refresh commands within a 16.4ms period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX.
The Self-refresh is entered by applying an Auto–refresh command in conjunction with CKE = L (SELF). Once SDRAM enters the self-refresh mode, all inputs except for CKE will be "don't care" (either logic high or low level state) and outputs will be in a high-Z state. During a self-refresh mode, CKE = L should be maintained.

SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum 4 clock cycle before CKE brought high, and then the NOP command (NOP) or Deselect command (DESL) should be asserted within one tRC period. Refer to Timing Diagram for the detail.
It is recommended to assert an Auto-refresh command just after the tRC period to avoid the violation of refresh period.

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of five operation fields; Burst Length, Burst Type, CAS latency, Test Mode, and Operation Code. Refer to MODE REGISTER TABLE in page 27.
The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held.
The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDRAM. Refer to POWER-UP INITIALIZATION below.

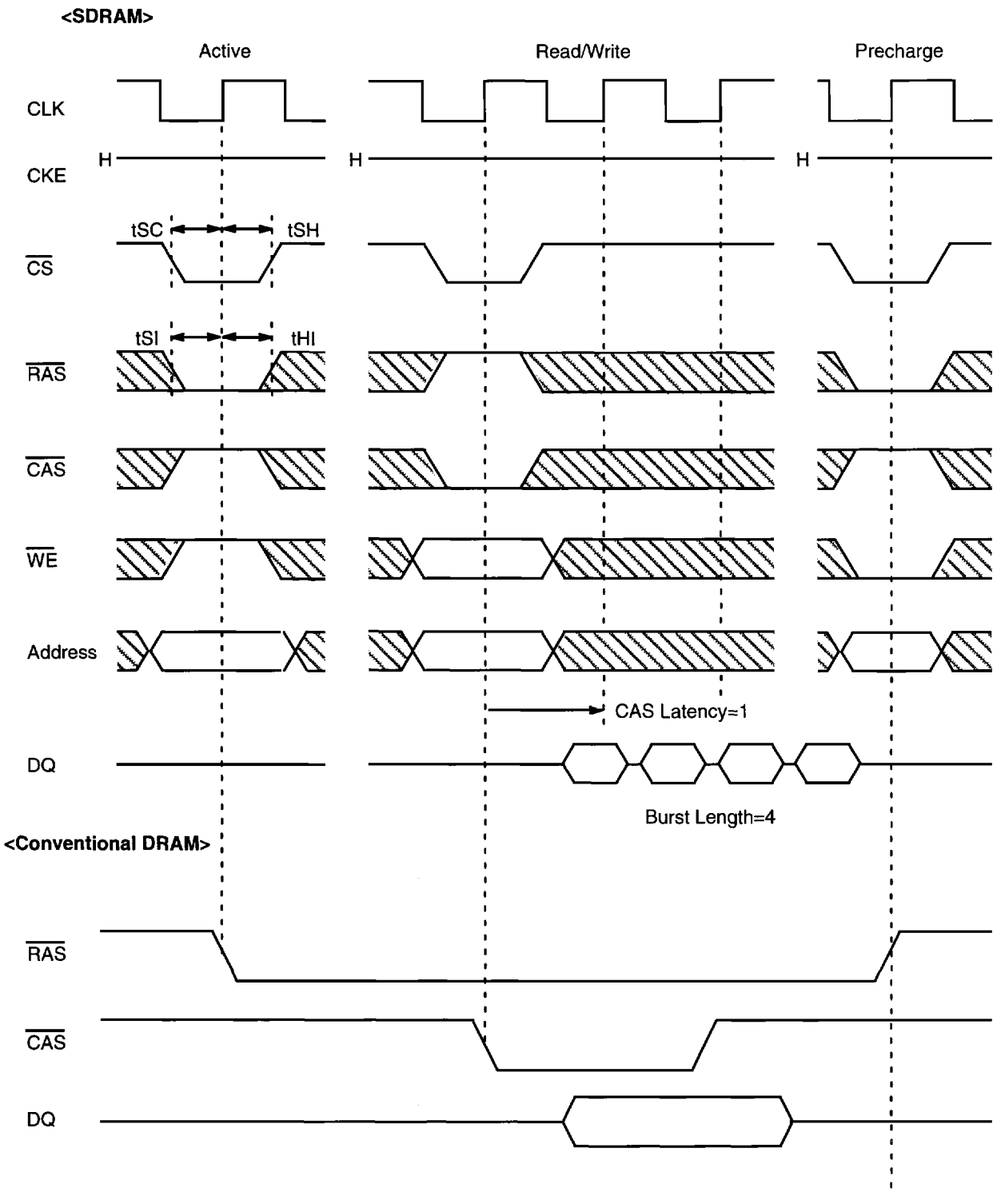
POWER-UP INITIALIZATION

The SDRAM internal condition after power-up will be undefined. It is required to follow the following **Power On Sequence** to execute read or write operation.

1. Apply power and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 200μs.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
4. Assert minimum of 8 Auto-refresh command(REF).
5. Program the mode register by Mode Register Set command(MRS).

In addition, it is recommended DQML/U and CKE to track VCC to insure that output is High-Z state. The mode register set command (MRS) can be set before 8 Auto–refresh command (REF).

Fig. 3 - Basic Timing for Conventional DRAM vs Syncronous DRAM



CAPACITANCE (TA=25° C, f = 1MHz)

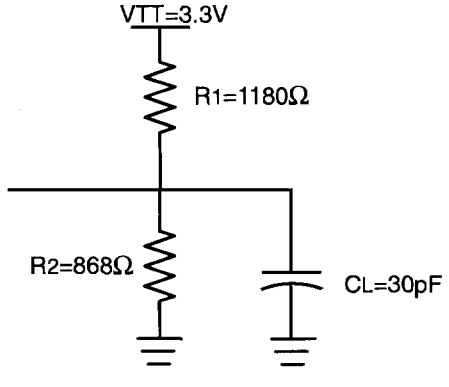
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, Address	CIN1	—	5	pF
Input Capacitance, Except for address	CIN2	—	5	pF
I/O Capacitance	CI/O	—	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC, VCCQ	3.0	3.3	3.6	V
	VSS, VSSQ	0	0	0	V
LVTTL Input High Voltage	VIH	2.0	—	VCC + 0.3	V
LVTTL Input Low Voltage	VIL	-0.3	—	0.8	V
Ambient Temperature	TA	0	—	70	°C

Fig.4 – SDRAM Load Circuit



LVTTL

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) **Notes 1, 2**

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
LVTTL Output High Voltage		VOH(DC)	IOH = –2 mA	2.4	–	–	V
LVTTL Output Low Voltage		VOL(DC)	IOL = 2 mA	–	–	0.4	V
Input Leakage Current (any input)		ILI	0V ≤ VIN ≤ VCC; All other pins not under test = 0V	–10	–	10	µA
Output Leakage Current		ILO	0V ≤ VIN ≤ VCC; Data out disabled	–10	–	10	µA
Operating Current (Average Power Supply Current)	MB81141623-010	ICC1S	No Burst : tCLK = min. One bank active	–	–	90	mA
	MB81141623-012					85	
	MB81141623-015					80	
	MB81141623-010	ICC1D	No Burst : tCLK = min. All banks active	–	–	130	mA
	MB81141623-012					120	
	MB81141623-015					110	
Precharge Standby Current (Power Supply Current)		ICC2P	CKE = VIL All banks idle tCLK = min. Power down mode	–	–	1	mA
		ICC2N	CKE = VIH All banks idle tCLK = min.	–	–	50	mA
Active Standby Current (Power Supply Current)		ICC3P	CKE = VIL Any bank active tCLK = min.	–	–	30	mA
		ICC3N	CKE = VIH Any bank active tCLK = min.	–	–	50	mA
Burst mode Current (Average Power Supply Current)	MB81141623-010	ICC4	tCLK = min.	–	–	135	mA
	MB81141623-012					125	
	MB81141623-015					115	
Refresh Current #1 (Average Power Supply Current)	MB81141623-010	ICC5S	Auto–Refresh; tCLK = min. tRC=min.	–	–	90	mA
	MB81141623-012					85	
	MB81141623-015					80	

DC CHARACTERISTICS ... Continued

(Recommended operating conditions unless otherwise noted.) Notes 1, 2

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Refresh Current #1 (Average Power Supply Current)	MB81141623-010	ICC5D	Auto–Refresh; tCLK = min. tRC=min. tRRD = min.	–	–	130	mA
	MB81141623-012					120	
	MB81141623-015					110	
Refresh Current #2 (Average Power Supply Current)		ICC6	Self–Refresh; CKE = VIL	–	–	2	mA

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 2, 3, 4

Parameter	Notes	Symbol	MB81141623-010		MB81141623-012		MB81141623-015		Unit
			Min	Max	Min	Max	Min	Max	
Clock Period	Latency=1	tCLK	30	–	35	–	40	–	ns
	Latency=2		15		17.5		20		ns
	[5] Latency=3		10		12		15		ns
Clock High Time		tCH	4	–	4	–	4	–	ns
Clock Low Time		tCL	4	–	4	–	4	–	ns
$\overline{CS}$ Setup Time		tSC	2	–	2	–	2	–	ns
$\overline{CS}$ Hold Time		tHC	2	–	2	–	2	–	ns
Input Setup Time		tSI	2	–	2	–	2	–	ns
Input Hold Time		tHI	2	–	2	–	2	–	ns
Output Valid from Clock	Latency=1	tOVC	–	28	–	32	–	35	ns
	Latency=2		–	13	–	14.5	–	16	ns
	[6, 7] Latency=3		–	8	–	9	–	10	ns
Output in Low-Z		tOLZ	3	–	3	–	3	–	ns
Output in High-Z [8]		tOHZ	2	10	2	12	2	15	ns
Output Hold Time		tOH	2	–	2	–	2	–	ns
Time between Refresh		tREF	–	16.4	–	16.4	–	16.4	ms
Transition Time		tT	0.5	2	0.5	2	0.5	2	ns
Power Down Exit Time		tPDE	12	–	14	–	17	–	ns

AC CHARACTERISTICS ... Continued

(Recommended operating conditions unless otherwise noted.) Note 2,3,4

BASE VALUES FOR CLOCK COUNT / LATENCY

Parameter	Notes	Symbol	MB81141623-010		MB81141623-012		MB81141623-015		Unit
			Min	Max	Min	Max	Min	Max	
RAS Cycle Time	9	tRC	100	–	118	–	140	–	ns
RAS Access Time	10	tRAC	–	58	–	67	–	75	ns
CAS Access Time	11, 14	tCAC	–	28	–	32	–	35	ns
RAS Precharge Time		tRP	40	–	48	–	60	–	ns
RAS Active Time		tRAS	60	10000	70	10000	80	10000	ns
RAS to CAS Delay Time	12	tRCD	30	–	35	–	40	–	ns
Write Recovery Time		tWR	15	–	15	–	20	–	ns
RAS to RAS Bank Active Delay Time		tRRD	30	–	35	–	40	–	ns

CLOCK COUNT FORMULA Note 14

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}}$$ (Round off a whole number)

LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81141623-010	MB81141623-012	MB81141623-015	Unit
CKE to Clock Disable		lCKE	1	1	1	cycle
DQM to Output in High-Z		lDQZ	2	2	2	cycle
DQM to Input Data Delay		lDQD	0	0	0	cycle
Last Output to Write Command Delay		lOWD	2	2	2	cycle
Write Command to Input Data Delay		lDWD	0	0	0	cycle
Precharge to Output in High-Z Delay	15	lROH	2	2	2	cycle
Mode Register Access to Bank Active(min.)		lMRD	2	2	2	cycle
CAS to CAS Delay (min.)		lCCD	1	1	1	cycle
CAS Bank Delay (min.)		lCBD	1	1	1	cycle

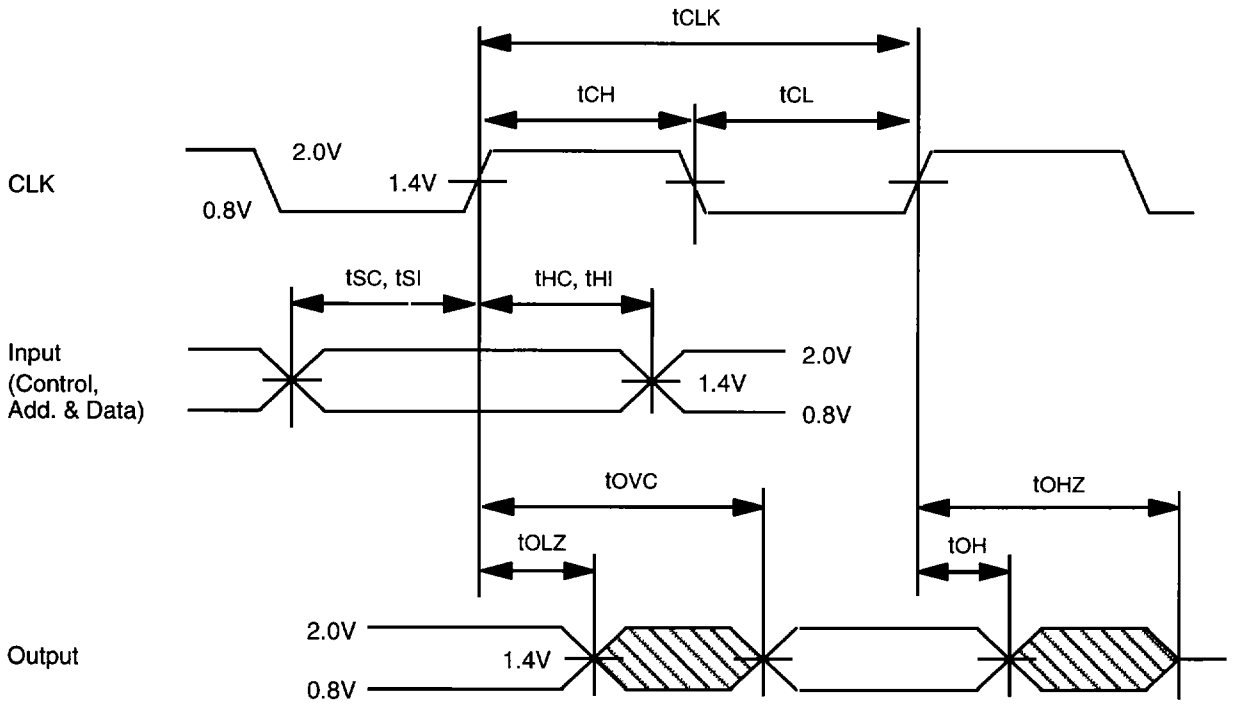
AC CHARACTERISTICS ... Continued

(Recommended operating conditions unless otherwise noted.) Note 2,3,4

Notes:

1. ICC depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.
2. An initial pause (DESL or NOP) of 200µs is required after power-up followed by a minimum of eight Auto Refresh cycles.
3. AC characteristics assume tT = 1ns and 30pF of capacitive load.
4. 1.4V is the reference level for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max).
5. Maximum value is a reference value and a device may work at a slower untested clock rate.
6. Assumes tRCD and tCAC are satisfied.
7. tOVC also specifies the access time at burst mode except for first access.
8. Specified where output buffer is no longer driven.
9. Actual clock count of tRC (IRC) will be sum of clock count of tRAS (IRAS) and tRP (IRP).
10. tRAC is a reference value. Maximum value is obtained from the sum of tRCD (min) and tCAC (max).
11. Assumes tRAC and tOVC are satisfied.
12. Operation within the tRCD (min) ensures that tRAC can be met; if tRCD is greater than the specified tRCD (min), access time is determined by tCAC or tOVC.
13. All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula:
    clock count equals base value divided by clock period (round off to a whole number).
14. The ICAC is programmed by the mode register.
15. IROH depends on CAS Latency (CL). If CL is one, the IROH will be one cycle. All other case will be two cycles Refer to CL REGISTER of MODE REGISTER TABLE in page 27.

Fig. 5 - TIMING DIAGRAM, SETUP, HOLD AND DELAY TIME



Note: Reference level of input signal is 1.4V for LVTTL.
Access time is measured at 1.4V for LVTTL.

Fig. 6 - TIMING DIAGRAM, DELAY TIME for Power Down Exit

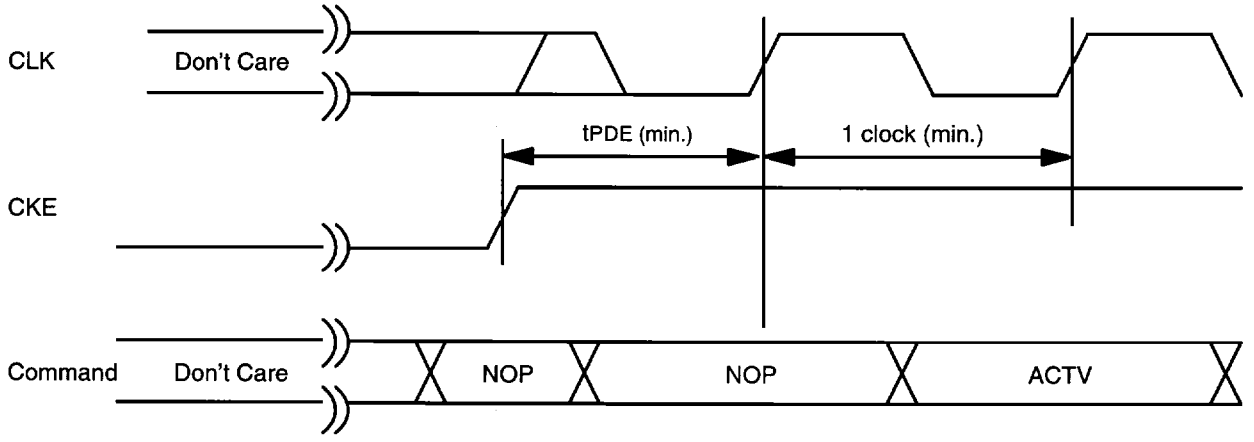


Fig. 7 - TIMING DIAGRAM, PULSE WIDTH

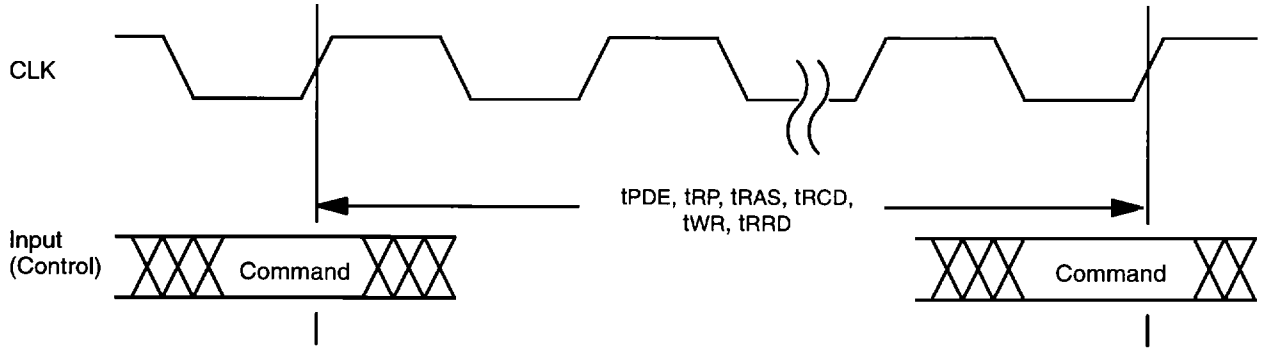
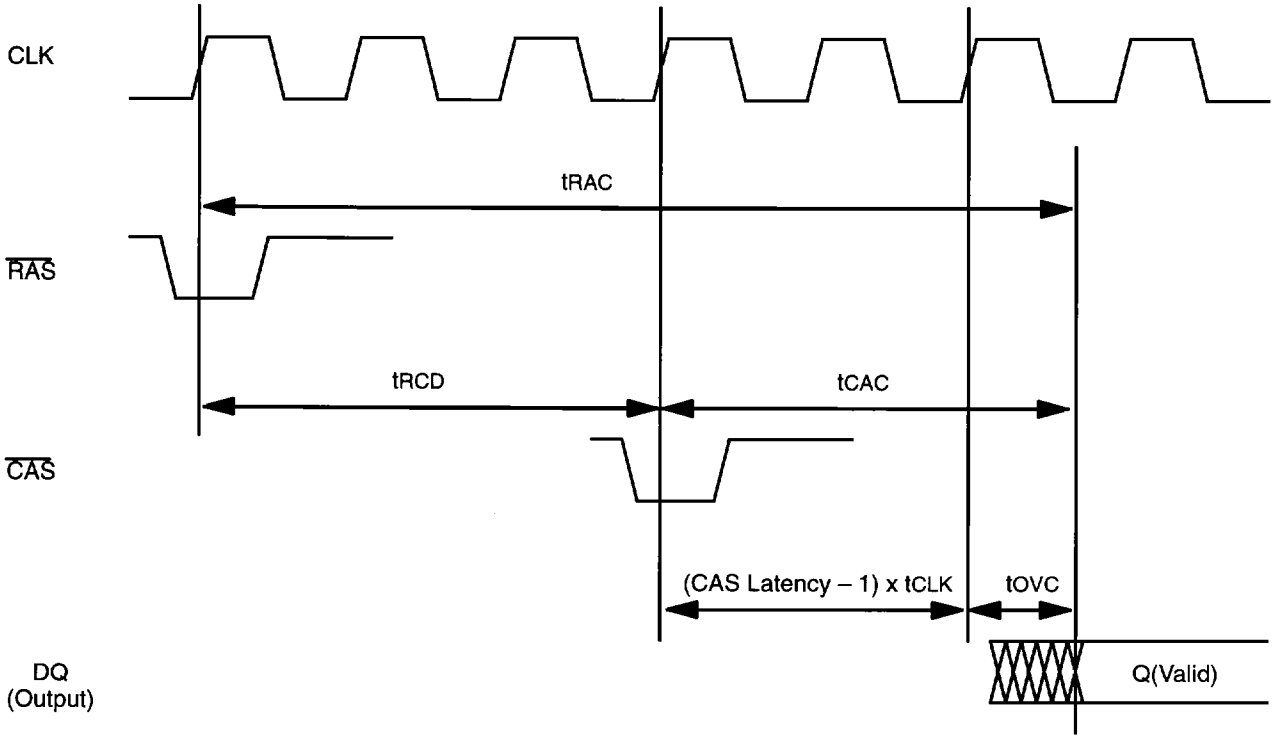


Fig. 8 - TIMING DIAGRAM, ACCESS TIME



Note: tRAC is a reference value. Data can be obtained after both tCAC and tOVC are satisfied.

MODE REGISTER TABLE

MODE REGISTER SET

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS
Op–code	0	0	CL			BT	BL			MODE REGISTER

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

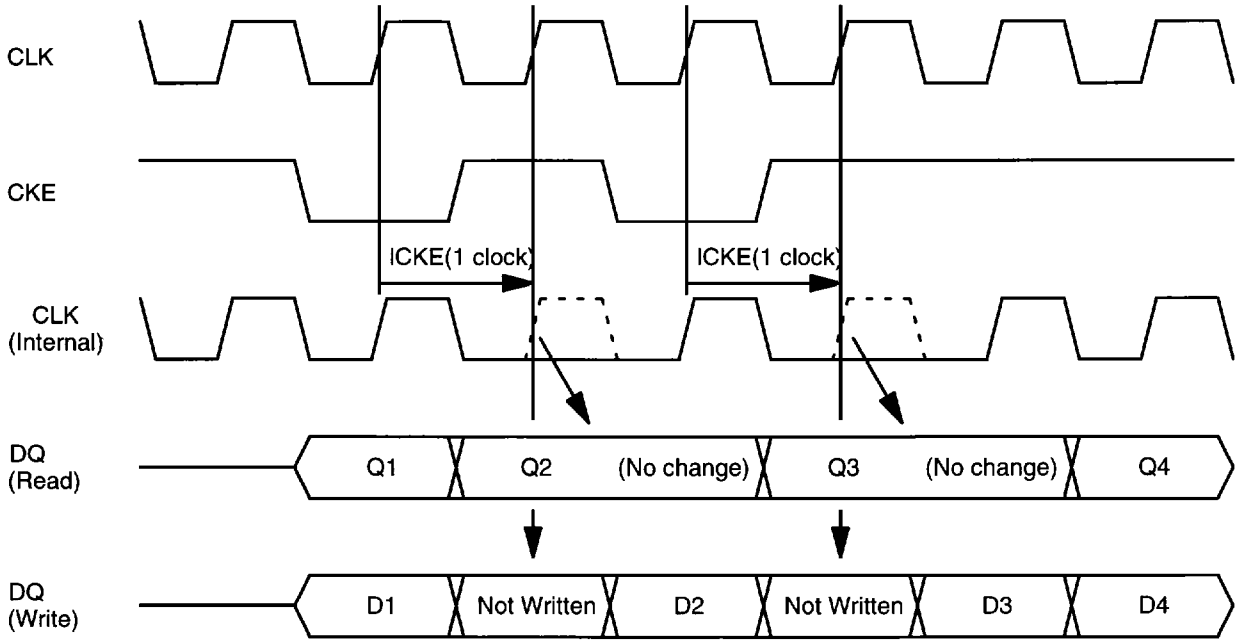
A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Column

A9	Op–code
0	Burst Read & Burst Write
1	Burst Read & Single Write

A3	Burst Type
0	Sequential (Wrap round, Binary–up)
1	Sequential (Wrap round, Binary–down)

NOTE : When A9=1, burst length at Write is always one regardless of BL value.

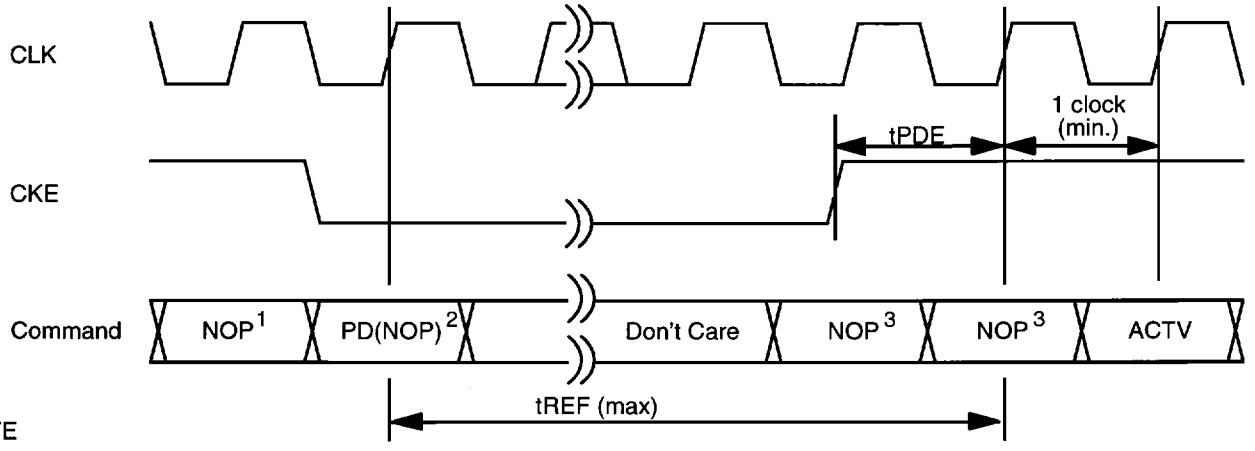
TIMING DIAGRAM-1 : CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)



FUNCTION DESCRIPTION:

The latency of CKE (ICKE) is one clock. During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output remain the same data. During the write mode, data at the next clock of CSUS command is ignored.

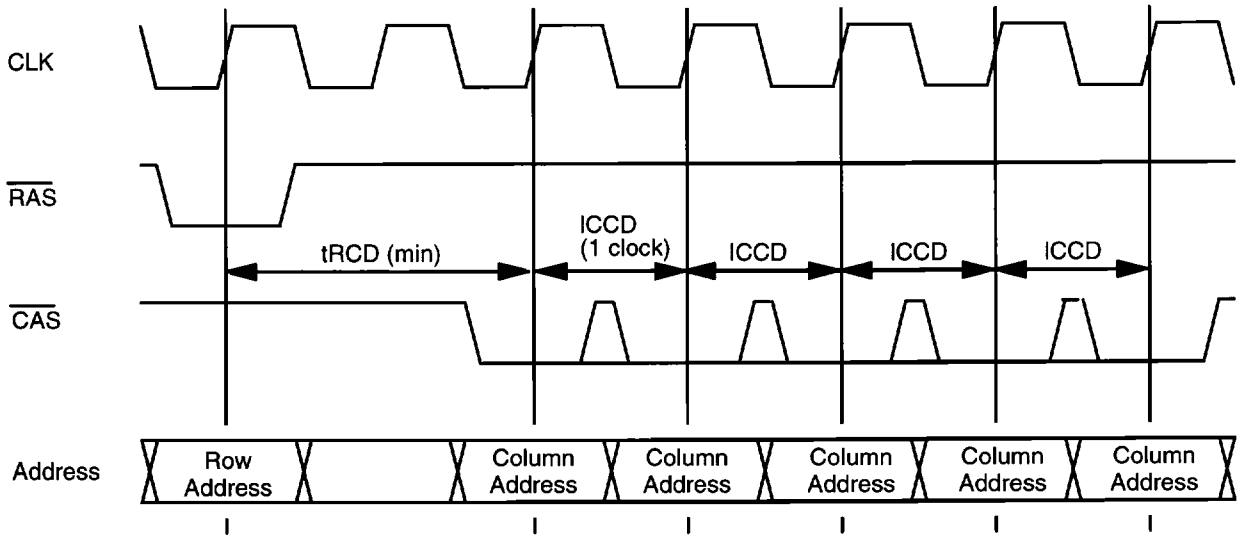
TIMING DIAGRAM-2 : CLOCK ENABLE - POWER DOWN ENTRY AND EXIT



NOTE

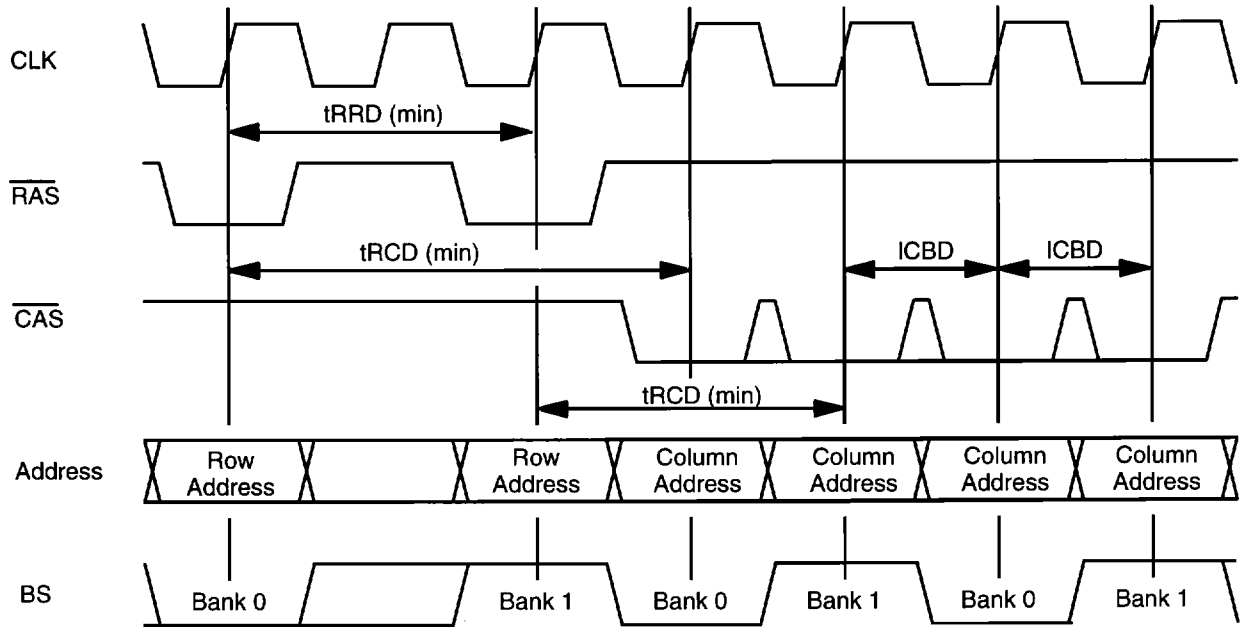
1: Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.
2: Precharge command can be posted in conjunction with CKE when burst mode is ended at this clock.
3: The ACTV command can be latched after tPDE (min) + 1clock(min.). It is recommended to apply NOP command in conjunction with CKE. It is also recommended to apply minimum of 4 clocks to stabilize external clock prior to ACTV command.

TIMING DIAGRAM-3 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY

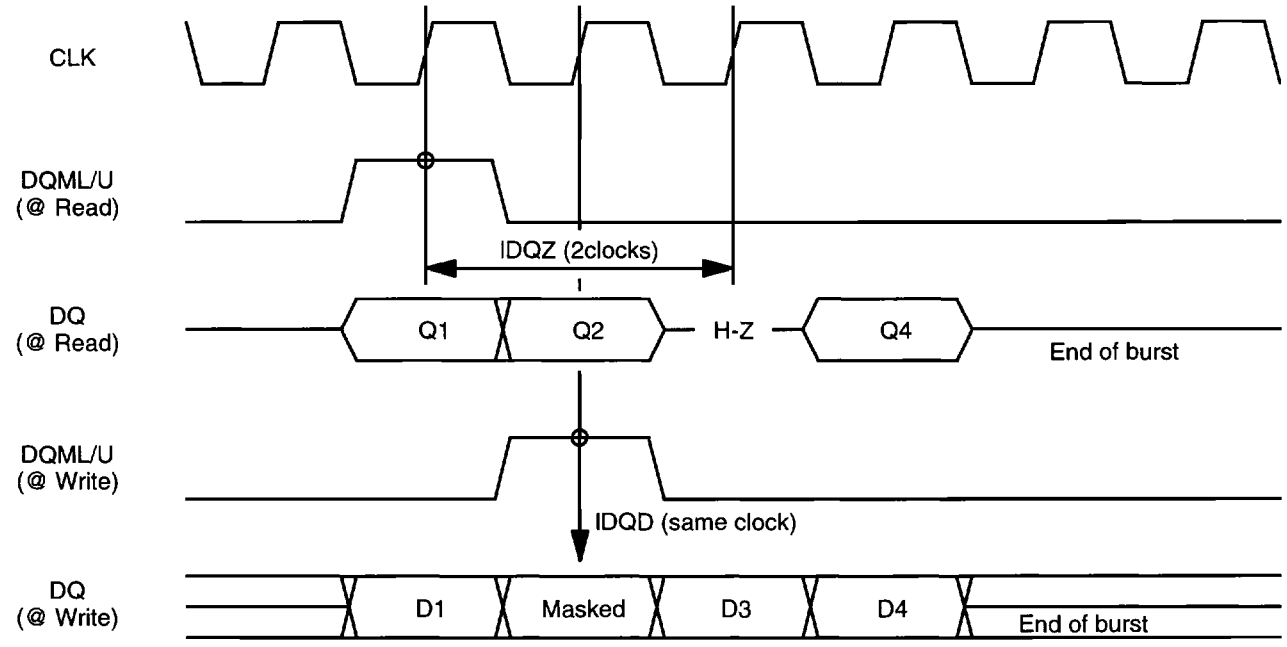


NOTE : $\overline{CAS}$ to $\overline{CAS}$ address delay can be one or more clock period.

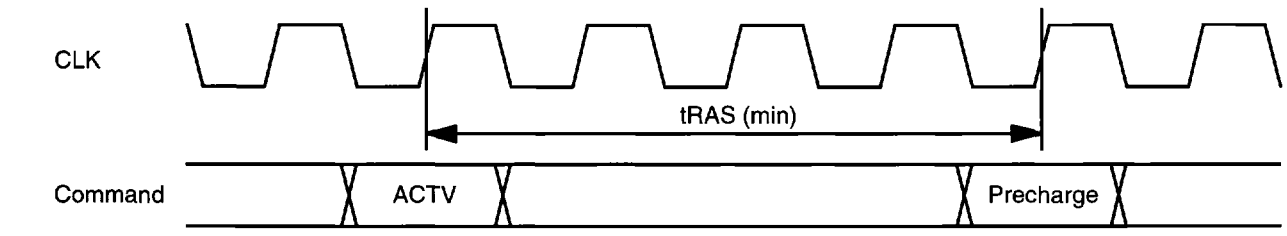
TIMING DIAGRAM-4 : DIFFERENT BANK ADDRESS INPUT DELAY



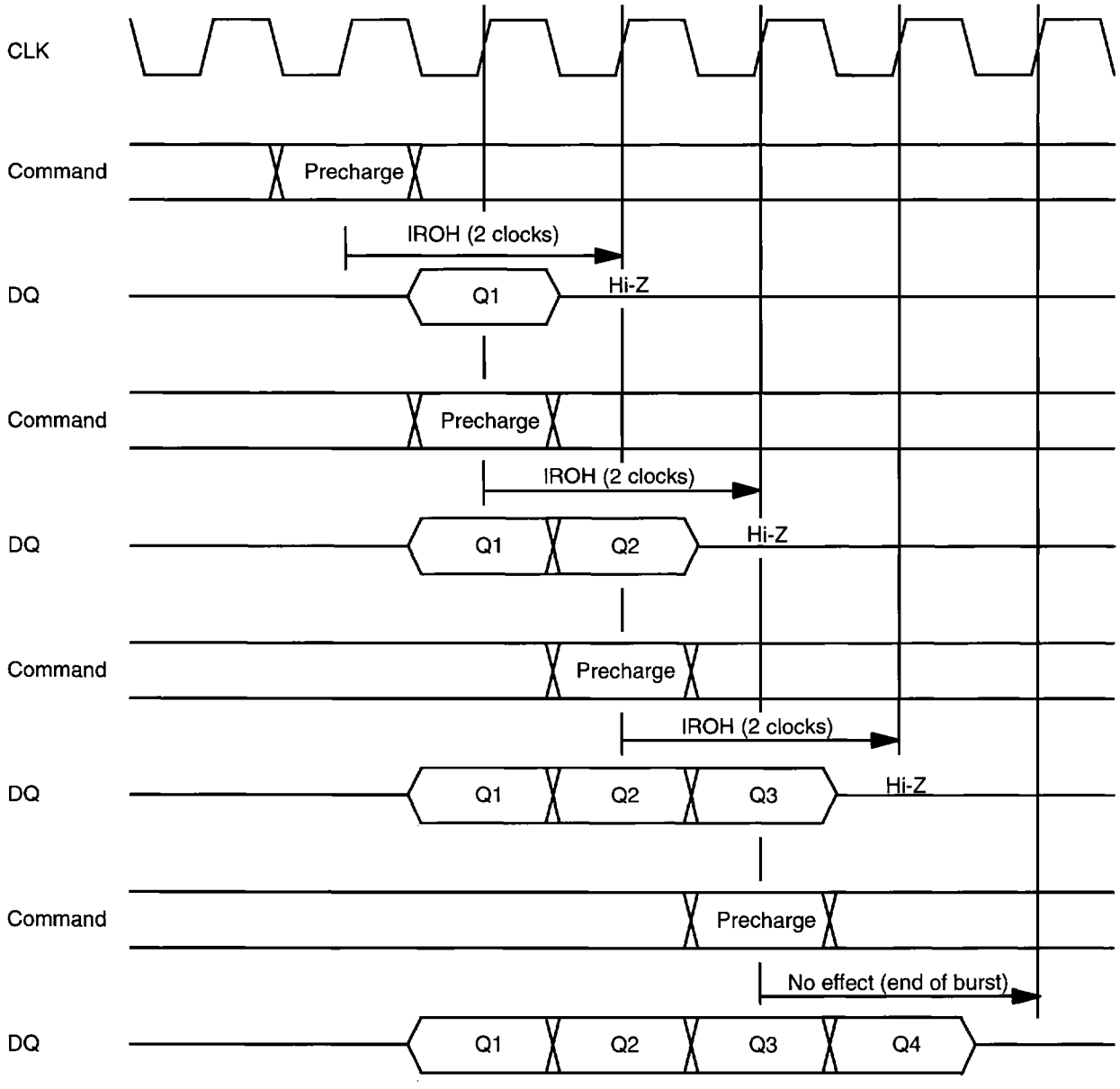
TIMING DIAGRAM-5 : DQM - INPUT MASK AND OUTPUT DISABLE (@ BL=4)



TIMING DIAGRAM-6 : PRECHARGE TIMING (APPLIED TO THE SAME BANK)

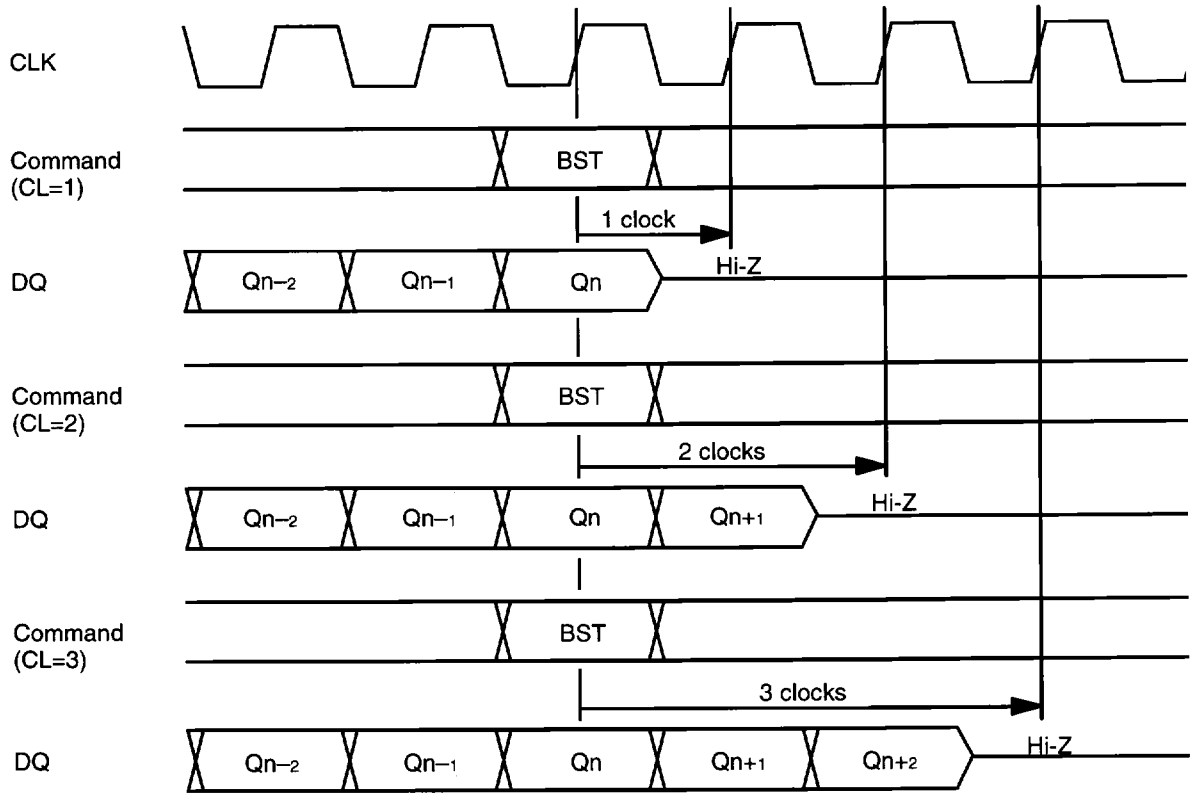


TIMING DIAGRAM-7 : READ INTERRUPTED BY PRECHARGE (Example @ CL=2, BL=4)



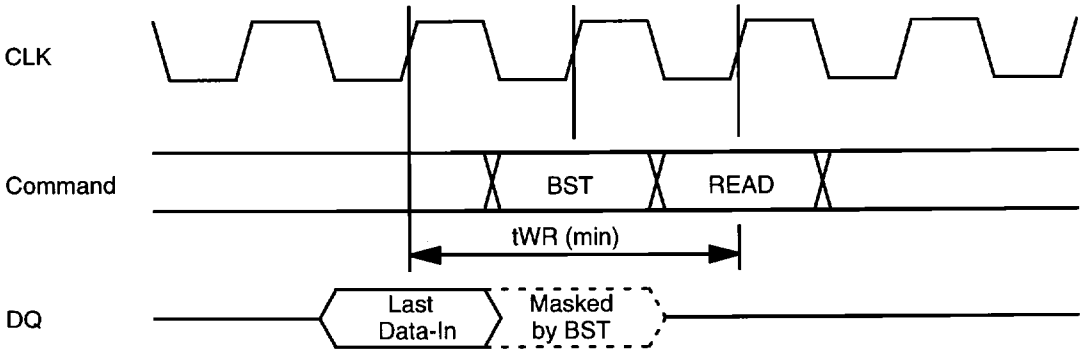
Note: In case of CL (CAS Letency) = 1, the IROH is 1 clock.

TIMING DIAGRAM-8 : READ INTERRUPTED BY BURST STOP (Example @ BL=Full Column)



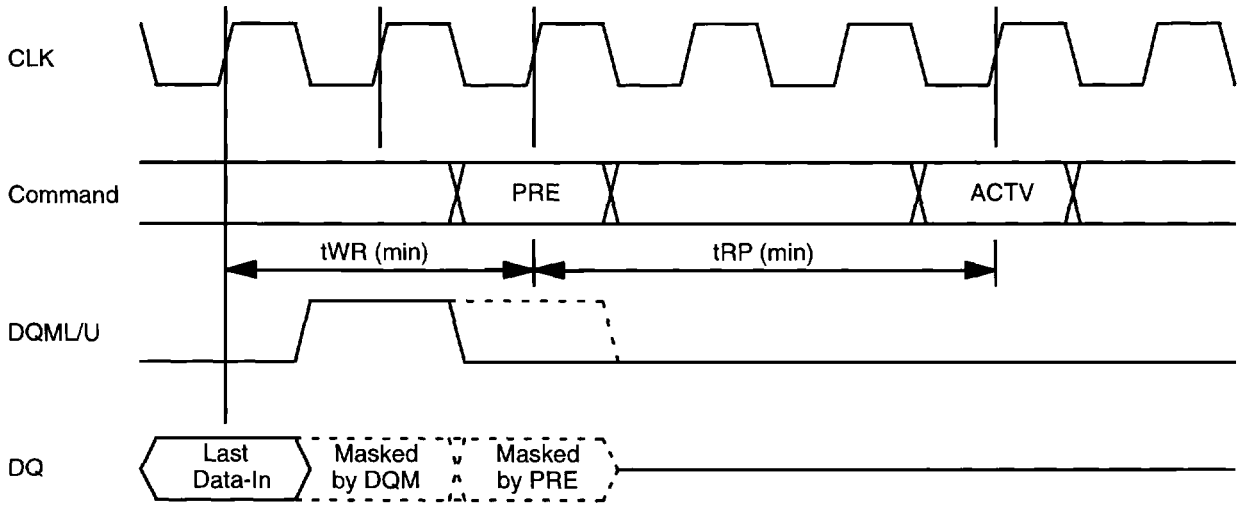
Note: In case of CL (CAS Letency) = 1, "n" should be 1≤n≤255. When "n" is equal to 256, BST command takes no effect.
In case of CL (CAS Letency) = 2, "n" should be 1≤n≤254. When "n" is 255≤n≤256, BST command takes no effect.
In case of CL (CAS Letency) = 3, "n" should be 1≤n≤253. When "n" is 254≤n≤256, BST command takes no effect.

TIMING DIAGRAM-9 : WRITE INTERRUPTED BY BURST STOP (Example @ CL=2)



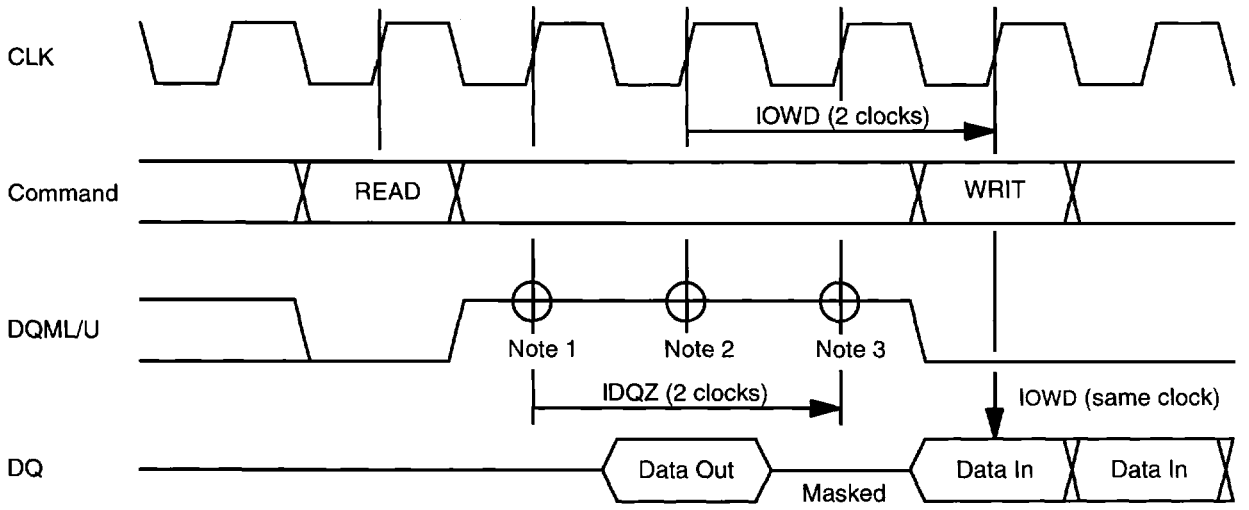
Note: The read command (RD) should only be issued after the tWR of final data input, is satisfied.

TIMING DIAGRAM-10 : WRITE INTERRUPTED BY DQML/U & PRECHARGE (Example @ CL=2)



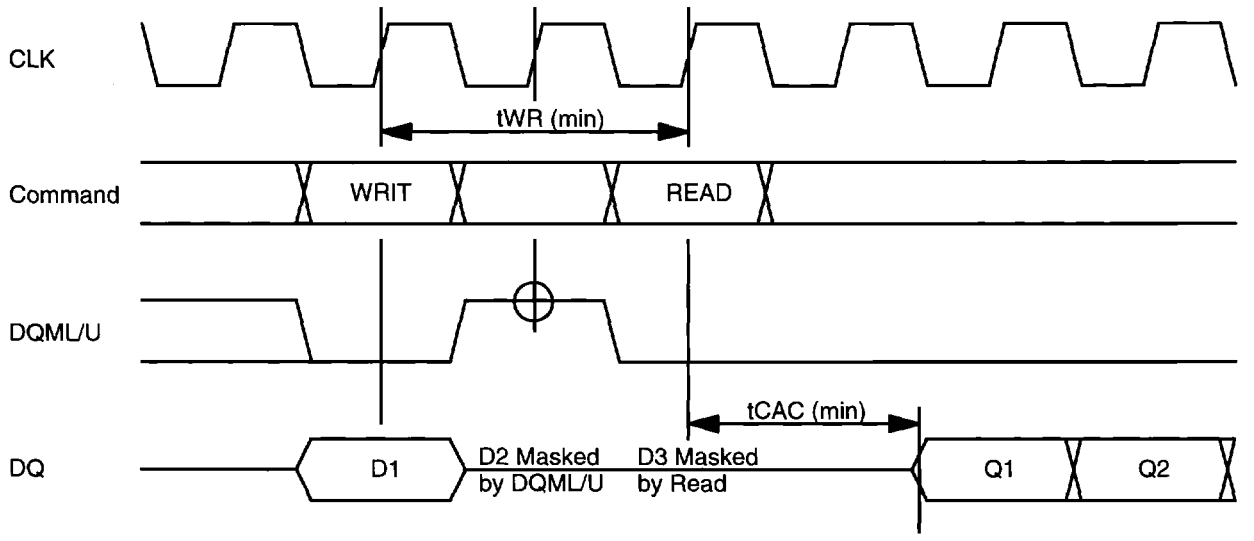
Note: The precharge command (PRE) should only be issued after the tWR of final data input, is satisfied.

TIMING DIAGRAM-11 : READ INTERRUPTED BY WRITE (Example @ CL=2, BL≥4)



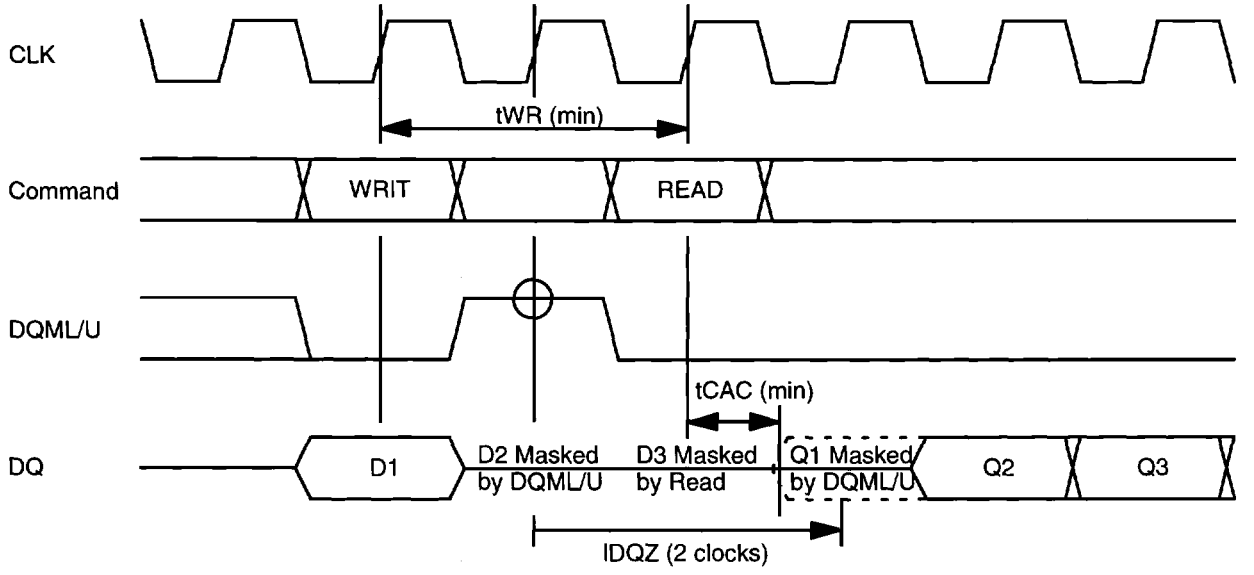
Note 1: First DQML/U makes high impedance state H–Z between last output and first input data.
Note 2: Second DQML/U makes internal output data mask to avoid bus contention.
Note 3: Third DQML/U in illustrated above also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQML/U is required to avoid internal bus contention.

TIMING DIAGRAM-12 : WRITE TO READ TIMING (Example @ CL=2, BL>2)



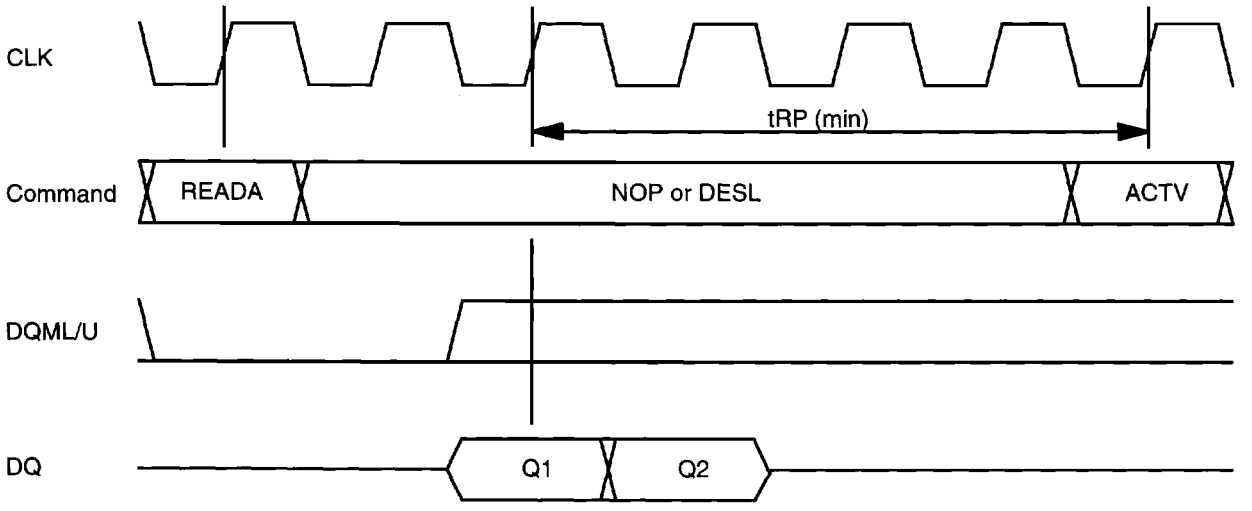
Note: Read command should be issued after tWR of final data input is satisfied if read command is applied to the same bank.

TIMING DIAGRAM-13 : WRITE TO READ TIMING (Example @ CL=1, BL>2)



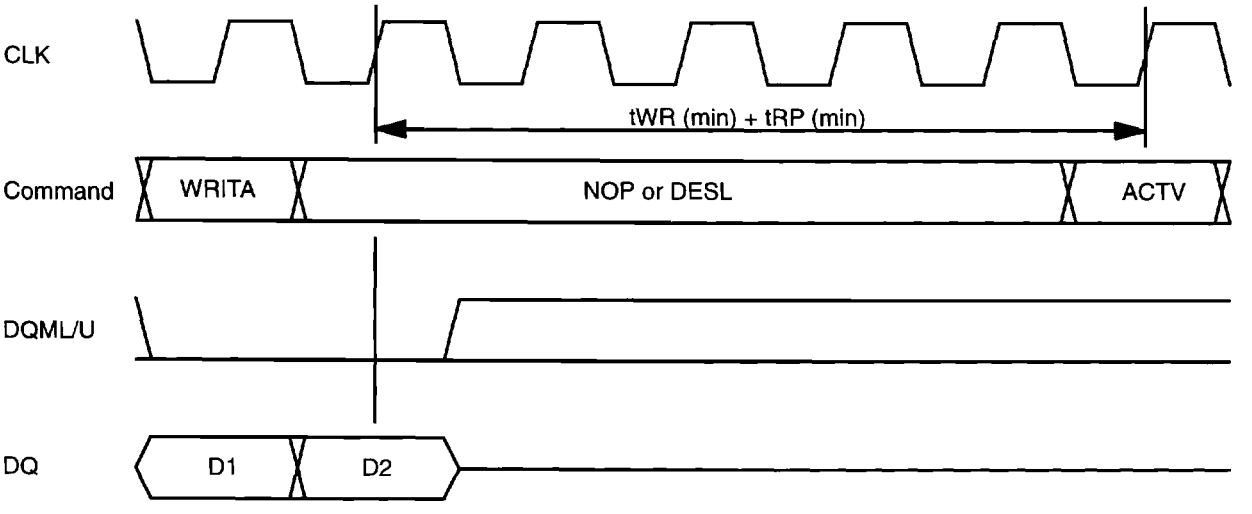
Note: In case of CAS latency (CL) = 1, the first output data is also masked by last DQML/U for write.

TIMING DIAGRAM-14 : READ WITH AUTO–PRECHARGE (Example @ CL=2, BL=2)



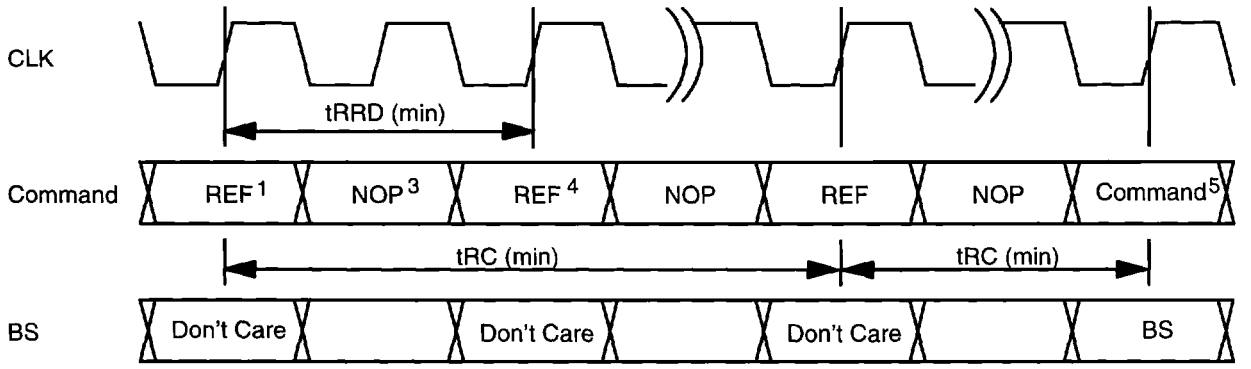
Note: Precharge at read with auto precharge (READA command) is started from one clock prior to end of burst.
Once auto precharge command is asserted, no new command within the same bank can be issued.

TIMING DIAGRAM-15 : WRITE WITH AUTO–PRECHARGE (Example @ CL=2, BL=2)



Note: Precharge at write with auto–precharge is started after the write recovery time (tWR) from the end of burst.
Even if the final data is masked by DQML/U, the precharge does not start the clock of final data input.
Once auto precharge command is asserted, no new command within the same bank can be issued.

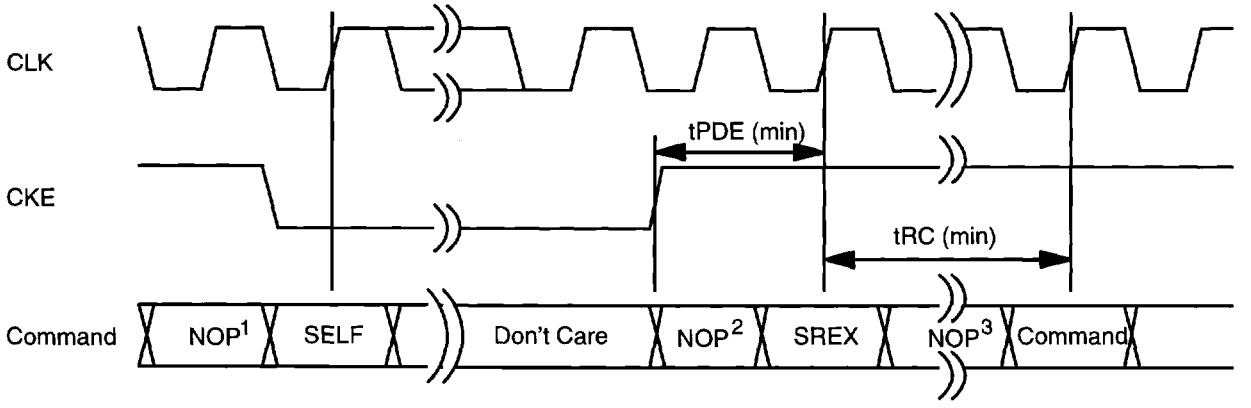
TIMING DIAGRAM-16 : AUTO-REFRESH TIMING



Note:

1: All banks should be precharged prior to the first auto–refresh command (REF).
2: Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.
3: Either NOP or DESL command should be issued during tRRD and tRC period while auto–refresh mode.
4: The second REF command can be issued after tRRD from the first REF command because the second REF command select the other bank.
5: Any activation command such as ACTV or MRS command other than REF command should be issued after tRC from the last REF comand.

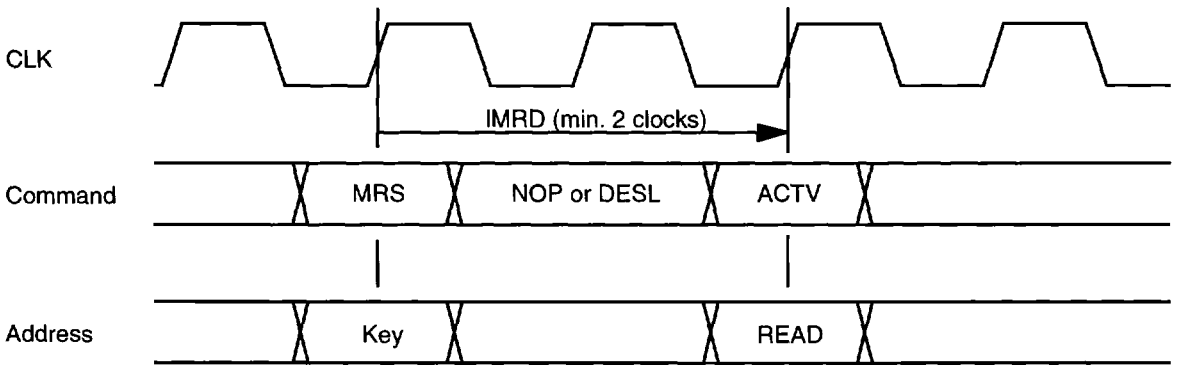
TIMING DIAGRAM-17 : SELF-REFRESH ENTRY AND EXIT TIMING



Note:

1: Precharge command (PRE or PALL) should be asserted if any bank is active prior to self-refresh entry command (SELF).
2: The self-refresh exit command (SELFX) is latched after tPDE (min.). It is recommended to apply NOP command in conjunction with CKE. It is also recommended to apply minimum of 4 clocks to stabilize external clock prior to SELFX command.
3: Either NOP or DESL command can be used during tRC period.

TIMING DIAGRAM-18 : MODE REGISTER SET TIMING

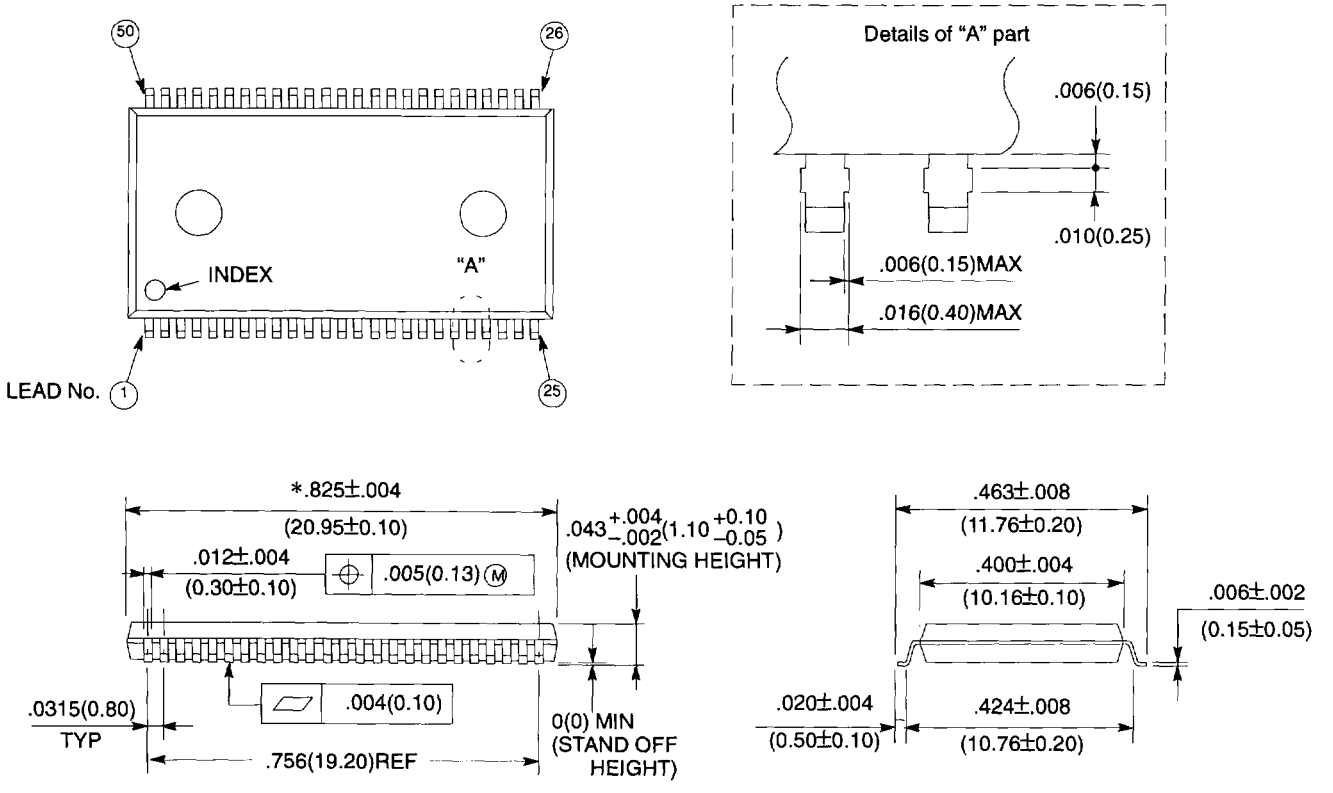


Note: The mode register set command (MRS) should be only issued after all banks have been precharged.

PACKAGE DIMENSIONS

Suffix: PFTN

50-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-50P-M01)



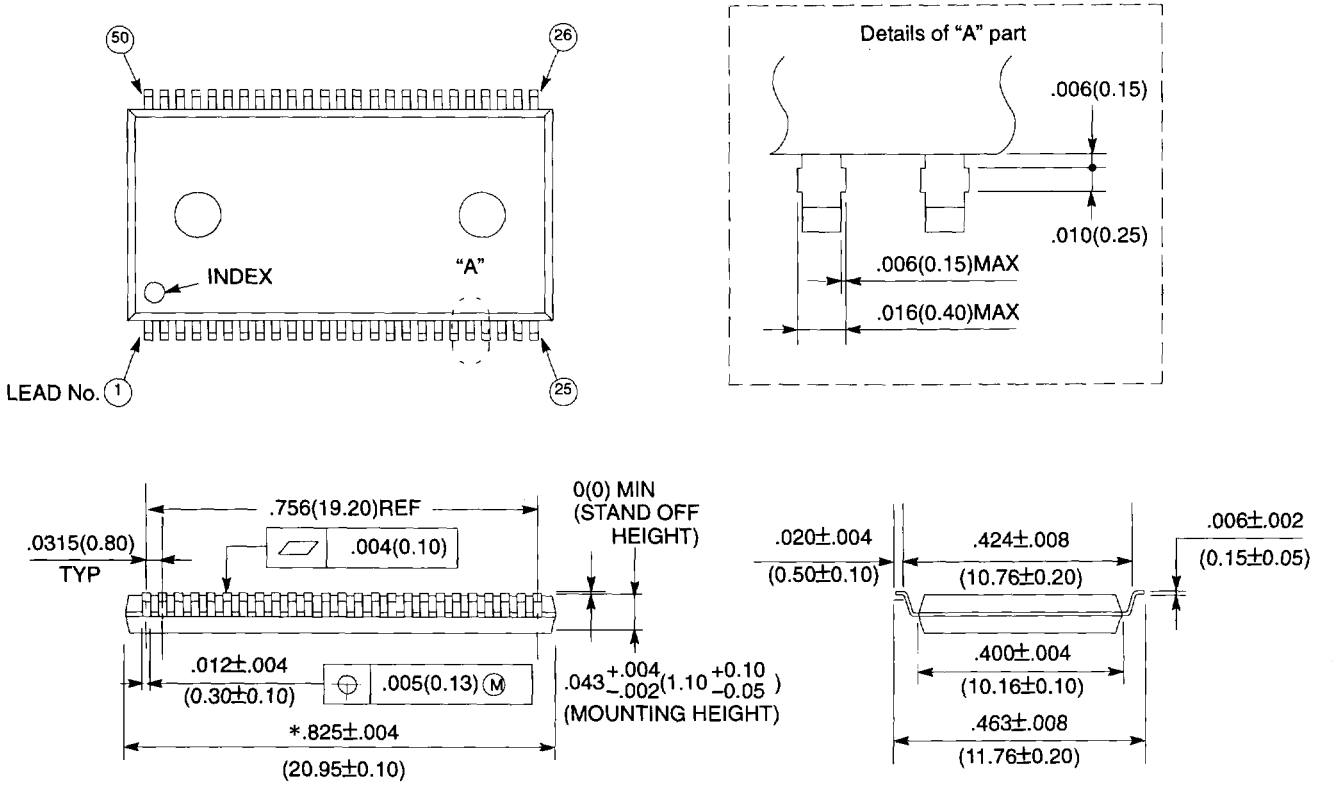
*: Resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS ... Continued

Suffix: PFTR

50-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-50P-M02)



*: Resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

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