4Mx4 CMOS EDO Dynamic RAM 3.3V

*ADVANCED**

FEATURES

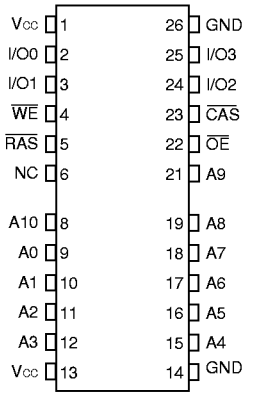
- Fast Access Time (t_{RAC}): 70, 80, 100ns
- Power Supply: 3.3V ±0.3V
- Packaging:
  - 24/26 pin Ceramic Flatpack (FP)
  - 24/26 pin Ceramic Flatpack, Lead Formed (F1)
  - 24/28 pin Ceramic Flatpack (FB)
  - 24/28 pin Ceramic Flatpack, Lead Formed (F2)
- Commercial, Industrial and Military Temperature Ranges
- Extended Data Out (EDO) Page Mode Access Cycle.
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Common I/O
- 2K Cycle Refresh = 32ms
- Low Active Power Dissipation
- Low Standby Power Dissipation

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PIN CONFIGURATION FOR WMD4M4-XXX

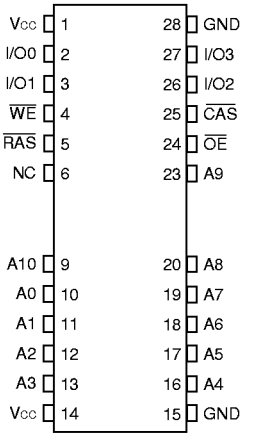
24/26 pin (FP, F1)

TOP VIEW



24/28 pin (FB, F2)

TOP VIEW



PIN DESCRIPTION

A_{0-10}	Address Inputs
I/O_{0-3}	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	+3.3V Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Short Circuit Output Current	Ios		50	mA
Power Dissipation	P_D		1	W
Supply Voltage Range	V_{CC}	-1.0	4.6	V
Voltage Range on any Pin*	V_T	-1.0	5.5	V

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

* All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.0	5.5	V
Input Low Voltage	V_{IL}	-1.0	+0.8	V
Operating Temp. (Com.)	T_A	0	+70	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

(T_A = 25°C)

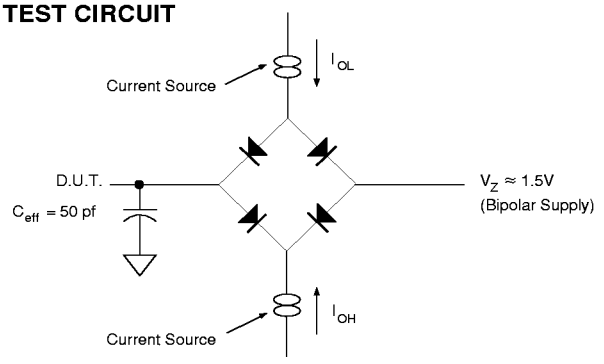
Parameter	Symbol	Max	Unit
A_{0-10} Input Capacitance	$C_{I(A)}$	6	pF
$\overline{RAS}$ and $\overline{CAS}$ Input Capacitance	$C_{I(RC)}$	7	pF
$\overline{OE}$ Input Capacitance	$C_{I(OE)}$	7	pF
$\overline{WE}$ Input Capacitance	$C_{I(WE)}$	7	pF
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	$C_{I/O}$	8	pF

This parameter is guaranteed by design but not tested.

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address		Data In/Out
						t_R	t_C	I/O_{0-3}
Standby		H	H→X	X	X	X	X	High-Z
Read		L	L	H	L	ROW	COL	Data-Out
Early Write		L	L	L	X	ROW	COL	Data-In
Read Write		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-Page-Mode Read	1st cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-Page-Mode Early Write	1st cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
	Any cycle	L	L→H	H	L	n/a	n/a	Data-Out
EDO-Page-Mode Read-Write	1st cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-Only Refresh		L	H	X	X	ROW	n/a	High-Z
Hidden Refresh (Read)		L→H→L	L	H	L	ROW	COL	Data-Out
Hidden Refresh (Write)		L→H→L	L	L	X	ROW	COL	Data-In
CBR Refresh		H→L	L	H	X	X	X	High-Z

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DC CHARACTERISTICS

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Test Condition	Symbol	Min	Max	Units
High Level Output Voltage	I_{OH} = -2mA	V_{OH}	2.4		V
Low Level Output Voltage	I_{OL} = 2mA	V_{OL}		0.4	V
Input Current (Leakage)	V_I = 0V to +3.6V All others = 0V	I_I		10	µA
Output current (Leakage)	VO = 0V to Vcc, data floating	I_O		20	µA
Read or Write Cycle Current (1,2)	Vcc = 3.6V, minimum cycle	I_{CC1}		80	mA
Standby Current	$\overline{RAS}$ and $\overline{CAS}$ = V_{IH}, output open	I_{CC2}		2	mA
Average Page Current (1,2)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, minimum cycle	I_{CC4}		80	mA

NOTES:
1. I_{CC1} and I_{CC4} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading, specified values are obtained with the output open.

AC CHARACTERISTICS FOR READ ONLY OPERATIONS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C) Note 1

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Access Time from $\overline{CAS}$ (2,3)	t_{CAC}		20		20		25	ns
Access Time from $\overline{RAS}$ (2,4)	t_{RAC}		70		80		100	ns
Column Address Access Time (2)	t_{CAA}		35		40		50	ns
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		40		40		50	ns
Access Time from $\overline{OE}$ (2)	t_{OEA}		20		20		25	ns
Output Low Impedance Time from $\overline{CAS}$ Low (5)	t_{CLZ}	0		0		0		ns
Output Disable Time after $\overline{CAS}$ High (6)	t_{OFF}	0	15	0	20	0	20	ns
Output Disable Time after $\overline{OE}$ High (6)	t_{DISOE}	0	15	0	20	0	20	ns

NOTES:
1. An initial pause of 100µs is required after power-up, followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-only or CBR with $\overline{WE}$ High), before proper device operation is ensured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} requirement is exceeded.
2. Measured with a load circuit equivalent to 2t_{TTL} loads 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
3. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
5. Guaranteed by design, but not tested.
6. t_{OFF} (max) defines the time at which the output achieves the high impedance state (IOUT ≤ ±10µA) and is not reference to V_{OH} (min) or V_{OL} (max).

AC OPERATIONS AND CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Refresh Cycle	t_{REF}		32		32		32	ms
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		80		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time (9)	t_{RCD}	20	50	20	60	25	75	ns
Delay $\overline{CAS}$ High to $\overline{RAS}$ Low	t_{CRP}	5		5		5		ns
$\overline{CAS}$ Precharge Time (Non Page Mode)	t_{CP}	10		10		10		ns
Column Address Delay Time from $\overline{RAS}$ Low (10)	t_{RAD}	15	35	15	40	20	50	ns
Row Address Setup Time	t_{ASR}	0		0		0		ns
Column Address Setup Time (11)	t_{ASC}	0		0		0		ns
Row Address Hold Time	t_{RAH}	10		10		15		ns
Column Address Hold Time	t_{CAH}	15		15		20		ns
Transition Time (12)	t_T	2	30	2	30	2	30	ns

NOTES:

7. The timing requirements are assumed t_T = 5ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
9. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max), access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max), access time is defined as t_{CAC} and t_{CAA} as shown in note 3.
10. t_{RAD} (max) is specified as a reference point only. If $t_{RAD} \geq t_{RAD}$ (max), access time is assumed by t_{CAA} for read cycle.
11. t_{ASC} (max) is specified as a reference point only of address access time.
12. t_T is measured between V_{IH} (min) and V_{IL} (max).

AC CHARACTERISTICS FOR READ OPERATIONS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C) Notes 1, 13, 14

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	130		150		190		ns
$\overline{RAS}$ Low Pulse Width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width	t_{CAS}	15	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	t_{CSH}	55		65		85		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	t_{RSH}	15		15		20		ns
Read Setup Time before $\overline{CAS}$ Low	t_{RCS}	0		0		0		ns
Read Hold Time after $\overline{CAS}$ High (1)	t_{RCH}	0		0		0		ns
Read Hold Time after $\overline{RAS}$ High (1)	t_{RRH}	0		0		0		ns
Column Address to $\overline{RAS}$ Setup	t_{RAL}	35		40		50		ns
Precharge to $\overline{CAS}$ Active	t_{RPC}	5		5		5		ns
Delay Time, Data to $\overline{OE}$ Low	t_{DOEL}	0		0		0		ns
Delay Time, $\overline{OE}$ High to Data	t_{OEHD}	20		20		25		ns

NOTES:

1. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

AC CHARACTERISTICS FOR WRITE OPERATIONS

(V_{CC} = 3.3V ±0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	130		150		190		ns
$\overline{RAS}$ Low Pulse Width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width	t_{CAS}	15	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	t_{CSH}	55		65		85		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	t_{RSH}	15		15		20		ns
Write Setup Time before $\overline{CAS}$ Low (1)	t_{WCS}	0		0		0		ns
Write Hold Time after $\overline{CAS}$ Low	t_{WCH}	12		15		20		ns
$\overline{CAS}$ Hold Time after $\overline{WE}$ Low	t_{CWL}	15		20		25		ns
$\overline{RAS}$ Hold Time after $\overline{WE}$ Low	t_{RWL}	15		20		25		ns
Write Pulse Width	t_{WP}	12		15		20		ns
Data Setup Time (1)	t_{DS}	0		0		0		ns
Data Hold Time after $\overline{CAS}$ Low (1)	t_{DH}	12		15		20		ns
Delay Time, $\overline{OE}$ High to Data	t_{OEHD}	20		20		25		ns
$\overline{OE}$ Hold Time after $\overline{WE}$ Low	t_{HWOE}	20		20		25		ns

1. t_{WCS} , t_{RWD}, t_{CWD}, and t_{AWD} do not define the limits of operation, but are included as electrical characteristics only. When $t_{WCS} \geq t_{WCS}$ (min), an early write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of the output (at the access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

AC CHARACTERISTICS FOR READ-WRITE OPERATIONS

(V_{CC} = 3.3V ±0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
Read-ModifyWrite Cycle Time	t_{RWC}	180		200		220		ns
$\overline{RAS}$ Low Pulse Width	t_{RASRW}	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width	t_{CASRW}	20	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	t_{CSHRW}	55		65		85		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	t_{RSHRW}	15		15		20		ns
Read Setup Time before $\overline{CAS}$ Low	t_{RCS}	0		0		0		ns
$\overline{CAS}$ Low to $\overline{WE}$ Low Delay (1)	t_{CWD}	45		45		50		ns
$\overline{RAS}$ Low to $\overline{WE}$ Low Delay (1)	t_{RWD}	90		105		120		ns
$\overline{CAS}$ Hold after $\overline{WE}$ Low	t_{CWL}	15		20		25		ns
$\overline{RAS}$ Hold after $\overline{WE}$ Low	t_{RWL}	15		20		25		ns
Write Pulse Width	t_{WP}	12		15		20		ns
Data Setup Time	t_{DS}	0		0		0		ns
Data Hold Time after $\overline{CAS}$ Low	t_{DH}	12		15		20		ns
Address to $\overline{WE}$ Low Delay (1)	t_{AWD}	65		70		80		ns
Delay Time, $\overline{OE}$ High to Data	t_{OEHD}	20		20		25		ns
$\overline{OE}$ Hold Time after Write Low	t_{HWOE}	20		20		25		ns

1. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} do not define the limits of operation, but are included as electrical characteristics only. When $t_{WCS} \geq t_{WCS}$ (min), an early write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of the output (at the access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

PAGE MODE OPERATIONS

(V_{CC} = 3.3V ±0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
EDO Page Mode Cycle Time	t_{PC}	35		40		50		ns
EDO Page Mode for R/W, R/M/W Cycle Time	t_{PRWC}	85		90		100		ns
$\overline{RAS}$ Low Pulse Width for Read, Write Cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns
$\overline{CAS}$ Low Pulse Width for Read Cycle	t_{CAS}	15	100,000	20	100,000	25	100,000	ns
$\overline{CAS}$ Pulse Width (Page Mode)	t_{CP}	10		10		10		ns
$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	t_{RSH}	15		15		20		ns

WRITE REFRESH OPERATIONS *

(V_{CC} = 3.3V ±0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		-80		-100		Units
		Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Setup for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	5		10		10		ns
$\overline{CAS}$ Hold for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	15		15		15		ns
Precharge to $\overline{CAS}$ Active	t_{RPC}	5		5		5		ns
Write Setup Time	t_{WRP}	10		10		10		ns
Write Hold Time	t_{WRH}	10		10		10		ns

* Eight or more CAS before RAS cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

GENERAL DESCRIPTION

The 4M x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. $\overline{RAS}$ is used to latch the row address. Once the page has been opened by $\overline{RAS}$, $\overline{CAS}$ is used to latch the column address. Read and Write cycles are selected with the $\overline{WE}$ input. A logic High on $\overline{WE}$ dictates Read mode while a logic Low on $\overline{WE}$ dictates Write mode. During a Write cycle, data-in (I) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes Low prior to $\overline{CAS}$ going Low, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle, regardless of $\overline{OE}$.

A logic High on $\overline{WE}$ dictates Read mode while logic Low on $\overline{WE}$ dictates Write mode. During a Write cycle, data-in is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. An Early Write occurs when $\overline{WE}$ is taken Low prior to $\overline{CAS}$ falling. A Late Write or Read-Modify-Write occurs when $\overline{WE}$ falls after $\overline{CAS}$ was taken Low. During Early Write cycles, the outputs (O) will remain High-Z regardless of the state of $\overline{OE}$. During Late Write or Read-Modify-Write cycles, $\overline{OE}$ must be taken High to disable the data outputs prior to applying input data. If a Late Write or Read-Modify-Write is attempted while keeping $\overline{OE}$ Low, no write will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

PAGE ACCESS

Page operations allow faster data operations (Read, Write or Read-Modify-Write) within a row-address-defined page boundary. The Page cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ Low and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ High terminates the Page Mode operation, i.e. closes the page.

EDO PAGE MODE

The 4M x 4 EDO DRAM provides EDO Page Mode, which is an accelerated Fast Page Mode cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ returns High. EDO allows $\overline{CAS}$ precharge time (t_{CP}) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control allows pipeline Reads.

Fast Page Mode DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO Page Mode DRAMs operate like Fast Page Mode DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes High during Reads, provided $\overline{RAS}$ and $\overline{OE}$ are held Low. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are Low, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes High while $\overline{RAS}$ remains Low, data will transition to and remain High-Z. $\overline{WE}$ can also perform the function of disabling the output devices under certain conditions.

During an application, if the I/O outputs are wire OR'd $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ high time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after t_{OFF}, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

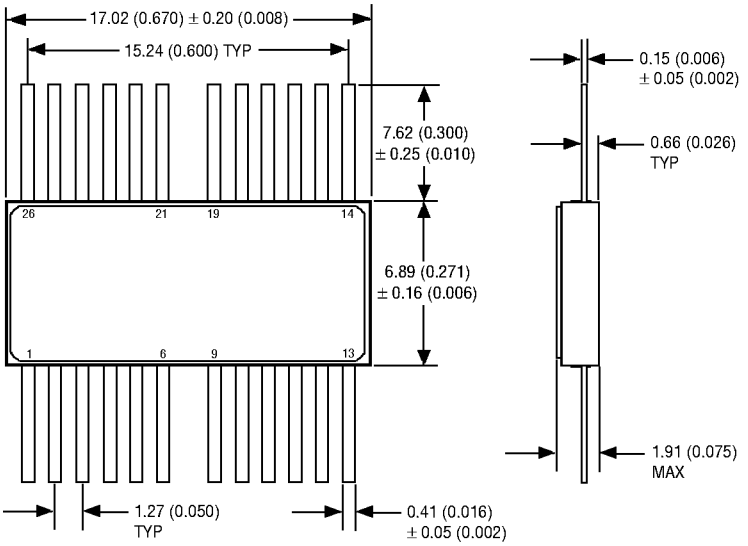
REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (Read, Write) or $\overline{RAS}$ refresh CYCLE ($\overline{RAS}$-only, CBR, or Hidden) so that all combinations of $\overline{RAS}$ addresses (2,048) are executed within tREF (max), regardless of sequence. The CBR Refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

STANDBY

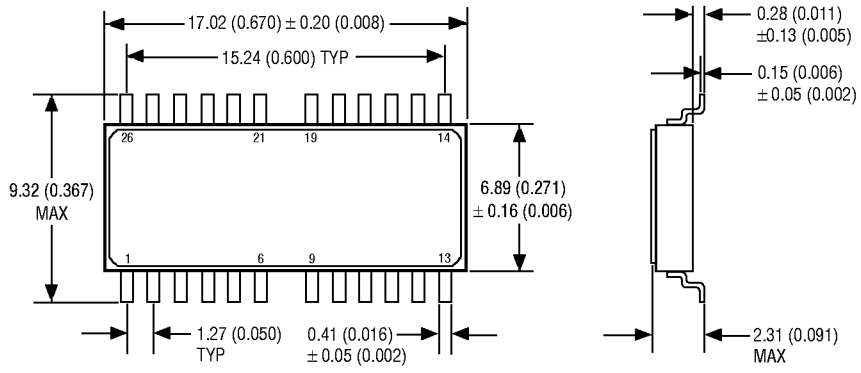
Returning $\overline{RAS}$ and $\overline{CAS}$ High terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{RAS}$ High time.

PACKAGE DIMENSION: 24/26 PIN, CERAMIC FLATPACK (FP)



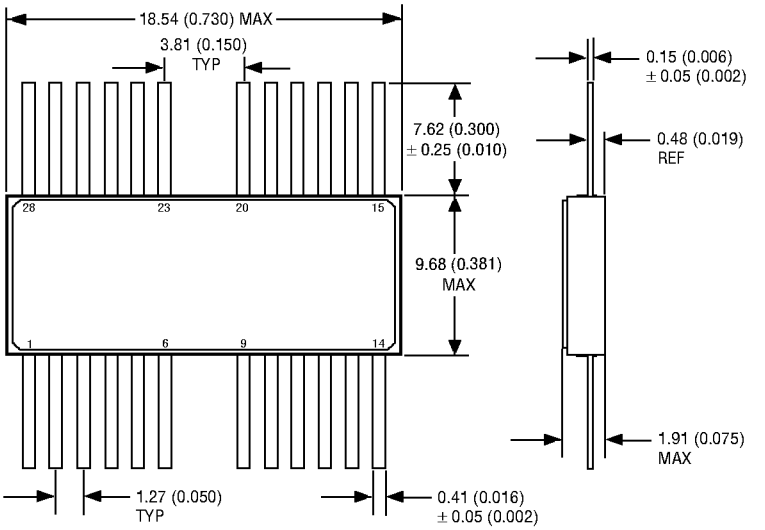
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 24/26 PIN, CERAMIC FLATPACK, LEAD FORMED (F1)



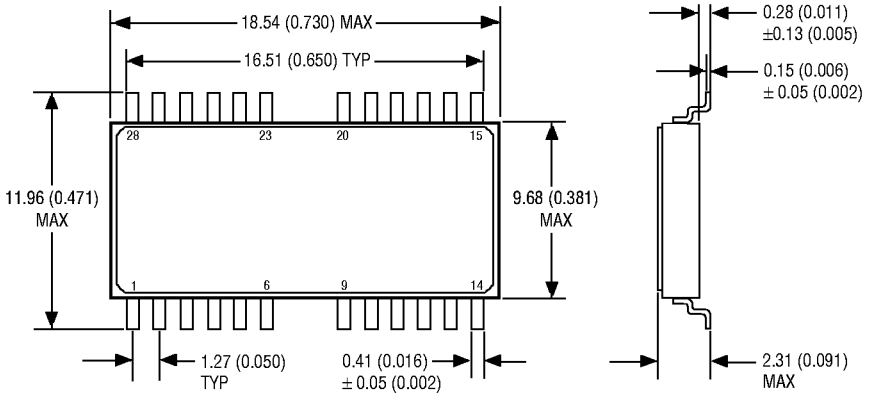
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 24/28 PIN, CERAMIC FLATPACK (FB)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 24/28 PIN, CERAMIC FLATPACK, LEAD FORMED (F2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION