Revision Date: May 5, 1997

AP9A401

512 x 9 CMOS FIFO

Features

- Fast access times: 15, 20, 25, 35 ns
- Full CMOS dual-port memory array
- Asynchronous read and write
- Expandable-in width and depth
- Full, half-full and empty status flags
- Read retransmit capability
- TTL-compatible I/O
- 32-Pin PLCC package
- Functionally compatible with the IDT7201

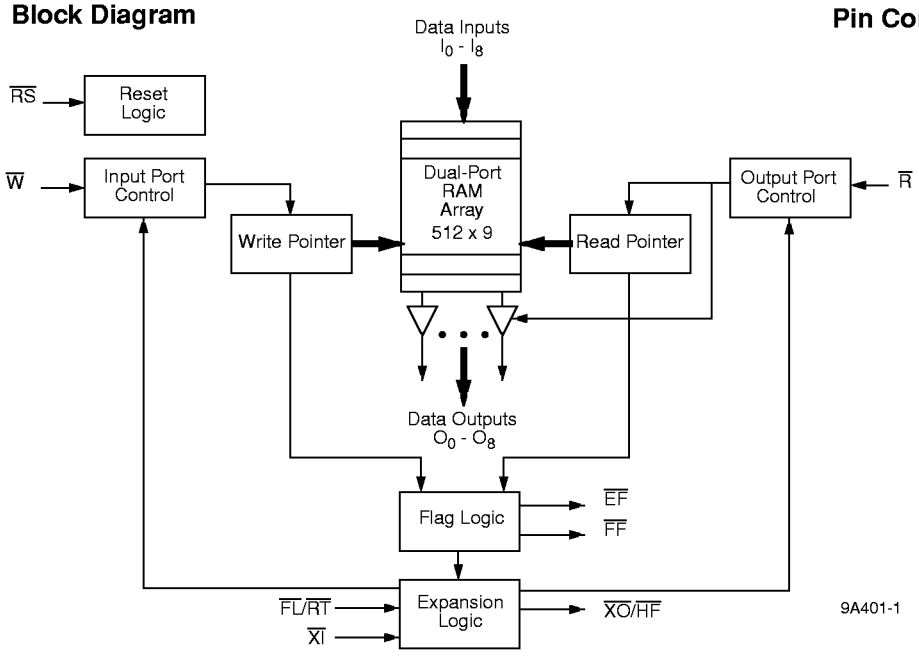
Functional Description

The AP9A401 is a dual-port memory with internal addressing to implement a first-in, first-out algorithm. Through an advanced dual-port architecture, it provides a fully asynchronous read/write operation. Empty, full and half-full status flags are provided to prevent data overflow and underflow. In addition, internal logic provides for unlimited expansion in both word size and depth.

Read and write operations automatically access sequential locations in memory so that data is read out in the same order that it was written. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, full and half-full status flags monitor the data that has been written into the FIFO, and prevent improper operations (i.e., a Read if the FIFO is empty, or a write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion-in and expansion-out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

Block Diagram



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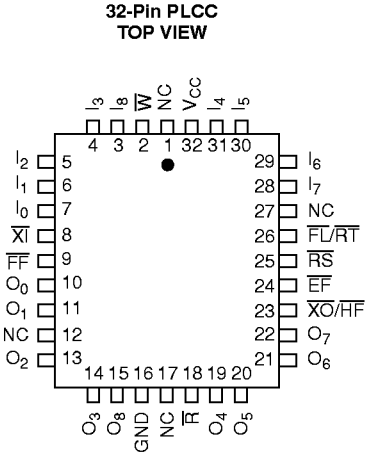
Pin Configuration



9A401-2

Selection Guide

	AP9A401-15	AP9A401-20	AP9A401-25	AP9A401-35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)	100	100	100	100
Maximum Standby Current (mA)	15	15	15	15

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C
V_{CC} Supply Relative to GND ..... -0.5 V to +7 V
Short Circuit Output Current[1] ..... ±50 mA

Voltage on any Pin Relative to GND[2, 3] .. -0.5 to V_{CC} +0.5 V
DC Voltage Applied to Outputs
in High-Z State[3] ..... -0.5 to V_{CC} +0.5 V
Power Dissipation ..... 1.0 W

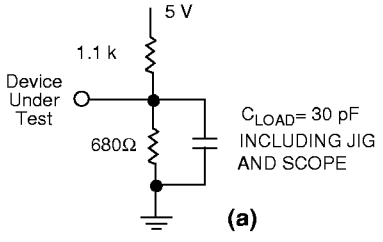
Electrical Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

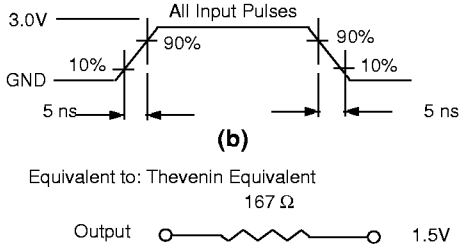
Symbol	Parameter	Test Conditions	9A401-15		9A401-20		9A401-25		9A401-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Supply Current[4]	Measured at f = 40 MHz		100		100		100		100	mA
I_{CC2}	Standby Current[4]	All Inputs = V_{IN}		15		15		15		15	mA
I_{CC3}	Power Down Current[4]	All Inputs = V_{CC} -0.2 V		5		5		5		5	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	-10	10	-10	10	-10	10	-10	10	A
I_{LO}	Output Leakage Current	$\overline{R} \ge V_{IH}$, $0 V \le V_{OUT} \le V_{CC}$	-10	10	-10	10	-10	10	-10	10	A
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Capacitance[5, 6]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	I/O Capacitance	7	pF

AC Test Loads and Waveforms





Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Not to exceed +7 V.
4. I_{CC}, I_{CC2} and I_{CC3} are dependent upon output loading and cycle rates. Specified values are with outputs open.
5. Sample tested only
6. Capacitances are maximum values at 25 C measured at 1.0 MHz with V_{IN} = 0 V.

Switching Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)[7]

Parameter	Description	9A401-15		9A401-20		9A401-25		9A401-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_A	Access Time		15		20		25		35	ns
t_{RR}	Read Recover Time	10		10		10		10		ns
t_{RPW}	Read Pulse Width[8]	15		20		25		35		ns
t_{RLZ}	Data Bus Active from Read LOW[9]	5		5		5		5		ns
t_{WLZ}	Data Bus Active from Write HIGH[9, 10]	10		10		10		10		ns
t_{DV}	Data Valid from Read Pulse HIGH	5		5		5		5		ns
t_{RHZ}	Data Bus High-Z from Read HIGH[9]		15		15		15		15	ns
Write Cycle										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{WPW}	Write Pulse Width[8]	15		20		25		35		ns
t_{WR}	Write Recovery Time	10		10		10		10		ns
t_{SD}	Data Set-up Time	10		10		10		15		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
Reset Timing										
t_{RSC}	Reset Cycle Time	25		30		35		45		ns
t_{RS}	Reset Pulse Width	15		20		25		35		ns
t_{RSR}	Reset Recovery Time	10		10		10		10		ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15		20		25		35		ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15		20		25		35		ns
Retransmit Timing										
t_{RTC}	Retransmit Cycle Time	25		30		35		45		ns
t_{RT}	Retransmit Pulse Width[8]	15		20		25		35		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		ns
Flag Timing										
t_{EFL}	Reset LOW to Empty Flag LOW		25		30		35		45	ns
$t_{HFH, FFH}$	Reset LOW to Half-Full and Full Flags HIGH		25		30		35		45	ns
t_{REF}	Read LOW to Empty Flag LOW		20		25		25		35	ns
t_{RFF}	Read HIGH to Full Flag HIGH		20		25		25		35	ns
t_{WEF}	Write HIGH to Empty Flag HIGH		20		25		25		35	ns
t_{WFF}	Write LOW to Full Flag LOW		20		25		25		35	ns
t_{WHF}	Write LOW to Half-Full Flag LOW		25		30		35		45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH		25		30		35		45	ns
Expansion Timing										
t_{XOL}	Expansion Out LOW		18		20		25		35	ns
t_{XOH}	Expansion Out HIGH		18		20		25		35	ns
t_{XI}	Expansion In Pulse Width	15		20		25		35		ns
t_{XIR}	Expansion In Recovery Time	10		10		10		10		ns
t_{XIS}	Expansion In Set-up Time	7		10		10		15		ns

Notes:

7. All timing measurements performed at 'AC Test Condition levels.
8. Pulse widths less than minimum value are not allowed.
9. Guaranteed but not tested.
10. Only applies to read data flow-through mode.

Operational Description

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data set-up and hold times must be observed on the data in (I_0 - I_8) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation that fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. It is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (O_0 - O_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ that accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when $\overline{W}$ is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$, which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 512 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

Operational Modes

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single Mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple AP9A401 devices in parallel. Each device should be configured for stand-alone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices (See *Figures 1 and 2*).

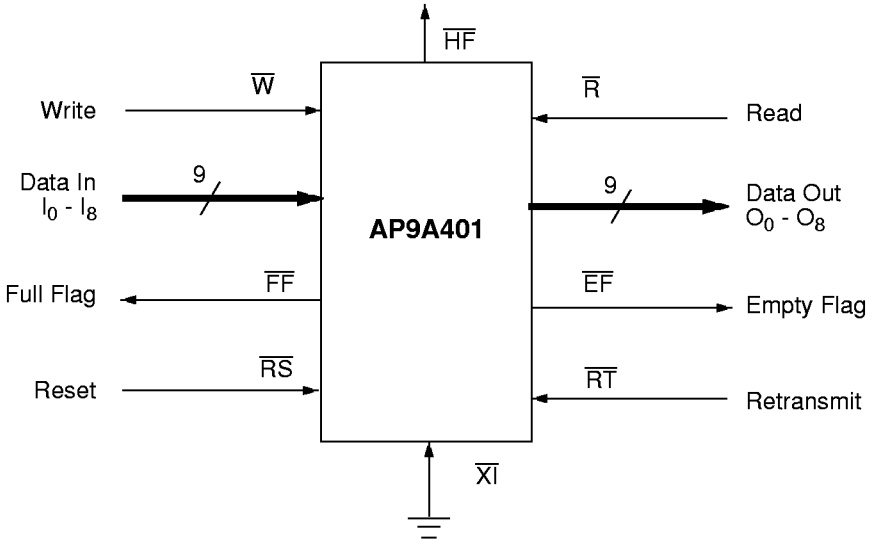


Figure 1. Single FIFO (512 x 9)

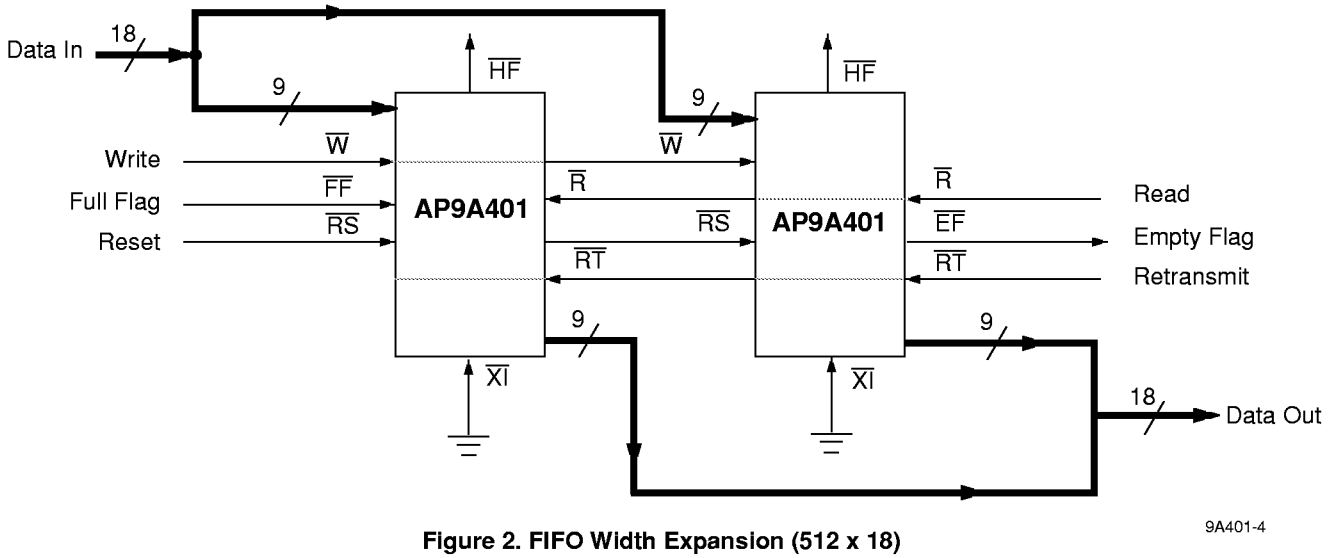


Figure 2. FIFO Width Expansion (512 x 18)

Operational Modes (continued)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices msut have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$, and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices, respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

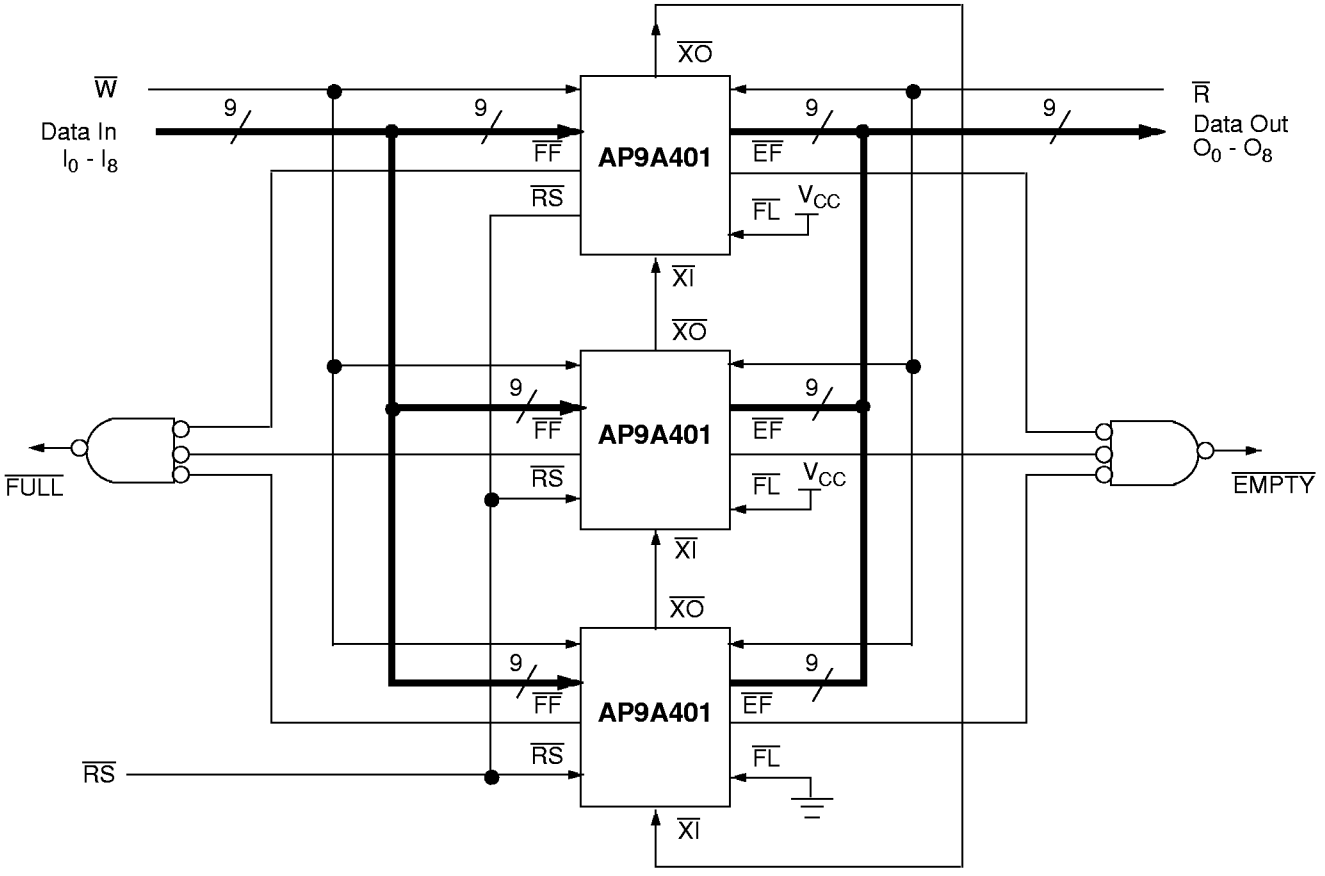


Figure 3. FIFO Depth Expansion (1536 x 9)

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Operational Modes (continued)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications that require bidirectional data buffering between two systems can be realized by operating AP9A401 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care msut be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

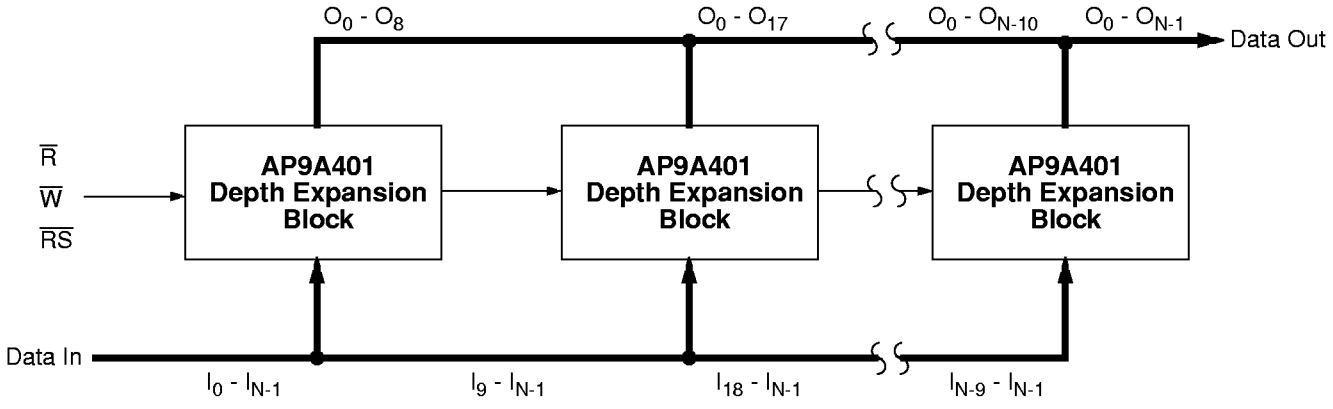

Figure 4. Compound FIFO Expansion

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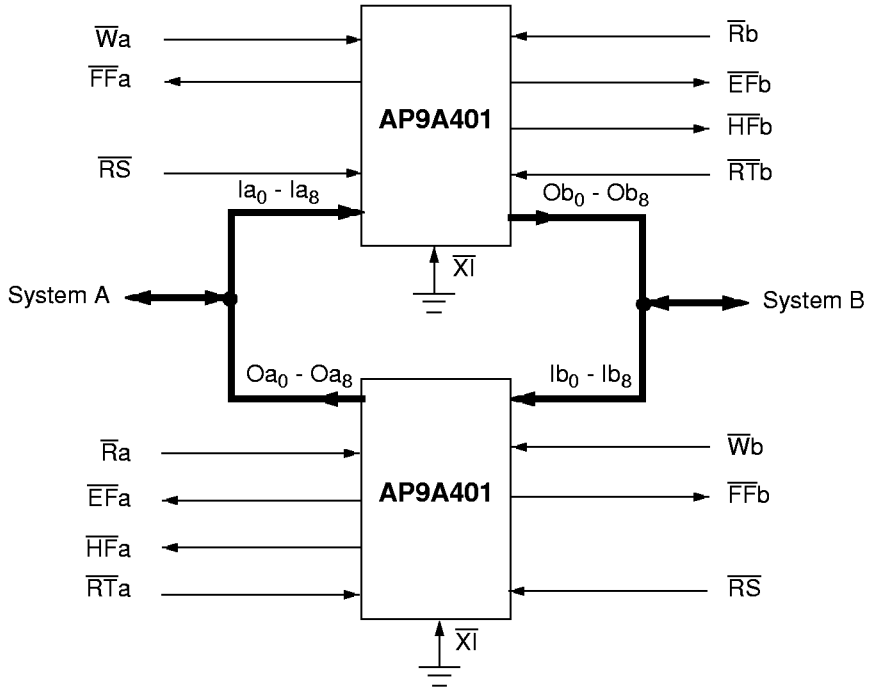

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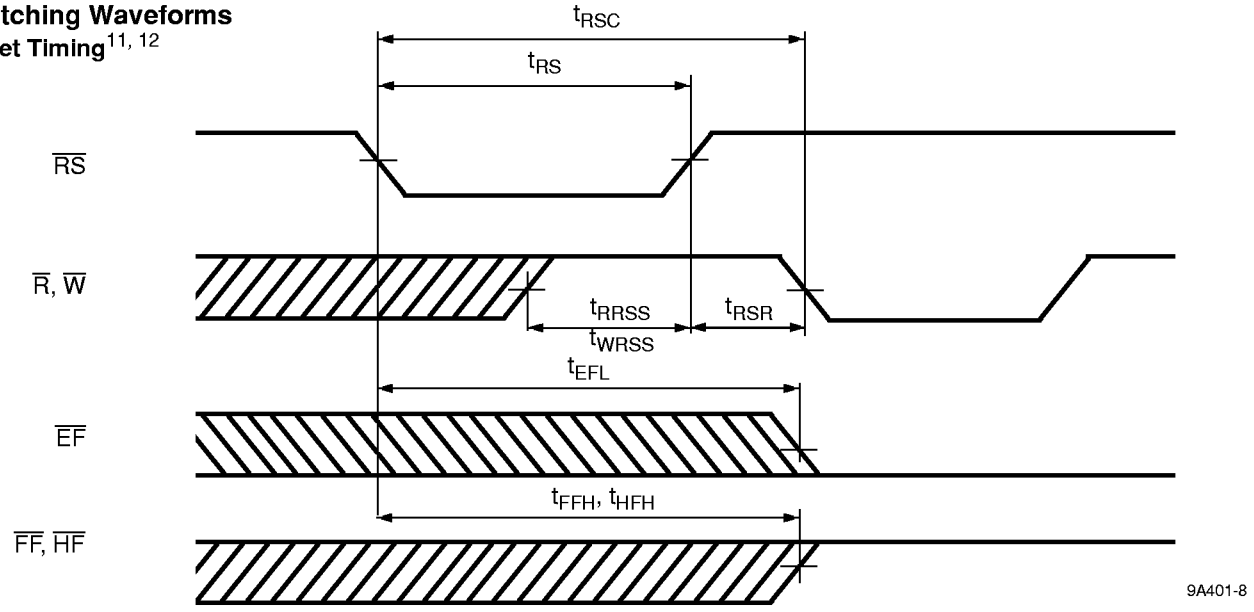
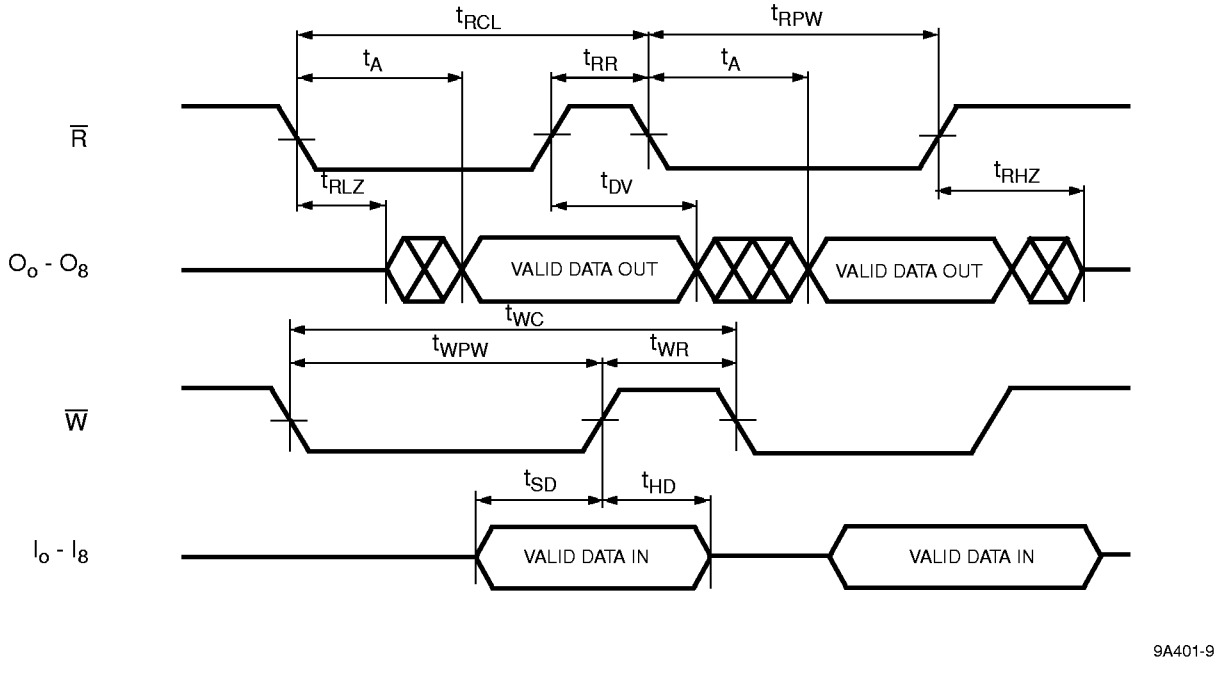
Figure 5. Bidirectional FIFO Buffer

Switching Waveforms

Reset Timing[11, 12]



Asynchronous Write and Read Operation

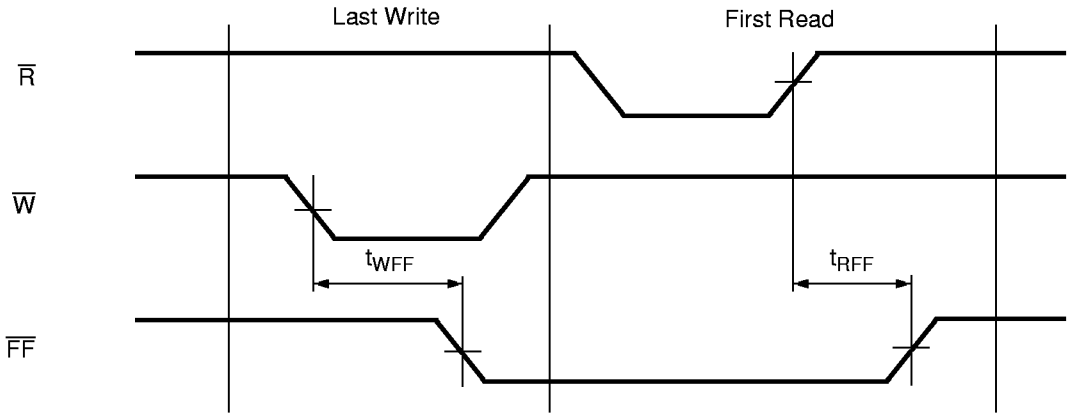


Notes:

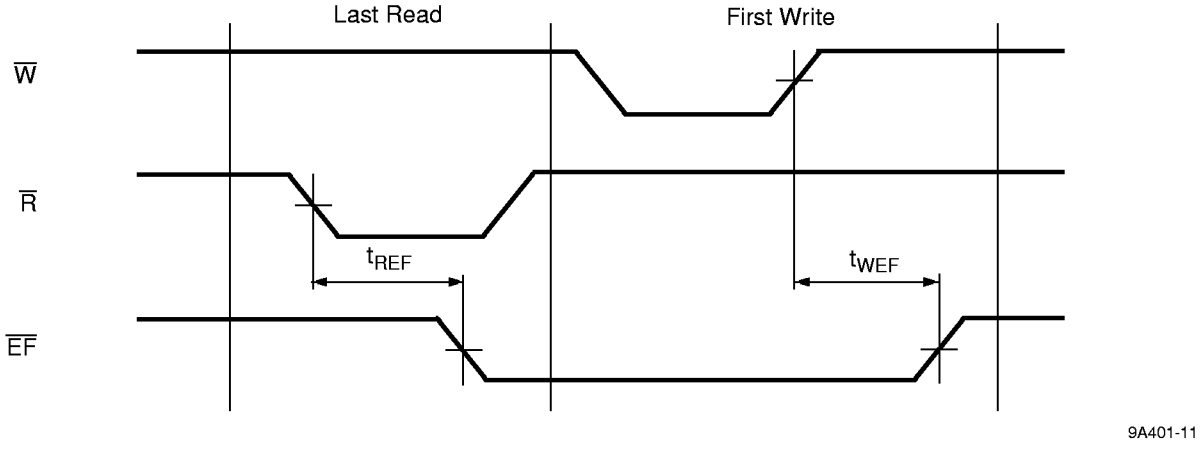
11. $t_{RSC} = t_{RS} + t_{RSR}$.
12. $\overline{W}$ and $\overline{R}$ $_{IN}$ around the rising edge of $\overline{RS}$.

Switching Waveforms (continued)

Full Flag from Last Write to First Read

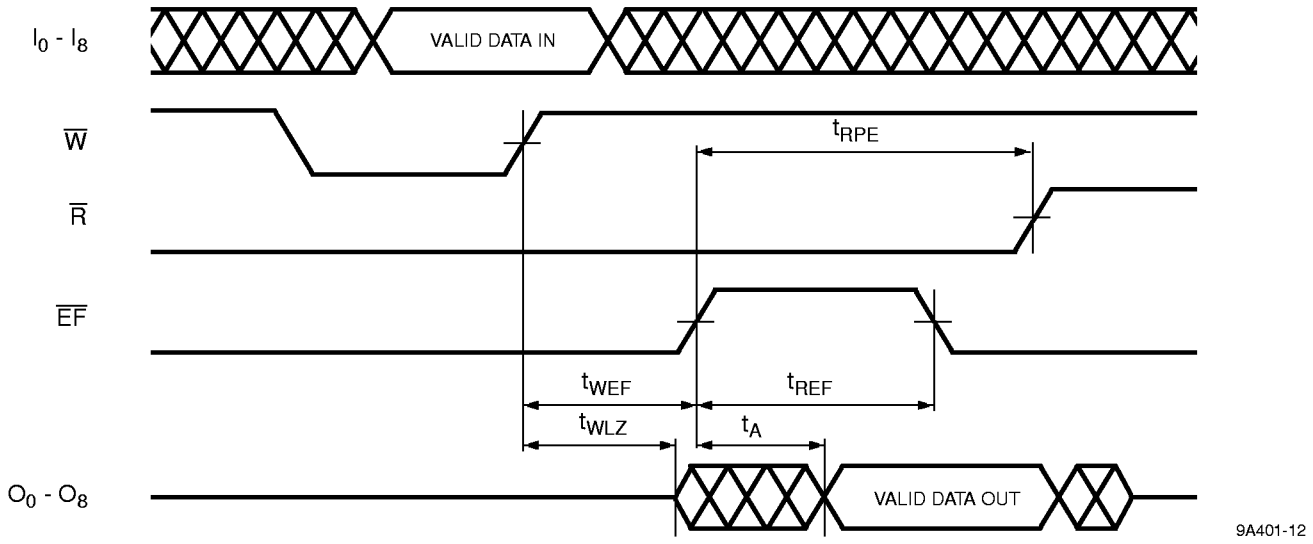


Empty Flag from Last Read to First Write

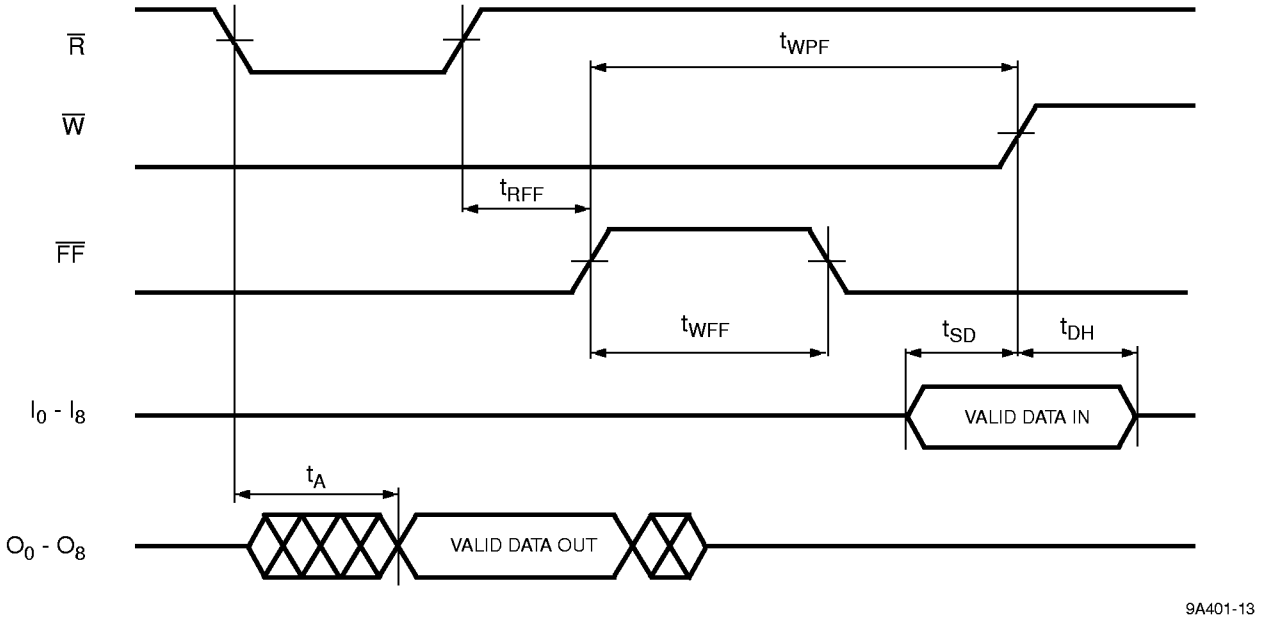


Switching Waveforms (continued)

Read Data Flow-Through



Write Data Flow-Through[13, 14]

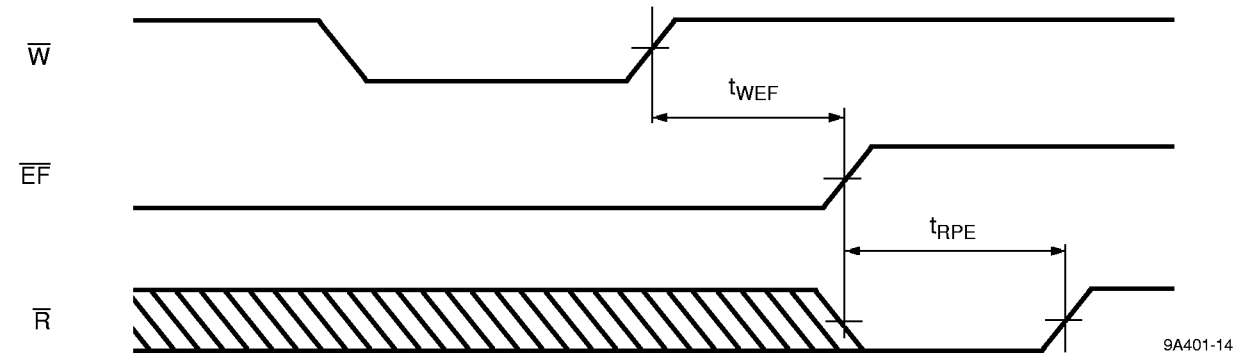


Notes:

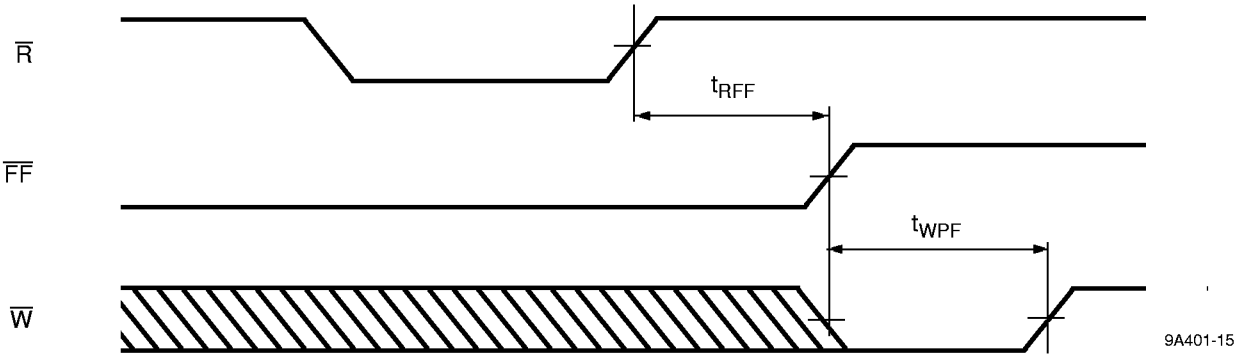
13. $t_{WPF} = t_{WPW}$
14. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

Switching Waveforms (continued)

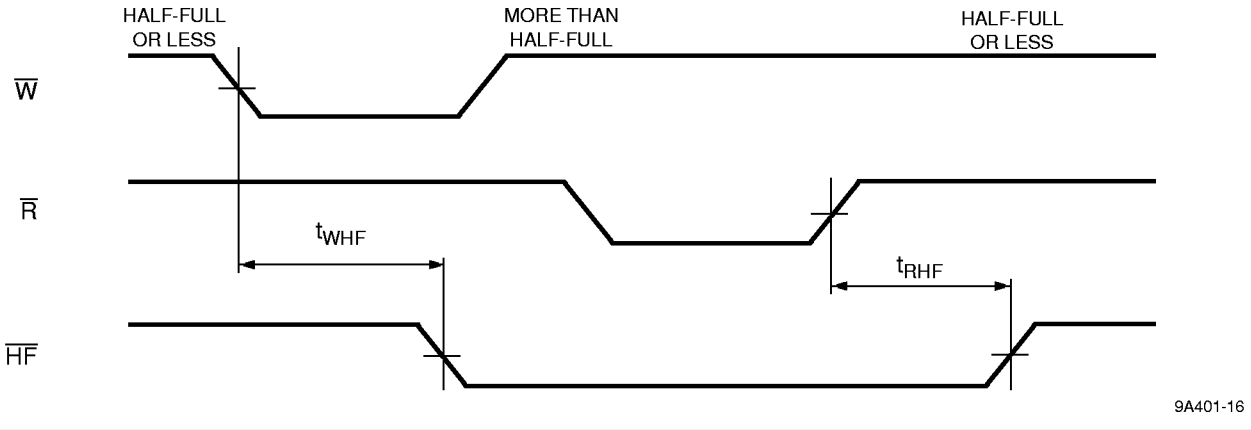
Empty Flag Timing [15, 16]



Full Flag Timing [13, 14]



Half-Full Flag Timing

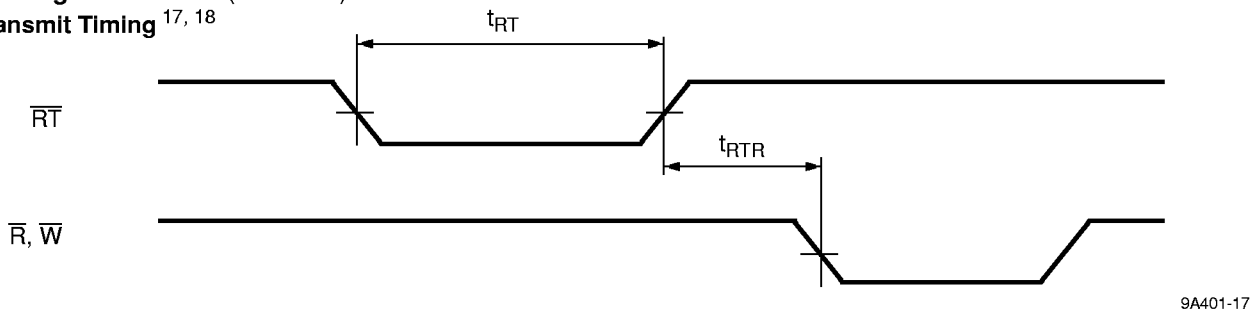


Notes:

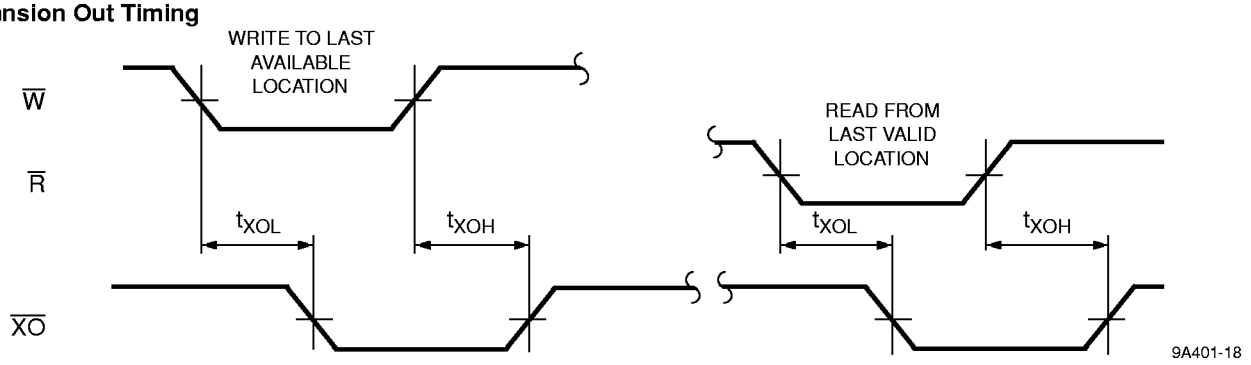
15. $t_{RPE} = t_{RPW}$.
16. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

Switching Waveforms (continued)

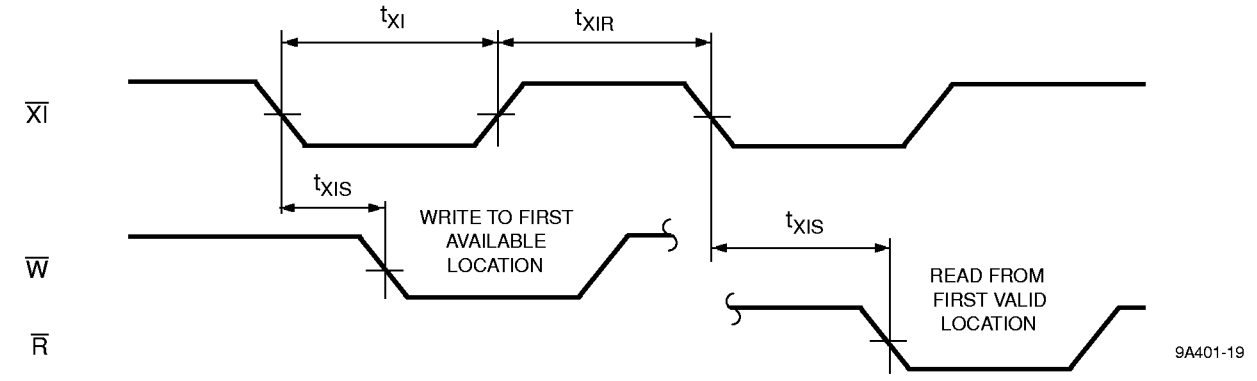
Retransmit Timing [17, 18]



Expansion Out Timing



Expansion In Timing



Notes:

17. $t_{RTC} = t_{RT} + t_{RTR}$
18. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit, but flags will be valid at t_{RTC}.

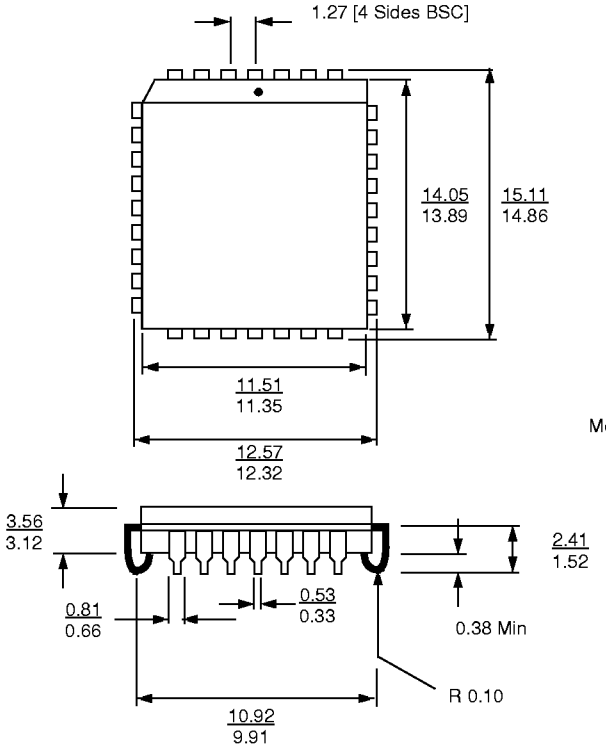
Ordering Information

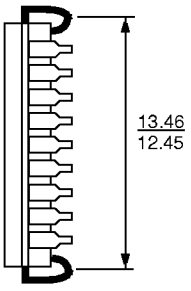
Speed	Part Number	Package Name	Package Type
15	AP9A401-15JC	J32.1	32-Pin Plastic Leaded Chip Carrier
20	AP9A401-20JC	J32.1	32-Pin Plastic Leaded Chip Carrier
25	AP9A401-25JC	J32.1	32-Pin Plastic Leaded Chip Carrier
35	AP9A401-35JC	J32.1	32-Pin Plastic Leaded Chip Carrier

Document # DS-00021-Rev A

Package Diagrams

J32.1 - 32-Pin Plastic Leaded Chip Carrier (PLCC)





Measurements are in Millimeters unless otherwise specified. (MAX / MIN)