

AK5328192WP 8,388,608 by 32 B it CMOS Dynamic Random Access Memory

DESCRIPTION

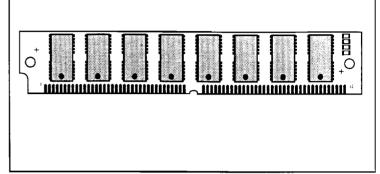
The Accutek AK5328192WP high density memory module is a CMOS dynamic RAM organized in 8192K x 32 bit words. The module consists of sixteen standard 4 Meg x 4 DRAMs in plastic SOJ packages. The assembly has 8 drams mounted on the front side and 8 drams mounted on the back side of a printed circuit board in a 72 pad leadless SIM configuration.

This configuration allows socket-mounting of large quantities of memory in applications where high density and ease of inserting additional memory are important.

The operation of the AK5328192 is identical to sixteen 4M x 4 Drams. There are four \overline{CAS} lines and four \overline{RAS} lines. On each bank of 4M x 32, independent byte control is accomplished by four \overline{CAS} lines. Each separate \overline{CAS} line controls two 4M x 4 Drams to form an 8 bit byte. Two banks of 32 bits are controlled by the two pairs of \overline{RAS} lines. A sixteen bit data path can be produced by connecting $\overline{DQ_0}$ to $\overline{DQ_{16}}$, $\overline{DQ_1}$ to $\overline{DQ_{17}}$, etc. and alternately strobing $\overline{RAS_0}$ with $\overline{RAS_1}$ and $\overline{RAS_2}$ with $\overline{RAS_3}$.

FEATURES

- 8,388,608 x 32 bit organization
- 72 pad Single In-Line Module
- Multiple CAS and RAS lines allow x16 or x32 bit widths
- CAS-before-RAS, RAS-only or hidden refresh
- Power
 5.32 Watt Max Active (60nS)
 4.48 Watt Max Active (70 nS)
 88 mW Max Standby



- Operating free air temperature 0°C to 70°C
- · Single 5 Volt Power Supply
- 2048 Refresh Cycles, 32 mSEC
- 4096 Refresh Cycles, 64 mSEC available for all module sizes
- Available in Fast Page Mode, EDO and Static Column mode
- Available in leadless (W) or leaded Zip (Z) versions
- Downward compatible with AK5324096W through AK532256W sizes

EXAMPLES

AK5328192WP-60

8Meg x 32 CMOS Dynamic RAM, SIM, Page Mode, Commercial 60 nSEC Access Time

PIN NOMENCLATURE

PIN NOWENCLATONE				
A ₀ - A ₁₀	Address Inputs			
DQ ₀ - DQ ₃₁	Data In/Data Out			
CAS ₀ - CAS ₃	Column Address Strobe			
RAS ₀ - RAS ₃	Row Address Strobe			
WE	Write Enable			
ŌĒ	Output Enable			
PD1 - PD4	Presence Detect			
Vcc	5v Supply			
Vss	Ground			
NC	No Connect			

MODULE OPTIONS

Leadless SIM: AK5328192W	
Leaded ZIP: AK5328192Z	

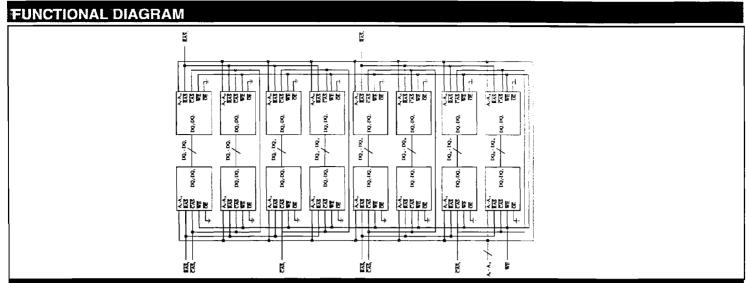
PIN ASSIGNMENT

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	Vss	57	DQ12
4	DQ1	22	DQ5	40	CAS ₀	58	DQ28
5	DQ17	23	DQ21	41	CAS ₂	59	Vcc
6	DQ2	24	DQ6	42	CAS3	60	DQ29
7	DQ18	25	DQ22	43	CAS1	61	DQ13
8	DQ3	26	DQ7	44	RAS0	62	DQ30
9	DQ19	27	DQ23	45	RAS1	63	DQ14
10	Vcc	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	WE	65	DQ15
12	A 0	30	Vcc	48	NC	66	NC
13	A 1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	А3	33	RAS3	51	DQ9	69	PD3
16	A4	34	RAS2	52	DQ25	70	PD4
17	A 5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	Vss

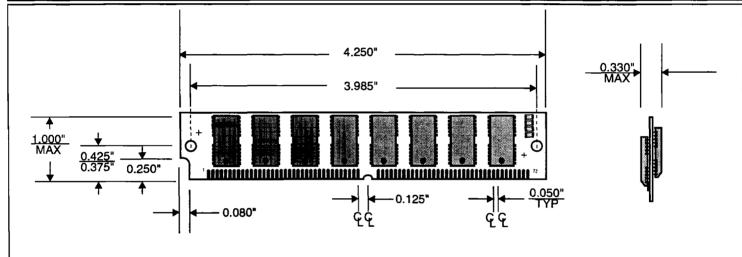
Presence Detect -

	-60	-70
PD1	NC	NC
PD2	Vss	Vss
PD3	NC	Vss
PD4	NC	NC





MECHANICAL DIMENSIONS



ORDER INFORMATION

PART NUMBER CODING INTERPRETATION

Position 1 2 3 4 5 6 7 8 **Product**

AK = Accutek Memory

2 Type

> 4 = Dynamic RAM

= CMOS Dynamic RAM 5

= Static RAM

Organization/Word Width

1 = b y 1 16 = by 16

32 = by 32 4 = by 4

8 = by 836 = by 36

9 = by 9

Size/Bits Depth

64K 4096 4 MEG 64 = = 256K 8192 8 MEG 1024 = 1 MEG16384 = 16 MEG

The numbers and coding on this page do not include all variations available, but are shown as examples of the most widely used variations. Contact Accutek if other information is required.



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Position

2 3 4 5 6 7 8

5 Package Type

G = Single In-Line Package (SIP)

S = Single In-Line Module (SIM)

D = Dual In-Line Package (DIP)

W = .050 inch Pitch Edge Connect

Z = Zig-Zag In-Line Package (ZIP)

Special Designation

P = Page Mode

N = Nibble Mode

Static Column Mode

W = Write Per Bit Mode

V = Video Ram

Separator

= Commercial 0°C to +70°C

Military Equivalent Screened

(-55°C to +125°C)

Industrial Temperature Tested (-45°C to +85°C)

X = Burned In

Speed (first two significant digits)

DRAMS SRAMS

60 nS 60 12 =12 nS 70 nS = 20 =20 nS

80 nS 25 =25 nS 80

100 nS 35 =35 nS

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