27HC191/27HC291

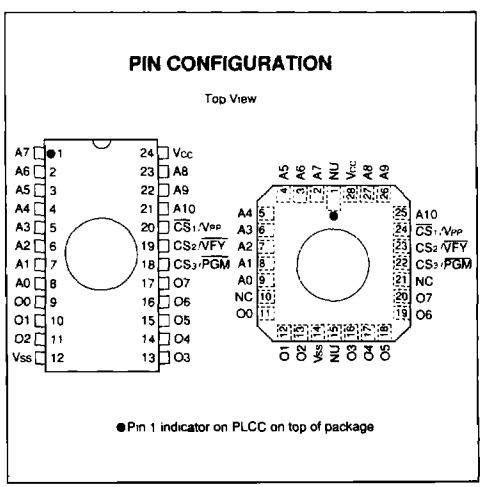
16K (2K x 8) High Speed CMOS UV Erasable PROM

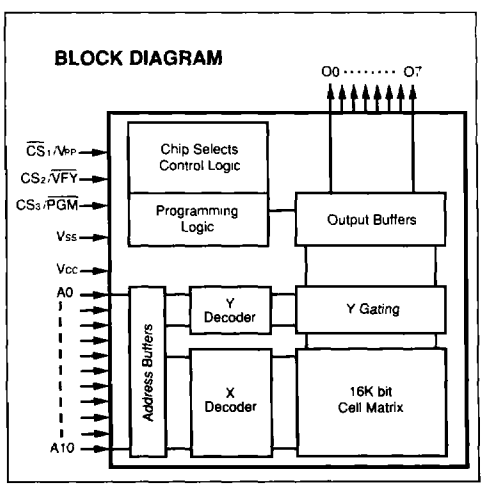
FEATURES

- Bipolar performance
  —35ns Access time available
- CMOS technology for low power consumption
  —65mA Active current
  —100μA Standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  —Fast programming
  —Express
- Organized in 2K x 8: bipolar PROM pinouts
  —24-pin Dual-in-line package
  —28-pin Chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Military**: -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27HC191 and 27HC291 are CMOS 16K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The devices are organized into 2K words of 8 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further reduction in the standby power requirement to 100μA. The 27HC191/27HC291 EPROMS are fully tested and then erased before shipment. This ensures the highest possible yield to the customer pattern. The 27HC191/27HC291 are configured in a standard bipolar PROM pinout which allows an easy upgrade for present 16K Bipolar PROM users. The 27HC191 is packaged in a standard 600 mil DIP and the 27HC291 is packaged in a 300 mil DIP. One Time Programming (OTP) is available for low cost (plastic) applications. The 27HC191/27HC291 allow DSP and other high performance microprocessors to run at full speed without the need of wait states. CMOS design and processing make this part suitable for applications where reliability and reduced power consumption are essential.





**See 27HC191/27HC291 Military Data Sheet DS60008

PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CS_1}$/VPP	Chip Select/Program Voltage
CS2/$\overline{VFY}$	Chip Select/Program Verify
CS3/$\overline{PGM}$	Chip Select/Program
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS ... -0.6V to +7.25V
$\overline{CS_1}$/VPP voltage w.r.t. during programming ... -0.6V to +14V
Voltage on A9 w.r.t. VSS ... -0.6V to +13.5V
Output voltage w.r.t. VSS ... -0.6V to VCC+1.0V
Temperature under bias ... -65° C to 125° C
Storage temperature ... -65° C to 150° C
Maximum exposure to UV ... 7258Wsec/cm²
ESD Protection on all pins ... 2kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to +70° C
Industrial: Tamb= -40° C to +85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -4mA IOL = 16mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V; Tamb = 25° C; f = 1MHz
Power Suppy Current, Active	S,L SX,LX	TTL input TTL input	ICC1 ICC2		70 80	mA mA	VCC = 5.5V; f = 2MHz; $\overline{CS_1}$/VPP = VIL; CS2/$\overline{VFY}$ = CS3/$\overline{PGM}$ = VIH; Iout = 0mA; VIL = -0.1V to 0.8V; VIH = 2.0V to VCC; Note 1
Power Supply Current, Standby	S SX		ICC(S)1		40 45	mA mA	
Power Supply Current, Standby	L LX L, LX	TTL input TTL input CMOS input	ICC(S)2		2 3 100	mA mA µA	$\overline{CS_1}$/VPP = VCC ±0.2V

* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 2 MHz: 4mA/5MHz

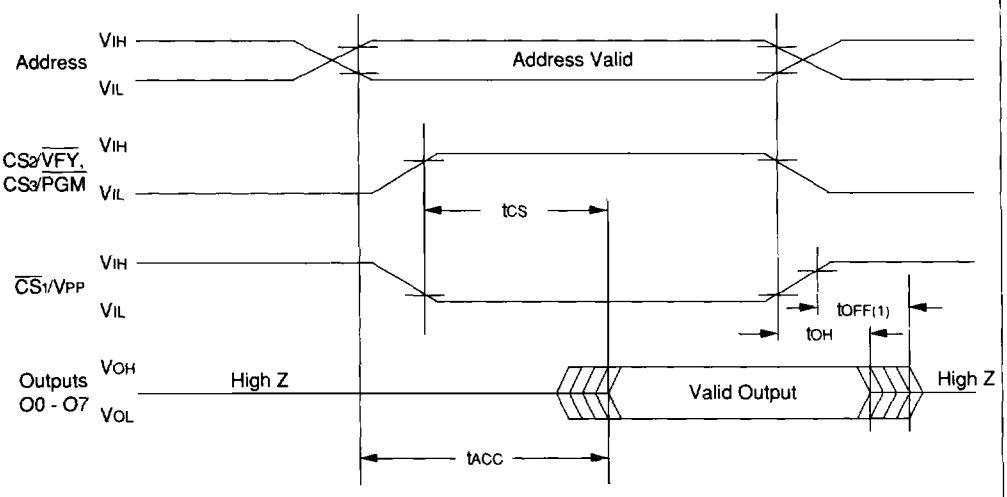
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load +30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Sym	27HC191/ 27HC291-35		27HC191/ 27HC291-40		27HC191/ 27HC291-45		27HC191/ 27HC291-55		Units	Conditions
			Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		35		40		45		55	ns	
CS to Output Delay	S L	t_{CS1} t_{CS2}		25 35		30 40		30 45		40 55	ns	Note 1
CS to O/P High Impedance	all	t_{OFF}	0	25	0	30	0	30	0	40	ns	Note 2
Output Hold from Address or CS, whichever occurs first	all	t_{OH}	0		0		0		0		ns	

*Parts: S = Standard Power; L = Low Power
Note 1: t_{CS1}, t_{CS2} to be specified from $\overline{CS_1}/V_{PP}$, $CS_2/\overline{VFY}$ and $CS_3/\overline{PGM}$, whichever occurs last
Note 2: t_{OFF} is specified from $\overline{CS_1}/V_{PP}$, $CS_2/\overline{VFY}$, or $CS_3/\overline{PGM}$ whichever occurs first

READ WAVEFORMS



Note: (1) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
For $\overline{CS}_1/V_{PP}$ and V_{CC} Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 4mA I_{OL} = 16mA
V_{CC} Current, program & verify		I_{CC}		65	mA	
V_{PP} Current, program		I_{PP}		30	mA	
A9 Product Identification		V_H	11.5	12.5	V	

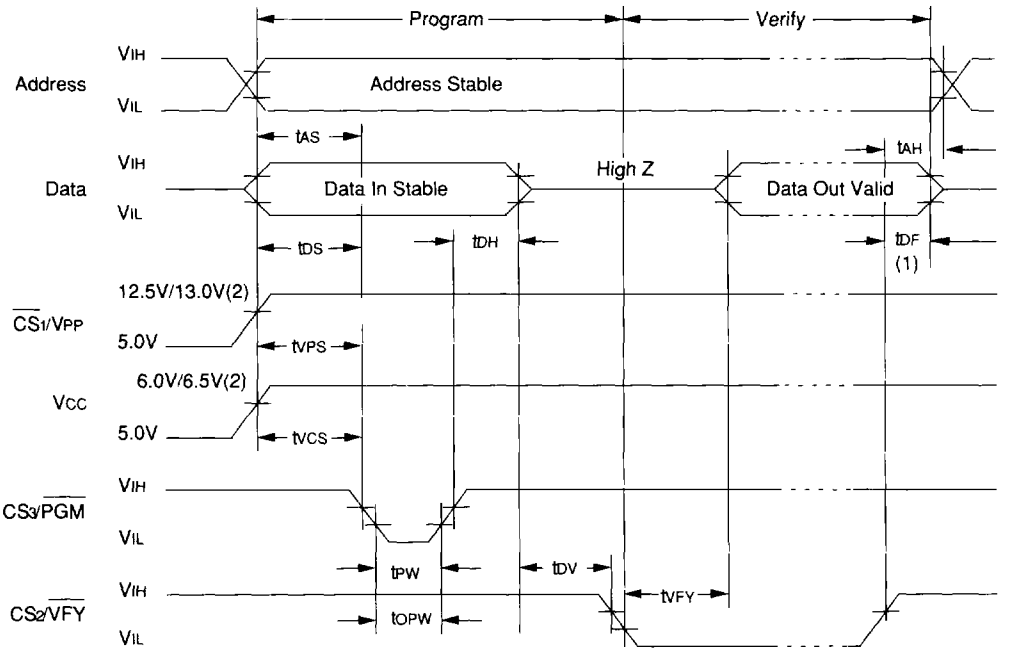
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
For $\overline{CS}_1/V_{PP}$ and V_{CC} Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (3)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	0.95	1.05	ms	1 ms typical
Program Pulse Width(1)	t_{PW}	95	105	µs	100 µs typical
Data Valid Set-Up Time	t_{DV}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Overprogram Pulse Width(2)	t_{OPW}	2.85	78.75	ms	
Verify Set-up Time	t_{VFY}		100	ns	

Notes: (1) For Express algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} is a characteristics of the device but must be accomodated by the programmer
(2) V_{CC} = 6.0V ±0.25V, $V_{PP} = V_H$ = 12.5V ±0.50V for fast programming algorithm
V_{CC} = 6.5V ±0.25V, $V_{PP} = V_H$ = 13.0V ±0.25V for Express algorithm

PACKAGING

The 27HC191/27HC291 is available in a variety of packages:

—Cerdip DIP (27HC191 only)
—Plastic Leaded Chip carrier
—Plastic DIP (27HC191 only)
—Ceramic Leadless Chip Carrier
—Skinny Cerdip DIP (27HC291 only)
—Skinny Plastic DIP (27HC291 only)

FUNCTIONAL DESCRIPTION

The 27HC191/27HC291 has the following functional modes:

—Operation: The 27HC191/27HC291 can be activated for data read, be put in standby mode to lower its power consumptioin or have the outputs disabled.
—Programming: To receive its permanent data, the 27HC191/27HC291 must be programmed. Both a program and program/verify procedure is available. It can be programmed with Fast or Express algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

Operation Mode	CS3/ $\overline{PGM}$	CS2/ $\overline{VFY}$	$\overline{CS1}$/ VPP	A9	O0 - O7
Read	VIH	VIH	VIL	X	Data Out
Standby	X	X	VIH	X	High Z
Standby	X	VIL	X	X	High Z
Standby	VIL	X	X	X	High Z
Program	VIL	VIH	VH	X	Data In
Program Verify	VIH	VIL	VH	X	Data Out
Program Inhibit	VIH	VIH	VH	X	High Z
Identity	VIH	VIH	VIL	VH	Identity Code

X = Don't care

Operation

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table above.

Read Mode

For timing and AC characteristics refer to the table Read Waveforms and Read Operation AC characteristics.

The 27HC191/27HC291 memory data is accessed when:

—the chip is selected by setting the $\overline{CS_1}/V_{PP}$ pin low, $CS_2/\overline{VFY}$ high, and $CS_3/\overline{PGM}$ high.

For Read operation on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from the last CS to be brought active to output (t_{CS2}). A faster CS access time (t_{CS1}) is available on the standard part to provide the additional time for the decoding of the CS signals.

Standby Mode

The standby mode is entered when $\overline{CS_1}/V_{PP}$ is high or when $CS_2/\overline{VFY}$ is low or $CS_3/\overline{PGM}$ is low. When any one of the conditions is met, the supply current will drop from 65mA to 100μA on the low power part and to 35mA on the standard part.

Programming/Verification

The 27HC191/27HC291 has to be programmed, and afterward the programmed information verified. The Identity Code can be read to properly set up automatic equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithm

Two programming algorithms are available: fast programming and Express.

The fast programming algorithm is the industry standard programming mode that requires both an initial programming pulse and overprogramming pulses. A flowchart is shown in Figure 1.

The Express algorithm has been developed to improve programming throughput times in a production environment. Up to 10 pulses of 100 μsec each are applied until the byte is verified. No overprogramming is required.

A flow chart of the algorithm is shown in Figure 2.

The programming mode is entered when:

—V_{CC} is brought to the proper level
—$\overline{CS_1}/V_{PP}$ is brought to the proper V_H level
—$CS_2/\overline{VFY}$ is high
—$CS_3/\overline{PGM}$ is pulsed low

Since the erase state is "1" in the array, programming of a "0" is required. The address of the memory location to be programmed is set via pins A0-A10, and the data is presented to pins O0-O7. When data and address are stable, a low going pulse on the $CS_3/\overline{PGM}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

—V_{CC} is at the proper level
—$\overline{CS_1}/V_{PP}$ is at the proper V_H level
—$CS_2/\overline{VFY}$ pin is low
—$CS_3/\overline{PGM}$ pin is high

Inhibit Mode

When programming multiple devices in parallel with different data only $CS_3/\overline{PGM}$ need to be under separate control to each device. By pulsing the $CS_3/\overline{PGM}$ line low on a particular device, that device will be programmed and all other devices with $CS_3/\overline{PGM}$ held high will not be programmed with data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies ths manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5 to12.5 V). The $\overline{CS_1}\backslash V_{PP}$ pin must be at V_{IL} and $CS_2/\overline{VFY}$ and $CS_3/\overline{PGM}$ at V_{IH}. A0 is used to access the two non-erasable bytes whose data appears on O0-O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O 7	O 6	O 5	O 4	O 3	O 2	O 1	O 0	H e x
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type	V_{IH}	0	0	0	1	0	1	0	1	15

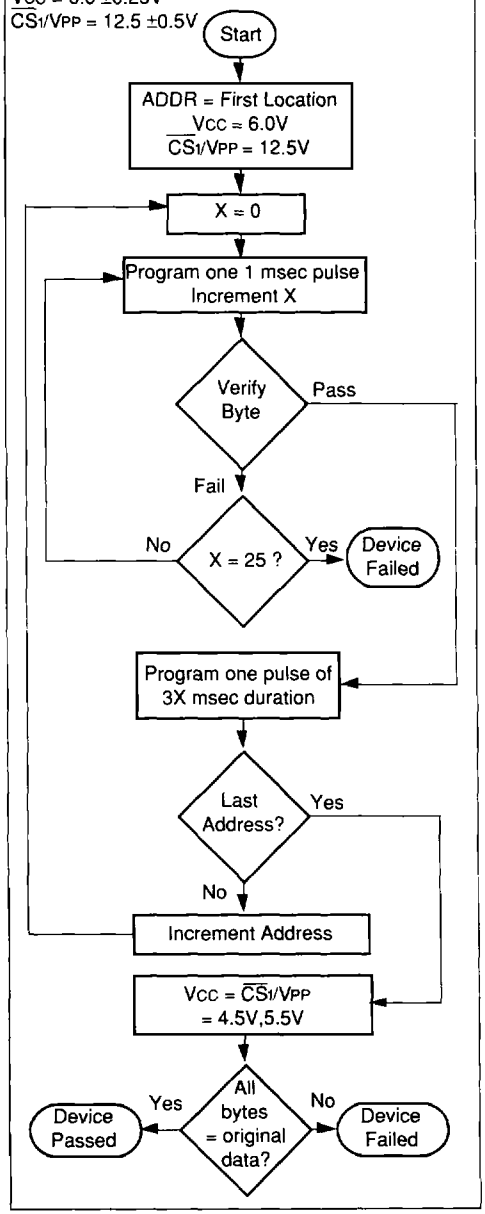
Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelenghts ≤4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial shortwave UV source emitting at 2537 Å with an intensity of 12000μW/cm² at 1". The erasure time at that distance is about 15 to 20 minutes.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

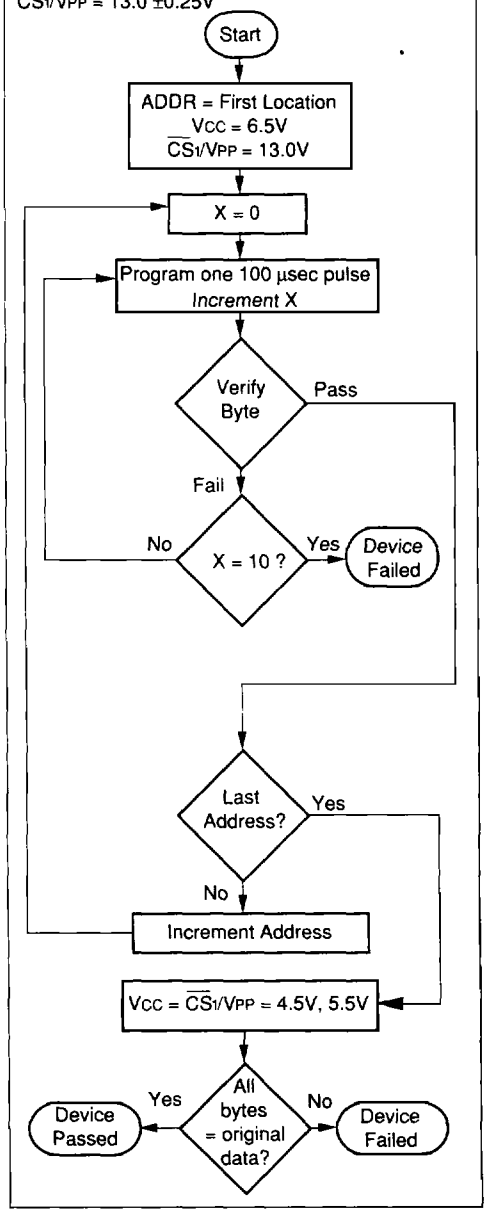
PROGRAMMING - Figure 1
Fast Algorithm

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.0 ±0.25V
$\overline{CS_1}/V_{PP}$ = 12.5 ±0.5V



PROGRAMMING - Figure 2
Express Algorithm

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
$\overline{CS_1}/V_{PP}$ = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC191 - 35 I / J

Package:	J	Cerdip DIP (27HC191 Only)
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier (OTP Available)
	P	Plastic DIP (27HC191 Only, OTP Available)
	SJ	SKINNY CERDIP (27HC291 Only)
	SP	SKINNY PLASTIC (27HC291 Only, OTP Available)
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
Access Time:	35	35 nsec
	40	40 nsec
	45	45 nsec
	55	55 nsec
Power Type:	Blank	Standard Power
	L	Low Power
Device:	27HC191	16K (2K x 8) High Speed EPROM
	27HC291	16K (2K x 8) High Speed EPROM

