HIGH-SPEED 2,048 x 8 CMOS DUAL-PORT RAM

FEATURES

- High speed:
  - 55, 70, and 90 ns access
- Fully static operation
- Full contention arbitration (VT7132)
- VT7142 slave for bus expansion
- Output enable function
- Separate port power-down
- Advanced CMOS technology
- Low power: 150 mA (max) operating
- 48-pin DIP or 52-pin PLCC

DESCRIPTION

The VT7132 and VT7142 are 16,384-bit dual-port static random access memories that are organized as 2,048 8-bit words. The VT7132 is designed to be used as a stand-alone "master" dual-port RAM with the VT7142 "slave" dual-port RAM in a system application larger than 8 bits. The master/slave approach in large bus systems requires no external contention logic.

The VT7132/VT7142 feature two separate I/O ports that each allow independent access to read or write to any location in the memory. The memory is designed to permit read and/or write operations to be performed at both ports at the same time. Contention arbitration logic is provided to eliminate overlapping operations to the same memory location.

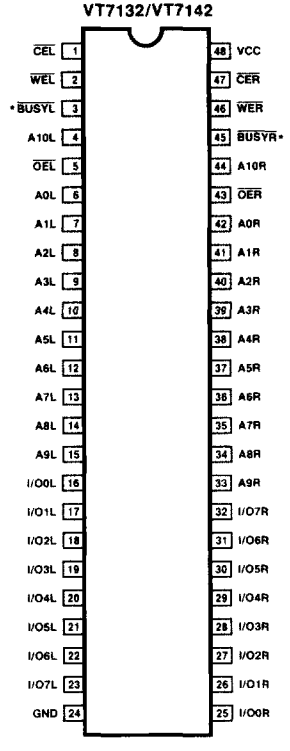
The on-chip contention logic arbitrates and delays one port until the other port's operation is completed. When this occurs, a Busy flag is sent to the side delayed. This flag stays set until the first operation is complete. When both sides request access at exactly the same time, the left port takes priority.

Automatic power down for each port is controlled independently by its Chip Enable input.

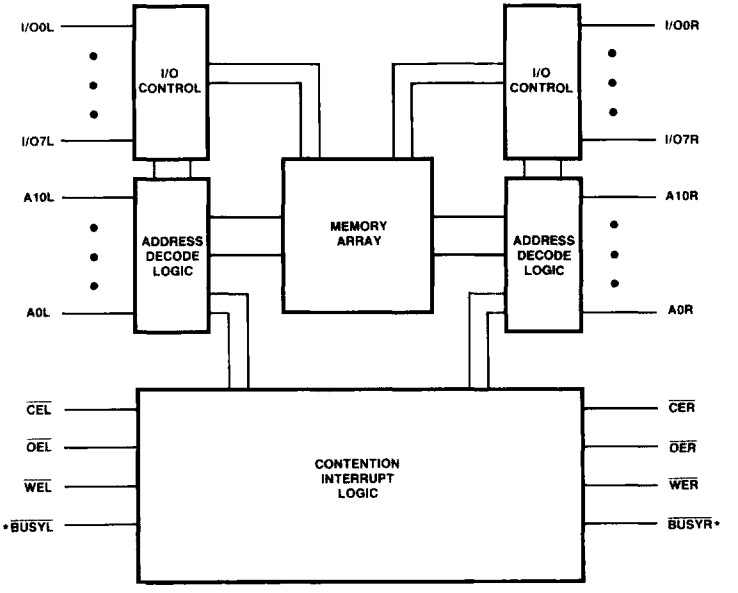
Interfacing to the VT7132/VT7142 is further simplified by the incorporation of an Output Enable control for each port.

PIN DIAGRAM

VT7132/VT7142



BLOCK DIAGRAM



* OPEN-DRAIN OUTPUTS FOR VT7132. INPUTS FOR VT7142.

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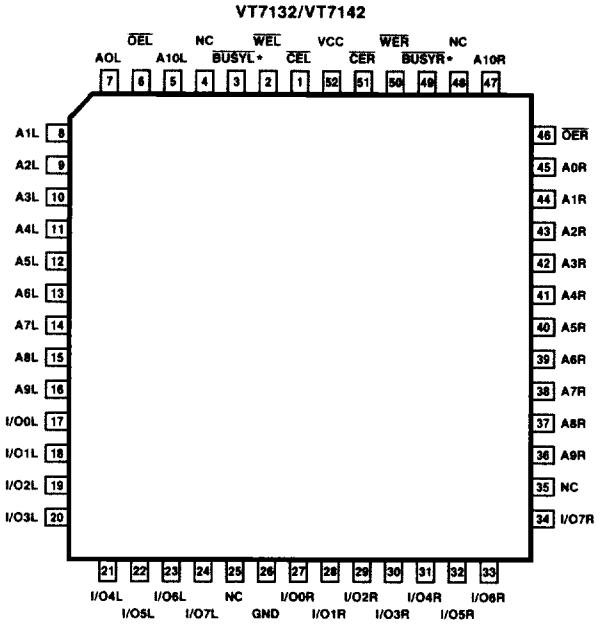
PIN DIAGRAM



*OPEN-DRAIN OUTPUTS FOR VT7132. INPUTS FOR VT7142.

FUNCTIONAL DESCRIPTION

The VT7132 and VT7142 are 16,384-bit dual-port RAMs that feature two separate I/O ports. Each allows independent access for reading or writing to any location in the memory.

PORT ENABLING

The VT7132/VT7142 feature separate left- and right-port chip enable controls ($\overline{CEL}$ and $\overline{CER}$) that activate their respective ports when they go LOW (see Table 1). When a port is active, it is allowed access to the entire memory array. When a chip enable signal is HIGH, its side of the device remains in a standby power mode as long as it does not change state.

Each port has an output enable control ($\overline{OEL}$ and $\overline{OER}$) that keeps its respective output in a high-impedance state when HIGH. When a port's $\overline{OE}$ is LOW and its write enable ($\overline{WE}$) input HIGH, its output bus drivers are turned on.

Separate write enable inputs ($\overline{WEL}$ and $\overline{WER}$) control writing of new data into any location in the RAM from either port. For example, when the left-port write enable ($\overline{WEL}$) is LOW, new data can be written into the location selected by the left-port address field. When a port's $\overline{WE}$ input is HIGH, data can be read from that port if its respective $\overline{OE}$ line is LOW. For example, when $\overline{WEL}$ is HIGH and $\overline{OEL}$ LOW, data can be read from the location selected by the left-port address field. Similarly, $\overline{WER}$ HIGH and $\overline{OER}$ LOW allows data to be read from the location selected by the right-port address field.

CONTENTION ARBITRATION

Contention for a memory location can occur when both the left and right ports are active and the addresses match.

On-chip control logic arbitration is used if the addresses at the ports match and both $\overline{CEL}$ and $\overline{CER}$ go LOW while $\overline{OEL}$ and $\overline{OER}$ are HIGH. In this case, priority is given to the port whose $\overline{CE}$ first becomes valid; the other port is not allowed access to the memory core until the first port's operation is completed. If $\overline{CEL}$ and $\overline{CER}$ become valid simultaneously, the arbitration logic gives priority to the left port.

If both $\overline{CE}$ inputs are valid while the $\overline{OE}$ controls are HIGH and an address change occurs that causes an address match, priority is given to the port whose address becomes valid first. If both addresses become valid at the same time and match, the left port is given priority.

BUSY FLAGS

Separate Busy flags ($\overline{BUSYL}$ and $\overline{BUSYR}$) are provided to signal when a port's access to the memory core has been delayed. This permits the user to stop the processor connected to the losing port and add wait states, if desired.

When both ports try to access the same memory location, the on-chip arbitration logic causes the Busy flag to go LOW on the side that is delayed. This occurs rapidly enough that, if the user wishes, the processor's address and data can be preserved.

MASTER/SLAVE OPERATION

Expanding the data bus width beyond 8 bits in a dual-port RAM system implies that more than one memory chip will be active at the same time. Because of system timing and skews, this could result in $\overline{BUSYL}$ being active on one device while $\overline{BUSYR}$ is active on another. To avoid this lock-out condition, the VT7132/VT7142 master/slave approach allows arbitration to be performed by only one of the memory devices.

In such a system, one VT7132 master would be used in conjunction with one or more VT7142 slaves, which would be configured to fill the additional bus width. The $\overline{BUSY}$ inputs of the VT7142 interface with the $\overline{BUSY}$ outputs of the VT7132 without the need for external components, maintaining system performance.

When expanding the width of dual-port RAMs, writing to the slave RAMs must be delayed until after the $\overline{BUSY}$ input has settled. If this is not done,the slave chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time beyond $\overline{BUSY}$ to ensure that a write cycle occurs after the contention is resolved. The write pulse to the slave should be delayed by the maximum arbitration time of the master so that, if contention occurs, the write to the slave will be inhibited by the $\overline{BUSY}$ signal from the master.

TABLE 1. READ/WRITE CONTROL FUNCTIONS

Left Port Signals					Right Port Signals					
$\overline{CEL}$	$\overline{OEL}$	$\overline{WEL}$	$\overline{BUSYL}$	A0L–A9L	$\overline{CER}$	$\overline{OER}$	$\overline{WER}$	$\overline{BUSYR}$	A0R–A9R	Function
H	X	X	H	X	X	X	X	H	X	Left Port Power-Down
X	X	X	H	X	H	X	X	H	X	Right Port Power-Down
L	L	H	H	X	X	X	X	X	X	Read Left Port
L	X	L	H	X	X	X	X	X	≠	Write Left Port
X	X	X	X	≠	L	L	H	H	X	Read Right Port
X	X	X	X	≠	L	X	L	H	≠	Write Right Port
L	X	X	L	=	L	X	X	H	Note 1	Left Port Busy, Right Port Active
L	X	X	H	Note 1	L	X	X	L	=	Right Port Busy, Left Port Active

Note:
1. Each address pin active before equivalent pin on other port.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
Applied Output Voltage	−0.5 V to +7.0 V
Applied Input Voltage	−0.5 V to +7.0 V
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of this device under these or any conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Limits Min	Typ	Max	Unit	Conditions
IIL	Input Leakage			10	µA	VCC = 5.5 V, VIN = 0 V to VCC
IOL	Output Leakage			10	µA	VCC = 5.5 V, $\overline{CE}$ = VIH, VOUT = 0 V to VCC
ICC1	Active Current, (Both Ports Active)			150	mA	VCC = 5.5 V, $\overline{CE}$ = VIL, Outputs Open
ICC2	Standby Current, (Both Ports Standby)			10	mA	$\overline{CEL}$ = $\overline{CER}$ = VIH
ICC3	Standby Current, (One Port Standby)			70	mA	$\overline{CEL}$ or $\overline{CER}$ = VIH, Active Port Outputs Open
ICC4	Standby Current, (Both Ports – All CMOS Level Inputs)			1	mA	$\overline{CEL}$ = $\overline{CER}$ = $\overline{OEL}$ = $\overline{OER}$ = VIH VIN ≥ VCC −0.2 V or VIN ≤ 0.2 V
VIL	Input LOW Voltage	−0.5		0.8	V	
VIH	Input HIGH Voltage	2.2		VCC +1	V	Note 1
VOL1	Output LOW Voltage			0.4	V	IOL = 6 mA
				0.5	V	IOL = 8 mA
VOL2	Output LOW Voltage, Open-Drain Outputs			0.5	V	IOL = 16 mA
VOH	Output HIGH Voltage	2.4			V	IOH = −4.0 mA

DATA RETENTION DC CHARACTERISTICS

Symbol	Parameter	Limits Min	Typ	Max	Unit	Conditions
VDR	Data Retention VCC	2.0			V	Note 4
ICCDR	Data Retention Current			1	mA	Note 2

CAPACITANCE $T_A = 25°C$, $f = 1$ MHz, Note 3

Symbol	Parameter	Typ	Max	Unit	Conditions
COUT	Output Capacitance		10	pF	VOUT = 0 V
CIN	Input Capacitance		10	pF	VIN = 0 V

Notes:
1. All inputs are diode clamped to VCC.
2. VCC = 2.0 V, $\overline{CE}$ ≥ VCC −0.2 V, VIN ≥ VCC −0.2 V or VIN ≤ 0.2 V
3. This parameter is guaranteed but not tested.
4. $\overline{CE}$ ≥ VCC −0.2 V, VIN ≥ VCC −0.2 V or VIN ≤ 0.2 V

AC TEST CONDITIONS

Input Voltage Levels	0 V to +3 V
Input Rise and Fall Times	5 ns
Input Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	Figures 1, 2, and 3

AC TESTING LOAD CIRCUITS

FIGURE 1. OUTPUT LOAD CIRCUIT A

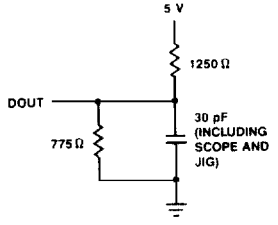


FIGURE 2. OUTPUT LOAD CIRCUIT B, Note 1

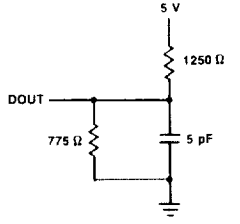
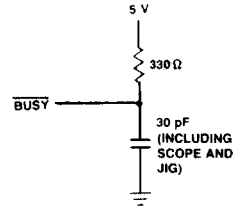
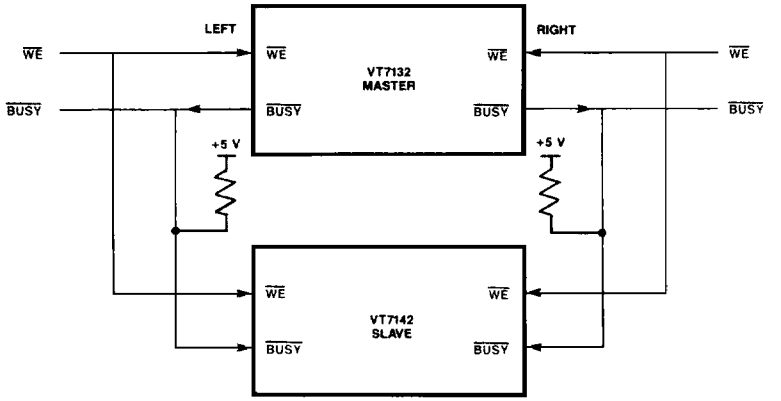


FIGURE 3. $\overline{\text{BUSY}}$ OUTPUT LOAD CIRCUIT (VT7132)



MASTER SLAVE EXPANSION TO 16-BIT MEMORY SYSTEM



Note:
1. For tHZ, tLZ, tWZ, and tOW.

TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%

Symbol	Parameter	VT7132-55		VT7132-70		VT7132-90		Units	Conditions
		Min	Max	Min	Max	Min	Max		
READ CYCLE, Note 1									
tRC	Read Cycle Time	55		70		90		ns	
tAA	Address Access Time		55		70		90	ns	
tACE	Chip Enable Access Time		55		70		90	ns	
tAOE	Output Enable Access Time		35		40		40	ns	
tOH	Output Hold from Address Change	0		0		10		ns	
tLZ	Output Low Z Time	0		0		0		ns	Notes 2, 3
tHZ	Output High Z Time	0	30	0	35	0	40	ns	Notes 2, 3
tPU	Chip Enable to Power-Up Time	0		0		0		ns	Note 2
tPD	Chip Disable to Power-Down Time		50		50		50	ns	Note 2
WRITE CYCLE									
tWC	Write Cycle Time	55		70		90		ns	Note 4
tEW	Chip Enable to End of Write	40		50		85		ns	
tAW	Address Valid to End of Write	40		50		85		ns	
tAS	Address Set-Up Time	0		0		0		ns	
tWP	Write Pulse Width	40		50		55		ns	
tWR	Write Recovery Time	0		0		0		ns	
tDW	Data Valid to End of Write	20		30		40		ns	
tDH	Data Hold Time	0		0		0		ns	
tWZ	Write Enable to Output High Z	0	30	0	35		40	ns	Notes 2, 3
tHZ	Output High Z Time	0	30	0	35	0	40	ns	Notes 2, 3
tOW	Output Active from End of Write	0		0		0		ns	Notes 2, 3

Notes:
1. $\overline{WE}$ is HIGH for read cycles.
2. This parameter is guaranteed but not tested.
3. Transition is measured ±500 mV from LOW or HIGH impedance voltage with load (Figures 1, 2, 3).
4. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP.

TIMING CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	VT7132-55		VT7132-70		VT7132-90		Units	Conditions
		Min	Max	Min	Max	Min	Max		
CONTENTION CYCLE									
tRC	Read Cycle Time	55		70		90		ns	
tWC	Write Cycle Time	55		70		90		ns	Note 9
tWB	Write to $\overline{BUSY}$	−10		−10		−10		ns	Notes 1, 2
tWH	Write Hold after $\overline{BUSY}$	20		20		20		ns	Note 5
tBAA	$\overline{BUSY}$ Access Time to Address		45		45		45	ns	
tBDA	$\overline{BUSY}$ Disable Time to Address		40		40		45	ns	
tBAC	$\overline{BUSY}$ Access Time to Chip Enable		35		35		45	ns	
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable		30		30		45	ns	
tWDD	Write Pulse to Data Delay		80		90		100	ns	Note 3
tDDD	Write Data Valid to Read Data Delay		55		70		90	ns	Note 3
tBDD	$\overline{BUSY}$ Disable to Valid Data		Note 4		Note 4		Note 4		Note 4
tAPS	Arbitration Priority Set-Up Time	5		5		5		ns	
tWP	Write Pulse Width	40		50		55			
DATA RETENTION TIMING									
tR	Operation Recovery Time	tRC		tRC		tRC		ns	Notes 6, 7, 8
tCDR	Chip Deselect to Data Retention Time	0		0		0		ns	Notes 7, 8

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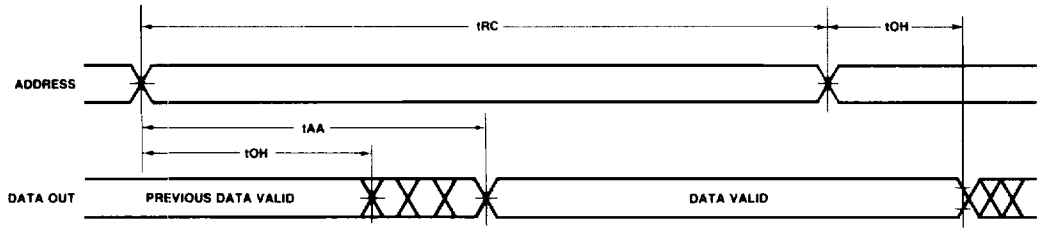
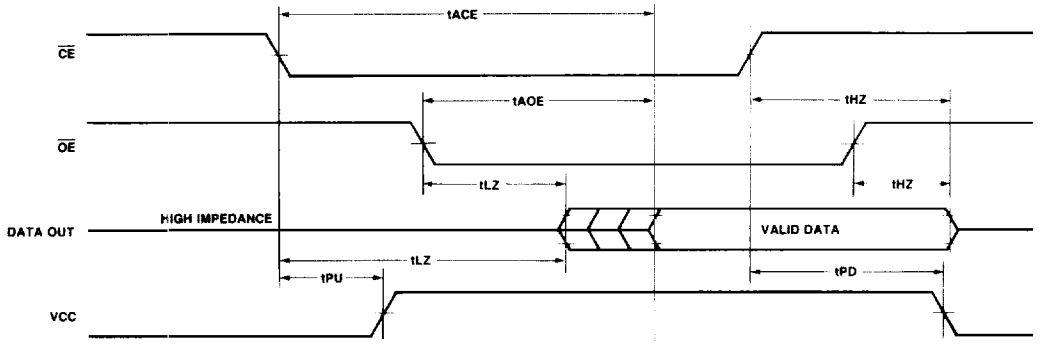
Notes:
1. For Slave (VT7142) only.
2. To ensure that the write cycle is inhibited during contention.
3. Port to port delay through RAM cells from writing port to reading port.
4. tBDD is a calculated parameter and is the greater of 0, tWDD–tWP (actual) or tDDD–tDW (actual).
5. Ensures that a write cycle is completed after contention.
6. tRC = Read Cycle Time.
7. This parameter is guaranteed but not tested.
8. $V_{CC} = 2.0\ V$, $\overline{CE} \geq V_{CC} - 0.2\ V$, $V_{IN} \geq V_{CC} - 0.2\ V$ or $V_{IN} \leq 0.2\ V$
9. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP.

TIMING DIAGRAMS

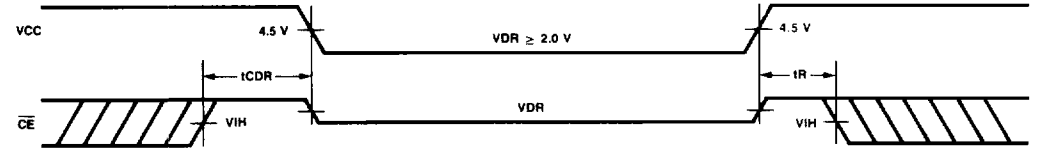
READ CYCLE NO. 1, EITHER SIDE, Notes 1, 2, and 4



READ CYCLE NO. 2, EITHER SIDE, Notes 1 and 3



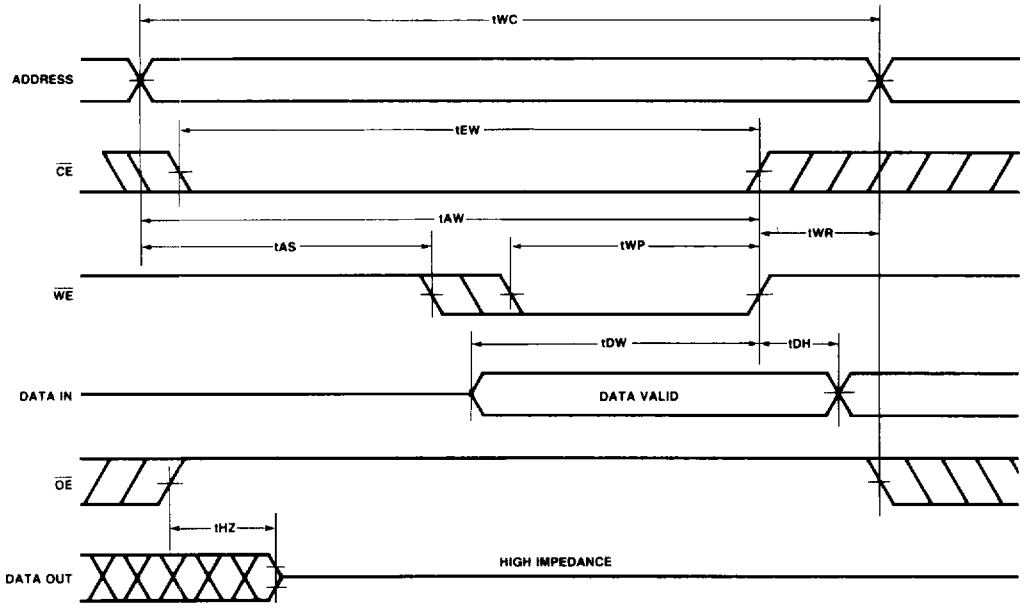
DATA RETENTION MODE



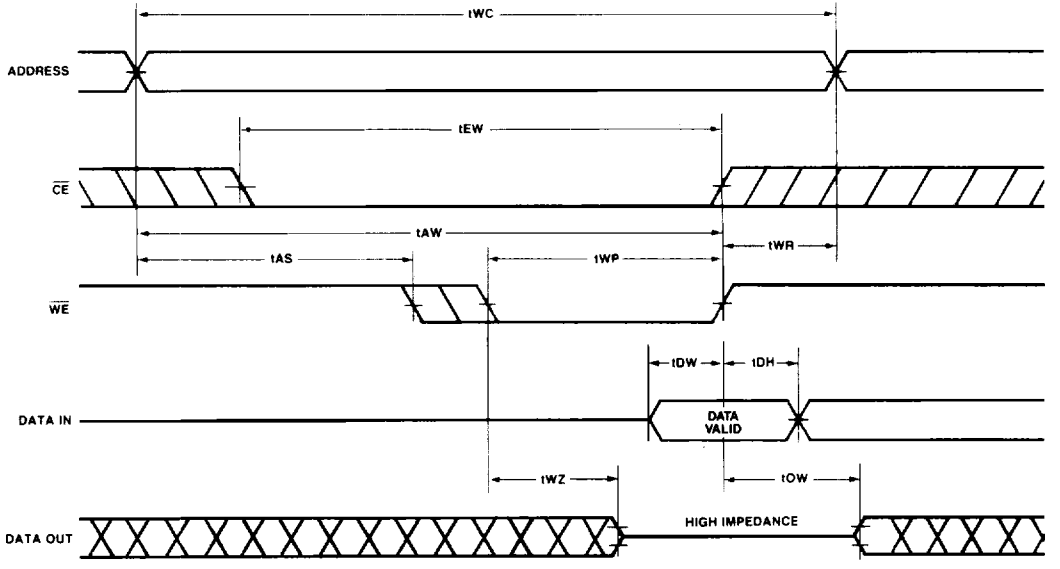
Notes:
1. $\overline{WE}$ is HIGH for read cycles.
2. Device is continuously enabled ($\overline{CE}$ = VIL).
3. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
4. $\overline{OE}$ = VIL.

TIMING DIAGRAMS

WRITE CYCLE NO. 1, EITHER SIDE, Note 1



WRITE CYCLE NO. 2, EITHER SIDE, ($\overline{OE}$ = VIL), Note 1



Note:
1. If $\overline{CE}$ goes HIGH at the same time $\overline{WE}$ goes HIGH, the outputs remain in a high-impedance state.

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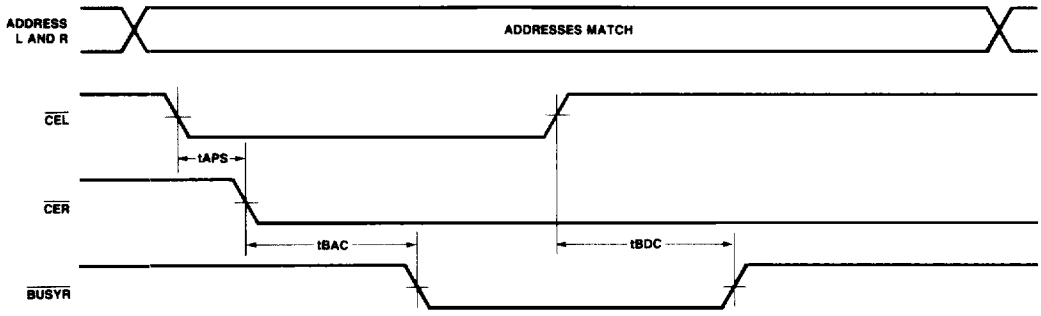
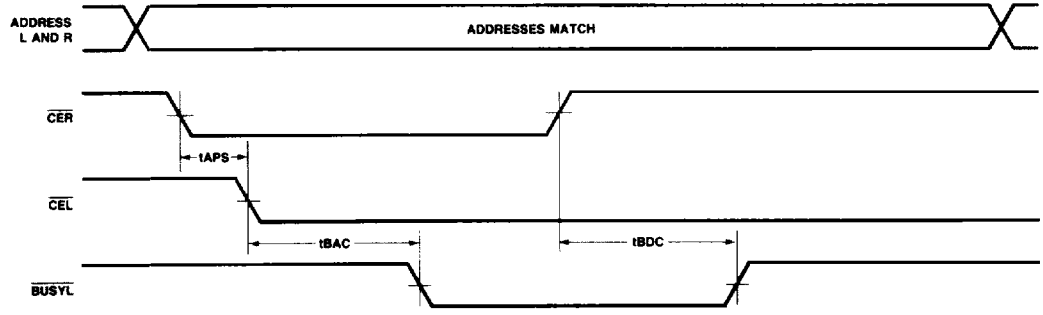
TIMING DIAGRAMS

CONTENTION CYCLE NO. 1, $\overline{CE}$ CONTENTION ARBITRATION MODE, Note 1

$\overline{CEL}$ VALID FIRST



$\overline{CER}$ VALID FIRST

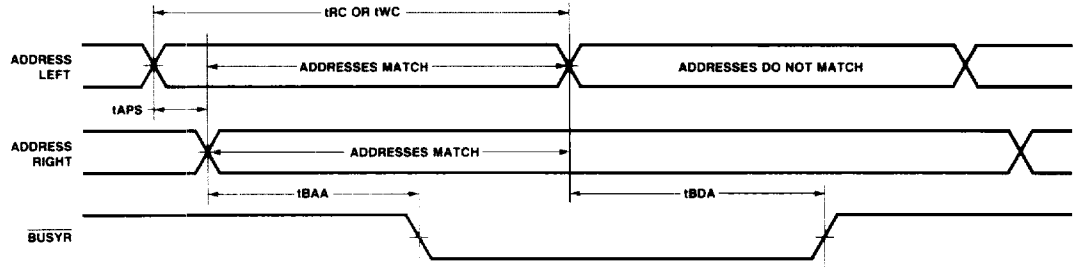


Note:
1. $\overline{OE}$ = VIH when contention occurs.

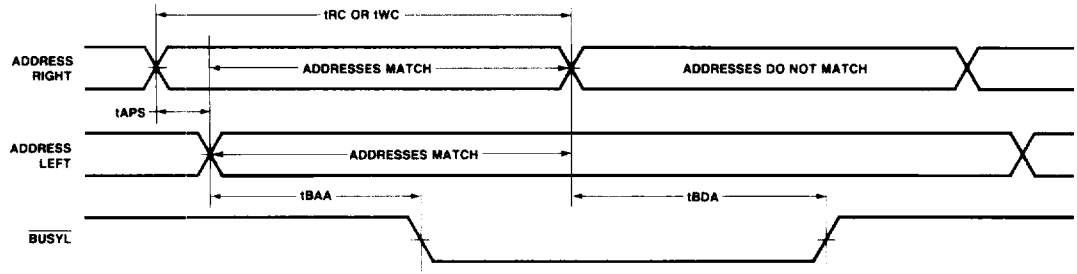
TIMING DIAGRAMS (Cont.)

CONTENTION CYCLE NO. 2, ADDRESS CONTENTION ARBITRATION MODE, Notes 1 and 2

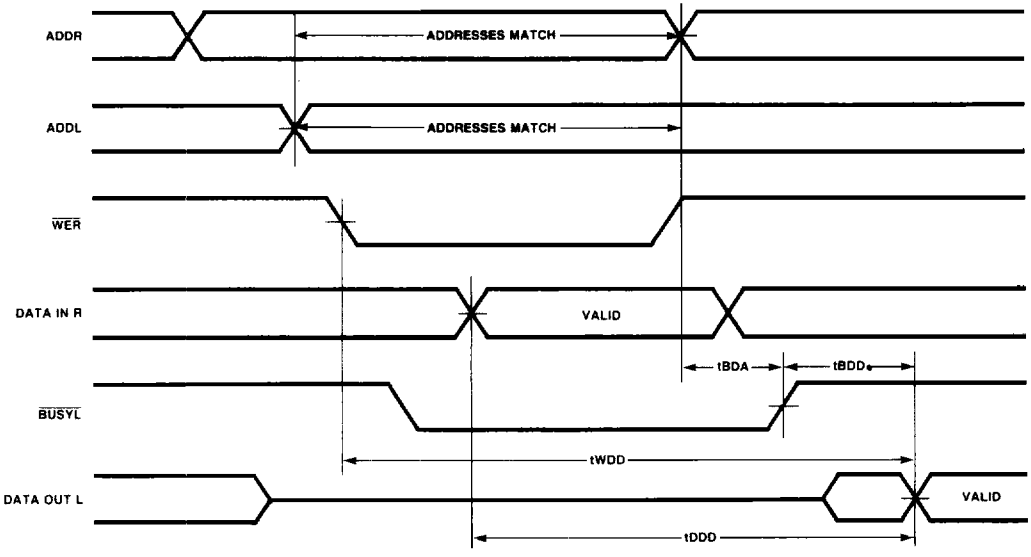
ADDRESS LEFT VALID FIRST



ADDRESS RIGHT VALID FIRST



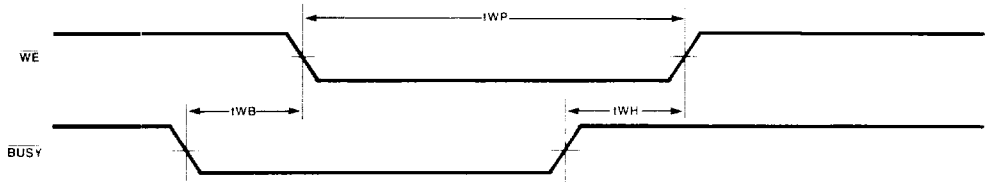
READ WITH $\overline{BUSY}$



Notes:
1. $\overline{OE}$ = VIH when contention occurs.
2. $\overline{CEL}$ = $\overline{CER}$ = VIL.

TIMING DIAGRAMS (Cont.)

WRITE WITH $\overline{BUSY}$ SLAVE ONLY (7142)



POWER DISTRIBUTION AND TRACE LINE TERMINATION CONSIDERATIONS

To achieve full compatibility with TTL-based devices, CMOS memories are typically designed to convert TTL input levels to the CMOS levels required for internal operation. Greater power efficiency is achieved, however, when an entire design takes advantage of the lower consumption capabilities of CMOS technology. When CMOS levels are used throughout a design and not only in the memory, lower current specifications can be achieved, resulting in a lower overall power requirement.

The operating margins of all devices on a board using very-high-speed memory can best be maintained by providing a quiet environment that is free of noise spikes, undershoot, and excessive ringing. Key elements in creating such an atmosphere are observing proper power distribution techniques and proper termination of TTL drive lines.

POWER DISTRIBUTION

A power distribution scheme that effectively maintains wide operating margins combines power trace layout with decoupling capacitor placement to minimize the series impedance in the decoupling path. This path runs from the power pin of a memory device through its decoupling capacitor to the ground pin.

The total impedance of this path is established by the power line impedance and the impedance of the capacitor itself. In practice, the capacitive effects of the decoupling path are minimal because of the very-high-frequency components of the current transients associated with memory operation. This makes the line inductance the dominant impedance factor.

The preferred technique for reducing power line impedance and improving the quality of VCC and ground is to use separate power and ground planes.

A somewhat-less-effective approach is to grid the power and ground traces. If this is done, the ground grid should extend to the TTL driver peripheral circuitry, providing a solid ground reference for the TTL drivers.

The decoupling capacitor, which provides energy for the high-frequency transients, should be placed as near the memory device as possible in order to have the shortest practical lead lengths. This capacitor should be of a low inductance type and, at a minimum, be 0.1 μF. For the greatest efficiency, it should be placed between the power supply and ground pins of each device.

Low-frequency current transients can be handled by larger tantalum capacitors placed near the memory board edge connector, where the power traces meet the backplane power distribution system. Such large capacitors provide bulk energy storage that prevents voltage drops caused by the long inductive path between the memory board and the power supply.

TRACE TERMINATION

On a memory board, trace lines have the appearance of shorted transmission lines to TTL-level driver signals. This can cause reflections of TTL signals propagating down the lines, particularly LOW-going signals. These reflections can be reduced or eliminated by proper line termination. Proper termination also reduces RFI emissions.

Trace line termination can be either series or parallel, although series termination is recommended. This type of termination has the advantage of drawing no dc current, and also requires the smallest number of components to implement. It simply calls for placing a series resistor in the signal line to dampen reflections. The resistor is placed at the output of the TTL driver, as close as possible to the driver package. The driver/termination combination should be placed close to the memory array to minimize lead length.

In most applications, a series resistor of between 10 ohms and 33 ohms is sufficient to dampen reflections. However, because the characteristic impedance of each layout is different, some experimentation may be necessary to determine the optimum value for a specific configuration.

SIGNAL FIDELITY

When the layout is complete and the power distribution and line termination requirements have been met, it is good procedure to verify signal fidelity by observation with a wide-band (300 MHz or faster) oscilloscope and probe.