NT2GT72U4NB0BV / NT2GT72U4NB1BV
NT512T72U89B0BV / NT1GT72U4PB0BV

512MB: 64M x 72 / 1GB: 128M X 72 / 2GB: 256M X 72

Registered DDR2 SDRAM DIMM

240pin Registered DDR2 SDRAM MODULE Based on 64Mx8 & 128Mx4 DDR2 SDRAM Die B

Features

- 64Mx72 Registered DDR2 DIMM based on 64Mx8 DDR2 SDRAM (NT5TU64M8BE)
- 128Mx72 & 256Mx72 Registered DDR2 DIMM based on 128Mx4 DDR2 SDRAM (NT5TU128M4BE)
- JEDEC Standard 240-pin Dual In-Line Memory Module
- Error Check Correction (ECC) Support
- Registered inputs with one-clock delay
- Performance:

		PC2-5300	PC2-6400	PC2-6400	
	Speed Sort	-3C	-25D	-25C	Unit
	DIMM $\overline{CAS}$ Latency[*]	5	6	5	
f CK	Clock Frequency	333	400	400	MHz
t CK	Clock Cycle	3	2.5	2.5	ns
f DQ	DQ Burst Frequency	667	800	800	MHz

- Intended for 333 and 400 MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = 1.8 \pm 0.1$ Volt, $V_{DDQ} = 1.8 \pm 0.1$ Volt
- SDRAMs have 4 internal banks for concurrent operation

- Differential clock inputs
- Data is read or written on both clock edges
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 5, 6
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- On-Die Termination (ODT)
- Off-Chip Driver (OCD)
- 14/10/1 Addressing (row/column/rank) – 512MB
- 14/11/1 Addressing (row/column/rank) – 1GB
- 14/11/2 Addressing (row/column/rank) – 2GB
- Serial Presence Detect
- Gold contacts
- SDRAMs in 60-ball FBGA Package
- RoHS compliance

Description

NT512T72U89B0BV, NT1GT72U4PB0BV, NT2GT72U4NB0BV and NT2GT72U4NB1BV are Registered 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a one-bank 64Mx72 or128Mx72 and two-banks 256Mx72 high-speed memory array. The module uses nine 64Mx8 (NT512T72U89B0BV), eighteen 128Mx4 (NT1GT72U4PB0BV) or thirty-six 128Mx4 (NT2GT72U4NB0BV, NT2GT72U4NB1BV) DDR2 SDRAMs in FBGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 333 MHz (400MHz) clock speeds and achieves high-speed data transfer rates of up to 667 MHz (800MHz). Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

NT2GT72U4NB0BV / NT2GT72U4NB1BV
NT512T72U89B0BV / NT1GT72U4PB0BV

512MB: 64M x 72 / 1GB: 128M X 72 / 2GB: 256M X 72

Registered DDR2 SDRAM DIMM

Ordering Information

Part Number	Speed			Organization	Leads	Power
NT512T72U89B0BV-3C	333 MHz (3ns @ CL = 5)	DDR2-667	PC2-5300	64Mx72		
NT1GT72U4PB0BV-3C				128Mx72		
NT2GT72U4NB0BV-3C				256Mx72		
NT512T72U89B0BV-25D	400 MHz (2.5ns @ CL = 6)	DDR2800	PC2-6400	64Mx72	Gold	1.8V
NT1GT72U4PB0BV-25D				128Mx72		
NT2GT72U4NB1BV-25D				256Mx72		
NT512T72U89B0BV-25C	400 MHz (2.5ns @ CL = 5)			64Mx72		
NT1GT72U4PB0BV-25C				128Mx72		
NT2GT72U4NB1BV-25C				256Mx72		

Pin Description

CK0, $\overline{CK0}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	CB0-CB7	ECC Check Bit Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQS0-DQS8	Bidirectional data strobes
$\overline{CAS}$	Column Address Strobe	DM0-DM8/DQS9-17	Input Data Mask/High Data Strobes
$\overline{WE}$	Write Enable	$\overline{DQS0}$-$\overline{DQS17}$	Differential data strobes
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	VDD	Core Power
A0-A9, A11-A13	Address Inputs	VDDQ	I/O Power
A10/AP	Column Address Input/Auto-precharge	VREF	Ref. Voltage for SSTL_18 inputs
BA0, BA1	SDRAM Bank Address Inputs	VDDSPD	Serial EEPROM positive power supply
$\overline{RESET}$	Reset pin	VSS	Ground
ODT0, ODT1	Active termination control lines	SCL	Serial Presence Detect Clock Input
NC	No Connect	SDA	Serial Presence Detect Data input/output
RFU	Reserved for Future Use	SA0-2	Serial Presence Detect Address Inputs
Par_In	Parity bit for the Address and Control bus	$\overline{Err\_Out}$	Parity error found on the Address and Control bus

NT2GT72U4NB0BV / NT2GT72U4NB1BV
NT512T72U89B0BV / NT1GT72U4PB0BV

512MB: 64M x 72 / 1GB: 128M X 72 / 2GB: 256M X 72

Registered DDR2 SDRAM DIMM

Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	42	CB0	82	Vss	121	Vss	162	CB5	202	DM4/DQS13
2	Vss	43	CB1	83	$\overline{DQS4}$	122	DQ4	163	Vss	203	NC, $\overline{DQS13}$
3	DQ0	44	Vss	84	DQS4	123	DQ5	164	DM8/DQS17	204	Vss
4	DQ1	45	$\overline{DQS8}$	85	Vss	124	Vss	165	$\overline{DQS17}$	205	DQ38
5	Vss	46	DQS8	86	DQ34	125	DM0, DQS9	166	Vss	206	DQ39
6	$\overline{DQS0}$	47	Vss	87	DQ35	126	$\overline{DQS9}$	167	CB6	207	Vss
7	DQS0	48	CB2	88	Vss	127	Vss	168	CB7	208	DQ44
8	Vss	49	CB3	89	DQ40	128	DQ6	169	Vss	209	DQ45
9	DQ2	50	Vss	90	DQ41	129	DQ7	170	VDDQ	210	Vss
10	DQ3	51	VDDQ	91	Vss	130	Vss	171	NC, CKE1	211	DM5/DQS14
11	Vss	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	VDD	212	$\overline{DQS14}$
12	DQ8	53	VDD	93	DQS5	132	DQ13	173	NC	213	Vss
13	DQ9	54	NC	94	Vss	133	Vss	174	NC	214	DQ46
14	Vss	55	$\overline{Err\_Out}$	95	DQ42	134	DM1/DQS10	175	VDDQ	215	DQ47
15	$\overline{DQS1}$	56	VDDQ	96	DQ43	135	$\overline{DQS10}$	176	A12	216	Vss
16	DQS1	57	A11	97	Vss	136	Vss	177	A9	217	DQ52
17	Vss	58	A7	98	DQ48	137	RFU	178	VDD	218	DQ53
18	$\overline{RESET}$	59	VDD	99	DQ49	138	RFU	179	A8	219	Vss
19	NC	60	A5	100	Vss	139	Vss	180	A6	220	NC
20	Vss	61	A4	101	SA2	140	DQ14	181	VDDQ	221	NC
21	DQ10	62	VDDQ	102	NC	141	DQ15	182	A3	222	Vss
22	DQ11	63	A2	103	Vss	142	Vss	183	A1	223	DM6/DQS15
23	Vss	64	VDD	104	$\overline{DQS6}$	143	DQ20	184	VDD	224	$\overline{DQS15}$
24	DQ16		KEY	105	DQS6	144	DQ21		KEY	225	Vss
25	DQ17	65	Vss	106	Vss	145	Vss	185	CK0	226	DQ54
26	Vss	66	Vss	107	DQ50	146	DM2/DQS11	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	VDD	108	DQ51	147	$\overline{DQS11}$	187	VDD	228	Vss
28	DQS2	68	Par_In	109	Vss	148	Vss	188	A0	229	DQ60
29	Vss	69	VDD	110	DQ56	149	DQ22	189	VDD	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	Vss
31	DQ19	71	BA0	112	Vss	151	Vss	191	VDDQ	232	DM7/DQS16
32	Vss	72	VDDQ	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	$\overline{DQS16}$
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{CS0}$	234	Vss
34	DQ25	74	$\overline{CAS}$	115	Vss	154	Vss	194	VDDQ	235	DQ62
35	Vss	75	VDDQ	116	DQ58	155	DM3/DQS12	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	$\overline{CS1}$	117	DQ59	156	$\overline{DQS12}$	196	A13	237	Vss
37	DQS3	77	ODT1	118	Vss	157	Vss	197	VDD	238	VDDSPD
38	Vss	78	VDDQ	119	SDA	158	DQ30	198	Vss	239	SA0
39	DQ26	79	Vss	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	Vss	200	DQ37		
41	Vss	81	DQ33			161	CB4	201	Vss		

$\overline{Err\_Out}$ and Par_In are optional functions to check address and command parity.

Input/Output Functional Description

| Symbol	Type	Polarity	Function
CK0	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-18 inputs
VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11-A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63 CB0 – CB7	(SSTL)	Active High	Data and Check Bit Input/Output pins. Check bits are only applicable on the x72 DIMM configurations.
VDD, VSS	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0 – DQS17 $\overline{DQS0}$ – $\overline{DQS17}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
$\overline{RESET}$	Input	Active Low	The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and the registers will be set to low level. The PLL will remain synchronized with the input clock.
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V DD to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V DD to act as a pull-up.
V DDSPD	Supply		Serial EEPROM positive power supply.
Par_In	Input		Parity bit for the Address and Control bus. (1 for Odd, 0 for Even)
$\overline{Err\_Out}$	Out		Parity error found in the Address and Control bus.

NT2GT72U4NB0BV / NT2GT72U4NB1BV
NT512T72U89B0BV / NT1GT72U4PB0BV

512MB: 64M x 72 / 1GB: 128M X 72 / 2GB: 256M X 72

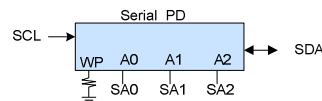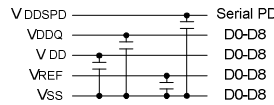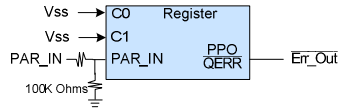**Registered DDR2 SDRAM DIMM**

Functional Block Diagram (512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)
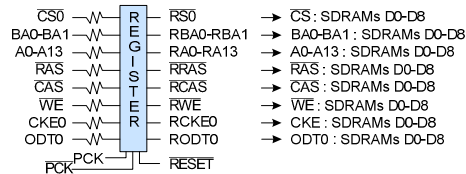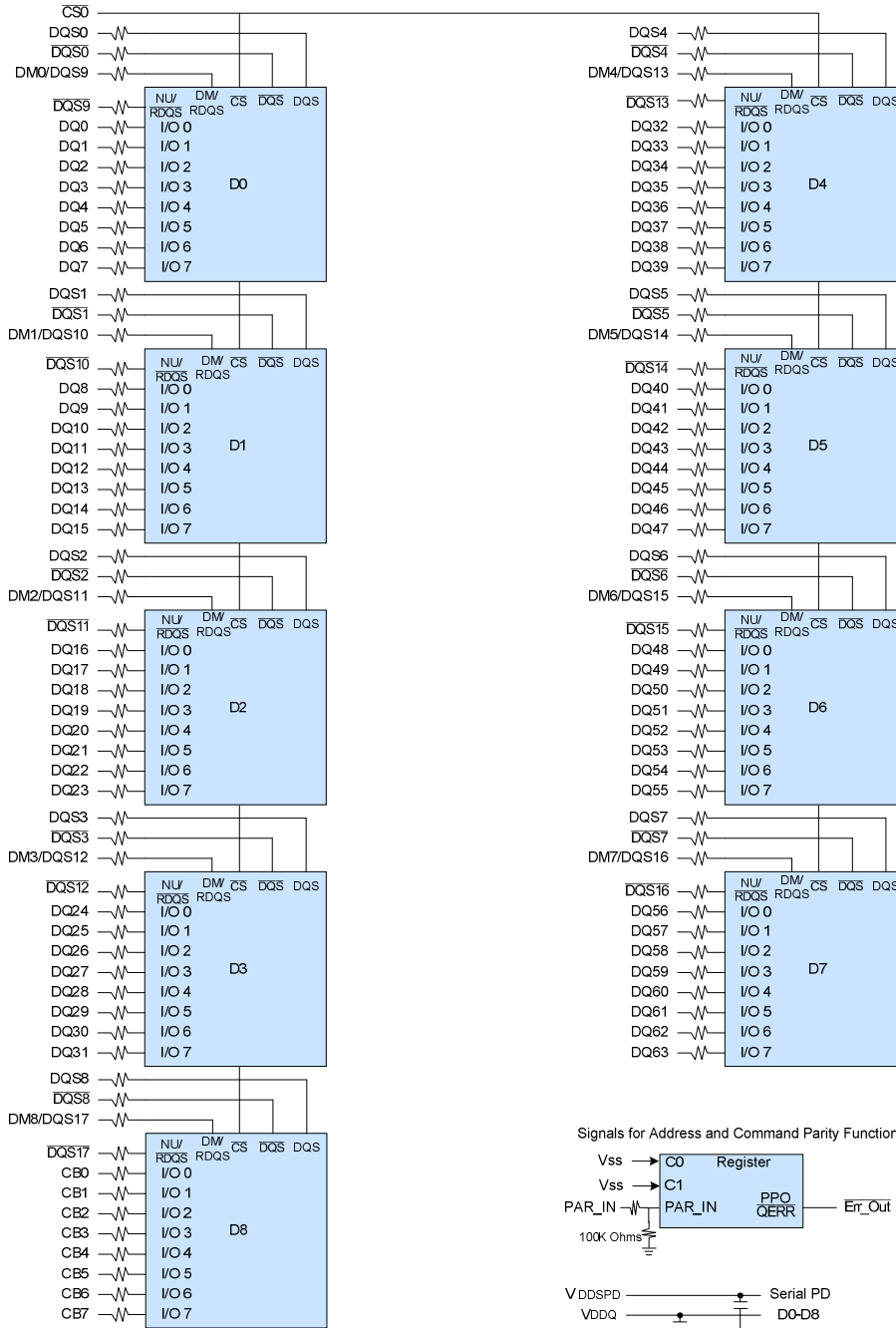
Notes :   1. DQ-to-I/O wiring may be changed within a byte.
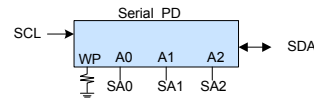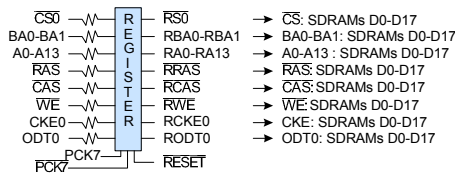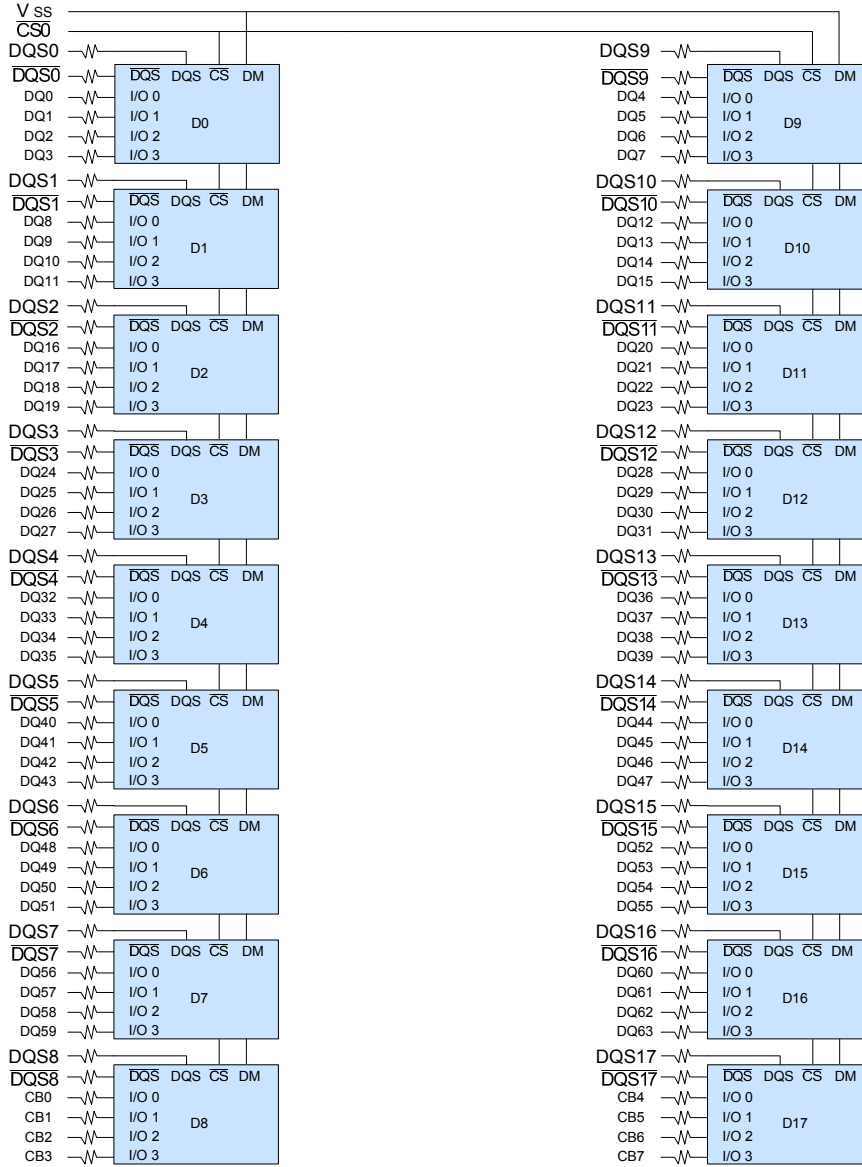   2. Resistor values without noted are 22 Ohms +/- 5%

NT2GT72U4NB0BV / NT2GT72U4NB1BV
NT512T72U89B0BV / NT1GT72U4PB0BV

512MB: 64M x 72 / 1GB: 128M X 72 / 2GB: 256M X 72

Registered DDR2 SDRAM DIMM

Functional Block Diagram (1GB, 1 Rank, 128Mx4 DDR2 SDRAMs)

Functional Block Diagram (2GB DDR2-533/667, 2 Ranks, 128Mx4 DDR2 SDRAMs)

Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. Resistor values without noted are 22 Ohms +/- 5%
3. RS0 and RS1 alternate between the bottom and surface side of DIMM.

Signals for Address and Command Parity Function

Functional Block Diagram (2GB DDR2-800, 2 Ranks, 128Mx4 DDR2 SDRAMs)
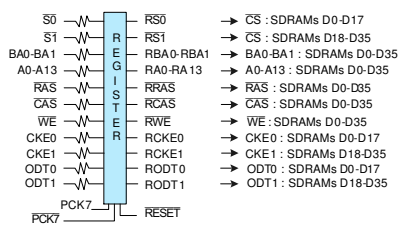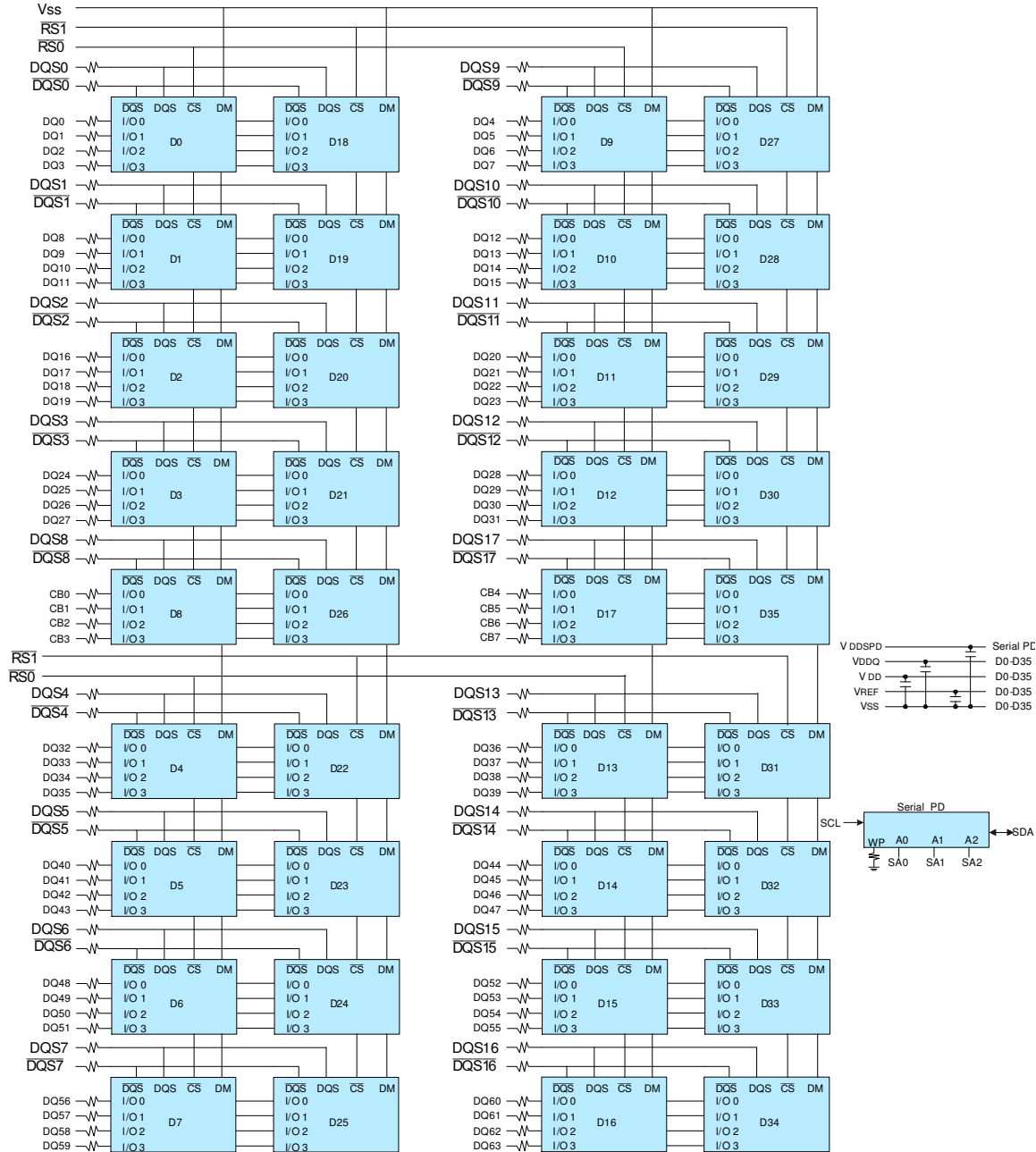
Notes : 1. DQ-to-I/O wiring may be changed within a byte.
2. Resistor values without noted are 22 Ohms +/- 5%.
3. RS0 and RS1 alternate between the bottom and surface side of DIMM
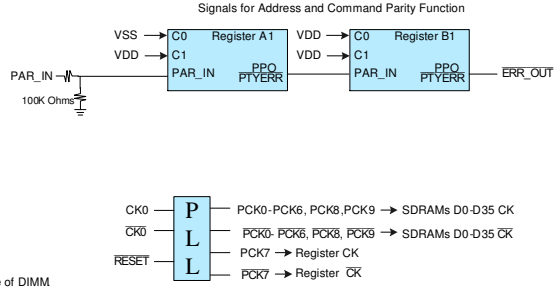
Serial Presence Detect -- Part 1 of 2 (512MB)

64Mx72 1 RANK REGISTERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	
0	Number of Serial PD Bytes Written during Production	128			80	80	80	
1	Total Number of Bytes in Serial PD device	256			08	08	08	
2	Fundamental Memory Type	DDR2-SDRAM			08	08	08	
3	Number of Row Addresses on Assembly	14			0E	0E	0E	
4	Number of Column Addresses on Assembly	10			0A	0A	0A	
5	Number of DIMM Bank	1 rank, Height=30mm			60	60	60	
6	Data Width of Assembly	X72			48	48	48	
7	Reserved	Undefined			00	00	00	
8	Voltage Interface Level of this Assembly	SSTL_1.8			05	05	05	
9	DDR2 SDRAM Device Cycle Time at CL=5	3ns	2.5ns		30	25	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.45ns	0.4ns		45	40	40	
11	DIMM Configuration Type	parity			06	06	06	
12	Refresh Rate/Type	7.8us/SR			82	82	82	
13	Primary DDR2 SDRAM Width	X8			08	08	08	
14	Error Checking DDR2 SDRAM Device Width	X8	Undefined		08	00	00	
15	Reserved	Undefined			00	00	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C	0C	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04	04	04	
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3/4/5	4/5/6	3/4/5	38	70	38	
19	DIMM Mechanical Characteristics	<4.10mm			01	01	01	
20	DDR2 SDRAM DIMM Type Information	Reg. DIMM			01	01	01	
21	DDR2 SDRAM Module Attributes:	PLL=1, Register =1			04	04	04	
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50ohm ODT, and PASR			07	07	07	
23	Minimum Clock Cycle at CL=5	3.75ns	3ns	3.75ns	3D	30	3D	
24	Maximum Data Access Time from Clock at CL=5	±0.5ns	±0.45ns	±0.5ns	50	45	50	
25	Minimum Clock Cycle Time at CL=3	5ns	3.75ns	5ns	50	3D	50	
26	Maximum Data Access Time from Clock at CL=3	±0.6ns	±0.5ns	±0.6ns	60	50	60	
27	Minimum Row Precharge Time (tRP)	15ns		12.5ns	3C	3C	32	
28	Minimum Row Active to Row Active delay (tRRD)	7.5ns			1E	1E	1E	
29	Minimum RAS to CAS delay (tRCD)	15ns		12.5ns	3C	3C	32	
30	Minimum RAS Pulse Width (tRAS)	45ns			2D	2D	2D	
31	Module Bank Density	512MB			80	80	80	
32	Address and Command Setup Time Before Clock (tIS)	0.2ns	0.17ns		20	17	17	
33	Address and Command Hold Time After Clock (tIH)	0.275ns	0.25ns		27	25	25	
34	Data Input Setup Time Before Clock (tDS)	0.10ns	0.05ns		10	05	05	
35	Data Input Hold Time After Clock (tDH)	0.17ns	0.12ns		17	12	12	
36	Write Recovery Time (tWR)	15.0ns			3C	3C	3C	
37	Internal Write to Read Command delay (tWTR)	7.5ns			1E	1E	1E	
38	Internal Read to Precharge delay (tRTP)	7.5ns			1E	1E	1E	
39	Reserved	Undefined			00	00	00	
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns			00	00	30	
41	Minimum Core Cycle Time (tRC)	60ns		57ns	3C	3C	39	

Serial Presence Detect -- Part 2 of 2 (512MB)

64Mx72 1 RANK REGISTERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	
42	Min. Auto Refresh Command Cycle Time (tRFC)	105ns			69	69	69	
43	Maximum Clock Cycle Time (tCK)	8.0ns			80	80	80	
44	Max. DQS-DQ Skew Factor (tDQS)	0.24ns	0.2ns		18	14	14	
45	Read Data Hold Skew Factor (tQHS)	0.34ns	0.3ns		22	1E	1E	
46	PLL Relock Time	15.0µs			0F	0F	0F	
47	Tcasemax	11.2	10		53	50	50	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	61˚C/W			7A	7A	7A	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	6˚C	7.2˚C		53	63	63	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	4.7˚C	6˚C		2F	3C	3C	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	0.825			37	37	37	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	5.85˚C	7.05˚C		27	2F	2F	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	3.85˚C	4.55˚C		4D	5B	5B	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	1.05˚C	1.05˚C		2A	2A	2A	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	15.2˚C	18.4˚C		4D	5C	5C	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	19˚C	20.5˚C		26	29	29	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	20˚C			28	28	28	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00	00	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00	00	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00	00	00	
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit(DT Register Active/Mode Bit)	00			00	00	00	
62	SPD Revision	1.2			12	12	12	
63	Checksum Data	Checksum Data			5C	60	7C	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-91	Module Part number	Module Part Number in ASCII			--			1
92-255	Module Revision Code	Undefined			--			

Note:
  NT512T72U89B0BV-3C ➜ 4E54353132543732553839423042562D334320
  NT512T72U89B0BV-25D ➜ 4E54353132543732553839423042562D323544
  NT512T72U89B0BV-25C ➜ 4E54353132543732553839423042562D323543

NT2GT72U4NB0BV / NT2GT72U4NB1BV
NT512T72U89B0BV / NT1GT72U4PB0BV

512MB: 64M x 72 / 1GB: 128M X 72 / 2GB: 256M X 72

Registered DDR2 SDRAM DIMM

Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx72 1 RANK REGISTERED DDR2 SDRAM DIMM based on 128Mx4, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	
0	Number of Serial PD Bytes Written during Production	128			80	80	80	
1	Total Number of Bytes in Serial PD device	256			08	08	08	
2	Fundamental Memory Type	DDR2-SDRAM			08	08	08	
3	Number of Row Addresses on Assembly	14			0E	0E	0E	
4	Number of Column Addresses on Assembly	11			0B	0B	0B	
5	Number of DIMM Bank	1 rank, Height=30mm			60	60	60	
6	Data Width of Assembly	X72			48	48	48	
7	Reserved	Undefined			00	00	00	
8	Voltage Interface Level of this Assembly	SSTL_1.8			05	05	05	
9	DDR2 SDRAM Device Cycle Time at CL=5	3ns	2.5ns		30	25	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.45ns	0.4ns		45	40	40	
11	DIMM Configuration Type	parity			06	06	06	
12	Refresh Rate/Type	7.8µs/SR			82	82	82	
13	Primary DDR2 SDRAM Width	X4			04	04	04	
14	Error Checking DDR2 SDRAM Device Width	X4			04	04	04	
15	Reserved	Undefined			00	00	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C	0C	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04	04	04	
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3/4/5	4/5/6	3/4/5	38	70	38	
19	DIMM Mechanical Characteristics	<4.10mm			01	01	01	
20	DDR2 SDRAM DIMM Type Information	Reg. DIMM			01	01	01	
21	DDR2 SDRAM Module Attributes:	PLL=1, Register=2			05	05	05	
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50ohm ODT, and PASR			07	07	07	
23	Minimum Clock Cycle at CL=5	3.75ns	3ns	3.75ns	3D	30	3D	
24	Maximum Data Access Time from Clock at CL=5	±0.5ns	±0.45ns	±0.5ns	50	45	50	
25	Minimum Clock Cycle Time at CL=3	5.0ns	3.75ns	5.0ns	50	3D	50	
26	Maximum Data Access Time from Clock at CL=3	±0.6ns	±0.5ns	±0.6ns	60	50	60	
27	Minimum Row Precharge Time (t_{RP})	15ns		12.5ns	3C	3C	32	
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns			1E	1E	1E	
29	Minimum RAS to CAS delay (t_{RCD})	15ns		12.5ns	3C	3C	32	
30	Minimum RAS Pulse Width (t_{RAS})	45ns			2D	2D	2D	
31	Module Bank Density	1GB			01	01	01	
32	Address and Command Setup Time Before Clock (t_{IS})	0.2ns	0.17ns		20	17	17	
33	Address and Command Hold Time After Clock (t_{IH})	0.27ns	0.25ns		27	25	25	
34	Data Input Setup Time Before Clock (t_{DS})	0.10ns	0.05ns		10	05	05	
35	Data Input Hold Time After Clock (t_{DH})	0.17ns	0.12ns		17	12	12	
36	Write Recovery Time (t_{WR})	15.0ns			3C	3C	3C	
37	Internal Write to Read Command delay (t_{WTR})	7.5ns			1E	1E	1E	
38	Internal Read to Precharge delay (t_{RTP})	7.5ns			1E	1E	1E	
39	Reserved	Undefined			00	00	00	
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns			00	00	30	
41	Minimum Core Cycle Time (t_{RC})	60ns		57ns	3C	3C	39	

Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx72 1 RANK REGISTERED DDR2 SDRAM DIMM based on 128Mx4, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	
42	Min. Auto Refresh Command Cycle Time (tRFC)	105ns			69	69	69	
43	Maximum Clock Cycle Time (tCK)	8.0ns			80	80	80	
44	Max. DQS-DQ Skew Factor (tDQS)	0.24ns	0.2ns		18	14	14	
45	Read Data Hold Skew Factor (tQHS)	0.34ns	0.3ns		22	1E	1E	
46	PLL Relock Time	15µs			0F	0F	0F	
47	Tcasemax	11.2	10		53	50	50	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	61˚C/W			7A	7A	7A	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	6˚C	7.2˚C		53	63	63	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	4.7˚C	6.0˚C		2F	3C	3C	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	0.825			37	37	37	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	5.85˚C	7.05˚C		27	2F	2F	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	3.85˚C	4.55˚C		4D	5B	5B	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	1.05˚C			2A	2A	2A	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	15.2˚C	18.4˚C		4C	5C	5C	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	19˚C	20.5˚C		26	29	29	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	20˚C			28	28	28	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00	00	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00	00	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00	00	00	
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit(DT Register Active/Mode Bit)	00			00	00	00	
62	SPD Revision	1.2			12	12	12	
63	Checksum Data	Checksum Data			D6	E3	FF	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-91	Module Part number	Module Part Number in ASCII			--			1
92-255	Module Revision Code	Undefined			--			

Note:
1. NT1GT72U4PB0BV-3C ➔ 4E54314754373255345042304 2562D33432020
2. NT1GT72U4PB0BV-25D ➔ 4E54314754373255345042304 2562D32354420
3. NT1GT72U4PB0BV-25C ➔ 4E54314754373255345042304 2562D32354320

Serial Presence Detect -- Part 1 of 2 (2GB)

256Mx72 2 RANKS REGISTERED DDR2 SDRAM DIMM based on 128Mx4, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	
0	Number of Serial PD Bytes Written during Production	128			80	80	80	
1	Total Number of Bytes in Serial PD device	256			08	08	08	
2	Fundamental Memory Type	DDR2-SDRAM			08	08	08	
3	Number of Row Addresses on Assembly	14			0E	0E	0E	
4	Number of Column Addresses on Assembly	11			0B	0B	0B	
5	Number of DIMM Bank	2 rank, Height=30mm			61	61	61	
6	Data Width of Assembly	X72			48	48	48	
7	Reserved	Undefined			00	00	00	
8	Voltage Interface Level of this Assembly	SSTL_1.8			05	05	05	
9	DDR2 SDRAM Device Cycle Time at CL=5	3ns	2.5ns		30	25	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.45ns	0.4ns		45	40	40	
11	DIMM Configuration Type	parity			06	06	06	
12	Refresh Rate/Type	7.8µs/SR			82	82	82	
13	Primary DDR2 SDRAM Width	X4			04	04	04	
14	Error Checking DDR2 SDRAM Device Width	X4			04	04	04	
15	Reserved	Undefined			00	00	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C	0C	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04	04	04	
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3/4/5	4/5/6	3/4/5	38	70	38	
19	DIMM Mechanical Characteristics	<4.10mm			01	01	01	
20	DDR2 SDRAM DIMM Type Information	Reg. DIMM			01	01	01	
21	DDR2 SDRAM Module Attributes:	PLL=1, Register 07=4,05=2			07	05	05	
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50ohm ODT, and PASR			07	07	07	
23	Minimum Clock Cycle at CL=5	3.75ns	3ns	3.75ns	3D	30	3D	
24	Maximum Data Access Time from Clock at CL=5	±0.5ns	±0.45ns	±0.5ns	50	45	50	
25	Minimum Clock Cycle Time at CL=3	5.0ns	3.75ns	5.0ns	50	3D	50	
26	Maximum Data Access Time from Clock at CL=3	±0.6ns	±0.5ns	±0.6ns	60	50	60	
27	Minimum Row Precharge Time (t_{RP})	15ns		12.5ns	3C	3C	32	
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns			1E	1E	1E	
29	Minimum RAS to CAS delay (t_{RCD})	15.0ns		12.5ns	3C	3C	32	
30	Minimum RAS Pulse Width (t_{RAS})	45.0ns			2D	2D	2D	
31	Module Bank Density	1GB			01	01	01	
32	Address and Command Setup Time Before Clock (t_{IS})	0.2ns	0.17ns		20	17	17	
33	Address and Command Hold Time After Clock (t_{IH})	0.27ns	0.25ns		27	25	25	
34	Data Input Setup Time Before Clock (t_{DS})	0.1ns	0.05ns		10	05	05	
35	Data Input Hold Time After Clock (t_{DH})	0.17ns	0.12ns		17	12	12	
36	Write Recovery Time (t_{WR})	15.0ns			3C	3C	3C	
37	Internal Write to Read Command delay (t_{WTR})	7.5ns			1E	1E	1E	
38	Internal Read to Precharge delay (t_{RTP})	7.5ns			1E	1E	1E	
39	Reserved	Undefined			00	00	00	
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns			00	00	30	
41	Minimum Core Cycle Time (t_{RC})	60ns		57ns	3C	3C	39	

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Serial Presence Detect -- Part 2 of 2 (2GB)

256Mx72 2 RANKS REGISTERED DDR2 SDRAM DIMM based on 128Mx4, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	DDR2-667 -3C	DDR2-800 -25D	DDR2-800 -25C	
42	Min. Auto Refresh Command Cycle Time (tRFC)	105ns			69	69	69	
43	Maximum Clock Cycle Time (tCK)	8.0ns			80	80	80	
44	Max. DQS-DQ Skew Factor (tDQS)	0.24ns	0.2ns		18	14	14	
45	Read Data Hold Skew Factor (tQHS)	0.34ns	0.3ns		22	1E	1E	
46	PLL Relock Time	15.0μs			0F	0F	0F	
47	Tcasemax	11.2	10		53	50	50	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	61˚C/W			7A	7A	7A	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	6˚C	7.2˚C		53	63	63	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	4.7˚C	5.3˚C		2F	35	35	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	0.825˚C			37	37	37	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	5.85˚C	7.05		27	2F	2F	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	3.85˚C	4.55		4D	5B	5B	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	1.05˚C			2A	2A	2A	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	15.2˚C	18.4˚C		4C	5C	5C	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	19˚C	20.5˚C		26	29	29	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	20˚C			28	28	28	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00	00	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00	00	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00	00	00	
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit(DT Register Active/Mode Bit)	00			00	00	00	
62	SPD Revision	1.2			12	12	12	
63	Checksum Data	Checksum Data			D9	DD	F9	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-91	Module Part number	Module Part Number in ASCII			--			1
92-255	Module Revision Code	Undefined			--			

Note:
1. NT2GT72U4NB0BV-3C ➜ 4E54324754373255344E423042562D33432020
2. NT2GT72U4NB0BV-25D ➜ 4E54324754373255344E423142562D32354420
3. NT2GT72U4NB0BV-25C ➜ 4E54324754373255344E423042562D32354320

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to V_{SS}	-1.0 to 2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to V_{SS}	-0.5 to 2.3	V
H_{STG}	Storage Humidity (without condensation)	5 to 95	%

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	℃	1,2,3
T_{STG}	Storage Temperature (Plastic)	-50 to 100	℃	
H_{STG}	Storage humidity (without condensation)	5 to 95	%	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	4

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. $t_{CASE} > 85℃$ ➜ $t_{REFI} = 3.9$ μs
3. All DRAM specification only support $0℃ < t_{CASE} < 85℃$
4. Up to 9850 ft.

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDQ}	I/O Supply Voltage	1.7	1.9	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	$0.49V_{DDQ}$	$0.51V_{DDQ}$	V	1, 2
$V_{IH (DC)}$	Input High (Logic1) Voltage	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V	1
$V_{IL (DC)}$	Input Low (Logic0) Voltage	-0.3	$V_{REF} - 0.125$	V	1
I_L	Input / Output Leakage Current	-5	5	μA	

Note:
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V (**512MB**, 1 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-25D)	PC2-6400 (-25C)	Unit
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	996	1094	1094	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1144	1243	1243	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	323	323	323	mA
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	748	748	748	mA
I_{DD2Q}	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	649	758	758	mA
I_{DD3PF}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	580	639	639	mA
I_{DD3PS}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	343	343	343	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	748	847	847	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	1639	1689	1689	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	1639	1738	1738	mA
I_{DD5}	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	1837	2134	2134	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	70	70	70	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	1936	2184	2184	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V (**1GB**, 1 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-25D)	PC2-6400 (-25C)	Unit
I DD0	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1826	2024	2024	mA
I DD1	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	2123	2321	2321	mA
I DD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	480	480	480	mA
I DD2N	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	1331	1331	1331	mA
I DD2Q	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	1133	1351	1351	mA
I DD3PF	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	995	1113	1113	mA
I DD3PS	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	519	519	519	mA
I DD3N	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1331	1529	1529	mA
I DD4R	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	3025	3124	3124	mA
I DD4W	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	3025	3223	3223	mA
I DD5	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	3421	4015	4015	mA
I DD6	Self-Refresh Current: CKE ≤ 0.2V	139	139	139	mA
I DD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	3707	4202	4202	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V (**2GB**, 2 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-25D)	PC2-6400 (-25C)	Unit
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	2816	3212	3212	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	3113	3509	3509	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	619	619	619	mA
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	2321	2321	2321	mA
I_{DD2Q}	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	1925	2361	2361	mA
I_{DD3PF}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	1648	1885	1885	mA
I_{DD3PS}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	698	698	698	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	2321	2717	2717	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	4015	4312	4312	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	4015	4411	4411	mA
I_{DD5}	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	4411	5203	5203	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	278	278	278	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	4697	5390	5390	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	DDR2-667 -3C		DDR2-800 -25D/25C		Unit	Notes
		Min.	Max.	Min.	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$	-0.45	+0.45	-0.4	+0.4	ns	
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$	-0.4	+0.4	-0.35	+0.35	ns	
$t_{CH\,(avg)}$	Average CK high-level width	0.48	0.52	0.48	0.52	t_{CK} (avg)	
$t_{CL\,(avg)}$	Average CK low-level width	0.48	0.52	0.48	0.52	t_{CK} (avg)	
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	Min(t_{CH} (abs), t_{CL}(abs))	-	Min(t_{CH} (abs), t_{CL}(abs))	-	ns	
$t_{CK\,(avg)}$	Clock Cycle Time	3	8	2.5	8	ns	
$t_{DH\,(base)}$	DQ and DM input hold time	175	-	125	-	ps	
$t_{DS\,(base)}$	DQ and DM input setup time	100	-	50	-	ps	
t_{IPW}	Input pulse width	0.60	-	0.60	-	t_{CK} (avg)	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	t_{CK} (avg)	
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$	-	$t_{AC\,max}$	-	$t_{AC\,max}$	ns	
$t_{LZ(DQ)}$	Data-out low-impedance time from CK/$\overline{CK}$	$2t_{AC\,min}$	$t_{AC\,max}$	$2t_{AC\,min}$	$t_{AC\,max}$	ns	
$t_{LZ(DQS)}$	DQS low-impedance time from CK/$\overline{CK}$	$t_{AC\,min}$	$t_{AC\,max}$	$t_{AC\,min}$	$t_{AC\,max}$	ns	
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.24	-	0.20	ns	
t_{QHS}	Data hold Skew Factor	-	0.34	-	0.30	ns	
t_{QH}	Data output hold time from DQS	t_{HP} -t_{QHS}	-	t_{HP} -t_{QHS}	-	ns	
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	0.25	t_{CK} (avg)	
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	t_{CK} (avg)	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.20	-	0.20	-	t_{CK} (avg)	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.20	-	0.20	-	t_{CK} (avg)	
t_{MRD}	Mode register set command cycle time	2	-	2	-	nCK	
t_{WPST}	Write postamble	0.40	0.60	0.40	0.60	t_{CK} (avg)	
t_{WPRE}	Write preamble	0.35	-	0.35	-	t_{CK} (avg)	
$t_{IH\,(base)}$	Address and control input hold time	275	-	250	-	ps	
$t_{IS\,(base)}$	Address and control input setup time	200	-	175	-	ps	
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	t_{CK} (avg)	
t_{RPST}	Read postamble	0.4	0.6	0.4	0.6	t_{CK} (avg)	
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	t_{IS} + t_{CK} + t_{IH}	-	t_{IS} + t_{CK} + t_{IH}	-	ns	
t_{RFC}	Refresh to active/Refresh command time	105				ns	

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	DDR2-667 -3C		DDR2-800 -25D/-25C		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{REFI}	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9				µs	
t_{REFI}	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8				µs	
t_{RRD}	Active bank A to Active bank B command	7.5	-	7.5	-	ns	
t_{FAW}	For Activate window	37.5	-	35	-	ns	
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$	2	-	2	-	nCK	
t_{WR}	Write recovery time	15	-	15	-	ns	
t_{DAL}	Auto precharge write recovery + precharge time	WR +t_{RP}	-	WR +t_{RP}	-	nCK	
t_{WTR}	Internal write to read command delay	7.5	-	7.5	-	ns	
t_{RTP}	Internal read to precharge command delay	7.5	-	7.5	-	ns	
t_{XSNR}	Exit self refresh to a Non-read command	t_{RFC} +10	-	t_{RFC} +10	-	ns	
t_{XSRD}	Exit self refresh to a Read command	200	-	200	-	nCK	
t_{XP}	Exit precharge power down to any Non- read command	2	-	2	-	nCK	
t_{XARD}	Exit active power down to read command	2	-	2	-	nCK	
t_{XARDS}	Exit active power down to read command	7-AL	-	8-AL	-	nCK	
t_{CKE}	CKE minimum pulse width	3	-	3	-	nCK	
t_{OIT}	OCD drive mode output delay	0	12	0	12	ns	
ODT							
t_{AOND}	ODT turn-on delay	2	2	2	2	nCK	
t_{AON}	ODT turn-on	$t_{AC(min)}$	$t_{AC(max)}$ +0.7	$t_{AC(min)}$	$t_{AC(max)}$ +0.7	ns	
t_{AONPD}	ODT turn-on (Power down mode)	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$+1	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$+1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	nCK	
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$+ 0.6	$t_{AC(min)}$	$t_{AC(max)}$+ 0.6	ns	
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$+1	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$+1	ns	
t_{ANPD}	ODT to power down entry latency	3	-	3	-	nCK	
t_{AXPD}	ODT power down exit latency	8	-	8	-	nCK	
Speed Grade Definition							
t_{RAS}	Row Active Time	45	70000	45	70000	ns	
t_{RCD}	RAS to CAS delay	15	-	15 (-25D) 12.5 (-25C)	-	ns	
t_{RC}	Row Cycle Time	60	-	60 (-25D) 57.5 (-25C)	-	ns	
t_{RP}	Row Precharge Time	15	-	15 (-25D) 12.5 (-25C)	-	ns	

Package Dimensions

(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)
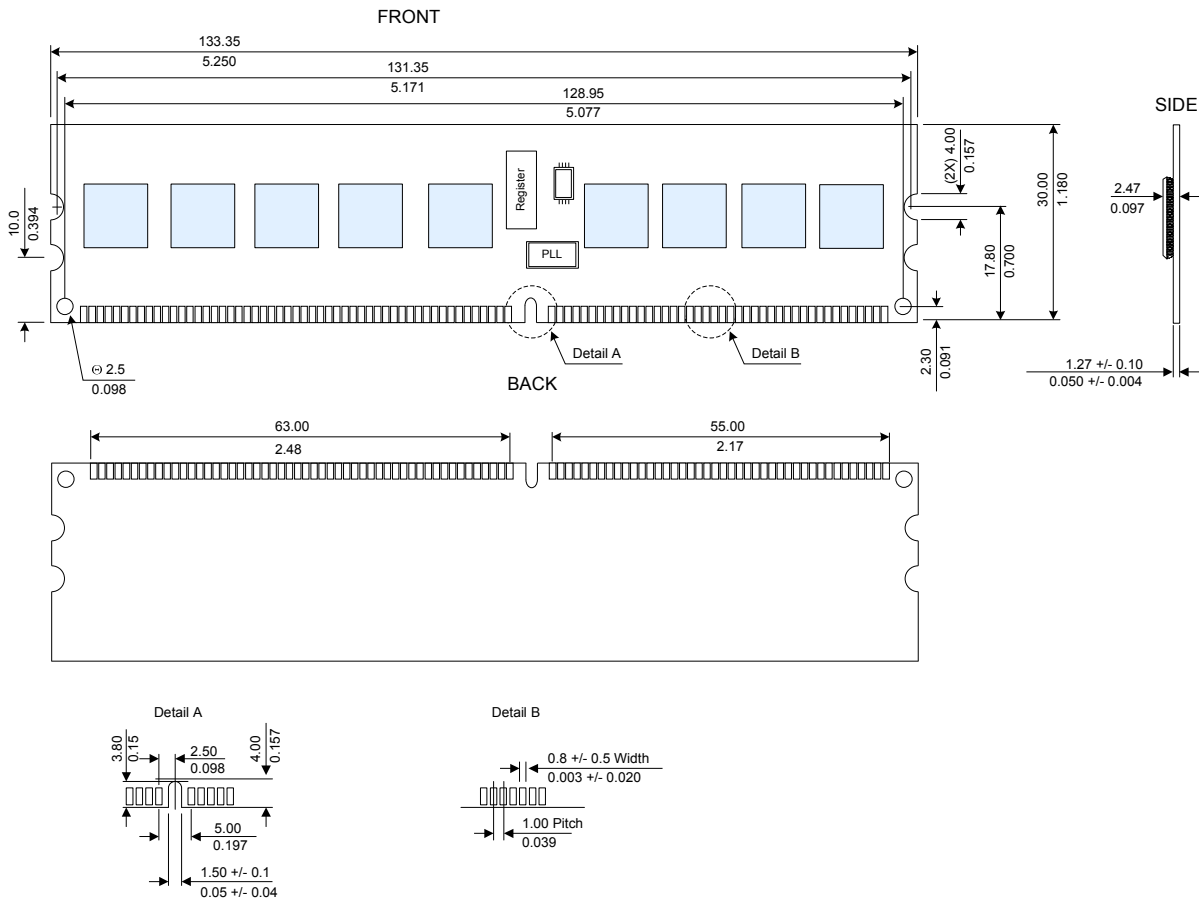
Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

*Device position is only for reference.

Package Dimensions

(1GB, 1 Rank, 128Mx4 DDR2 SDRAMs)
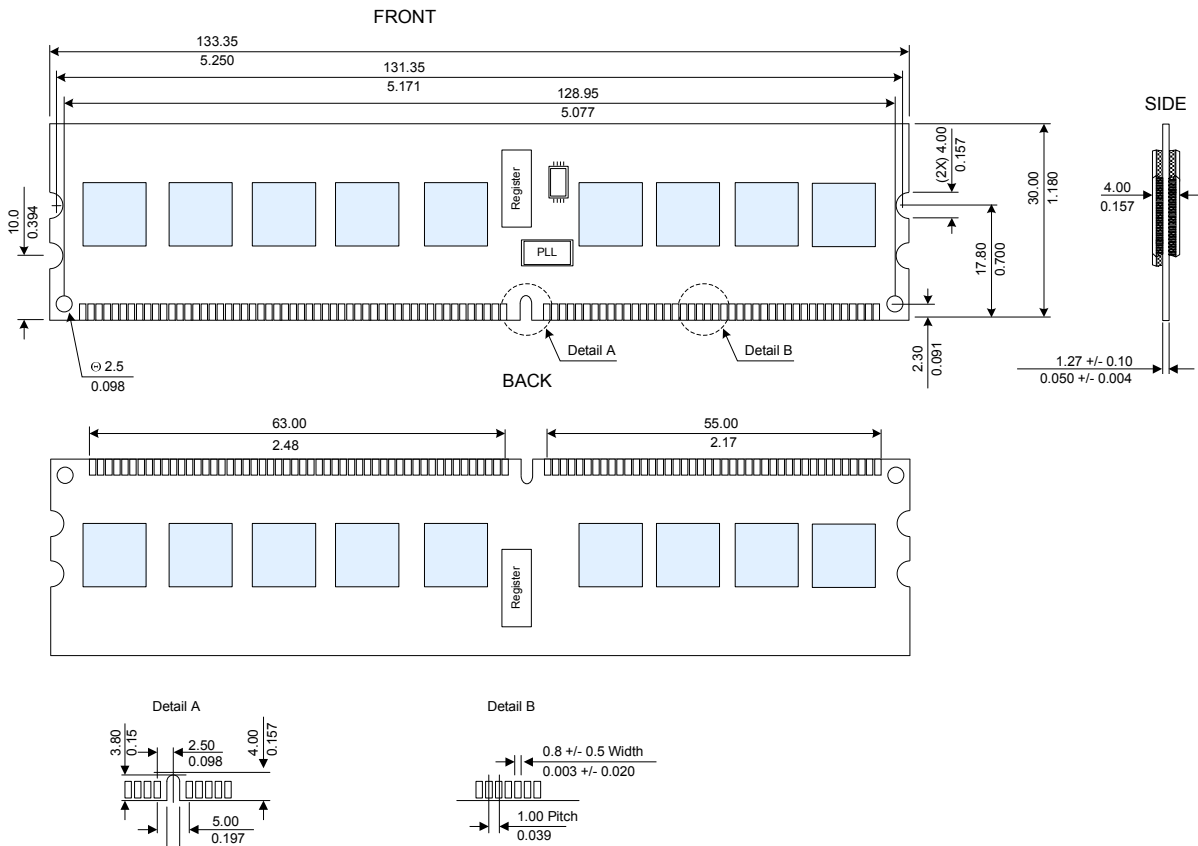
FRONT

SIDE

BACK

Detail A

Detail B

Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

*Device position is only for reference.

Package Dimensions

(2GB, 2 Ranks, 128Mx4 DDR2-667 SDRAMs)
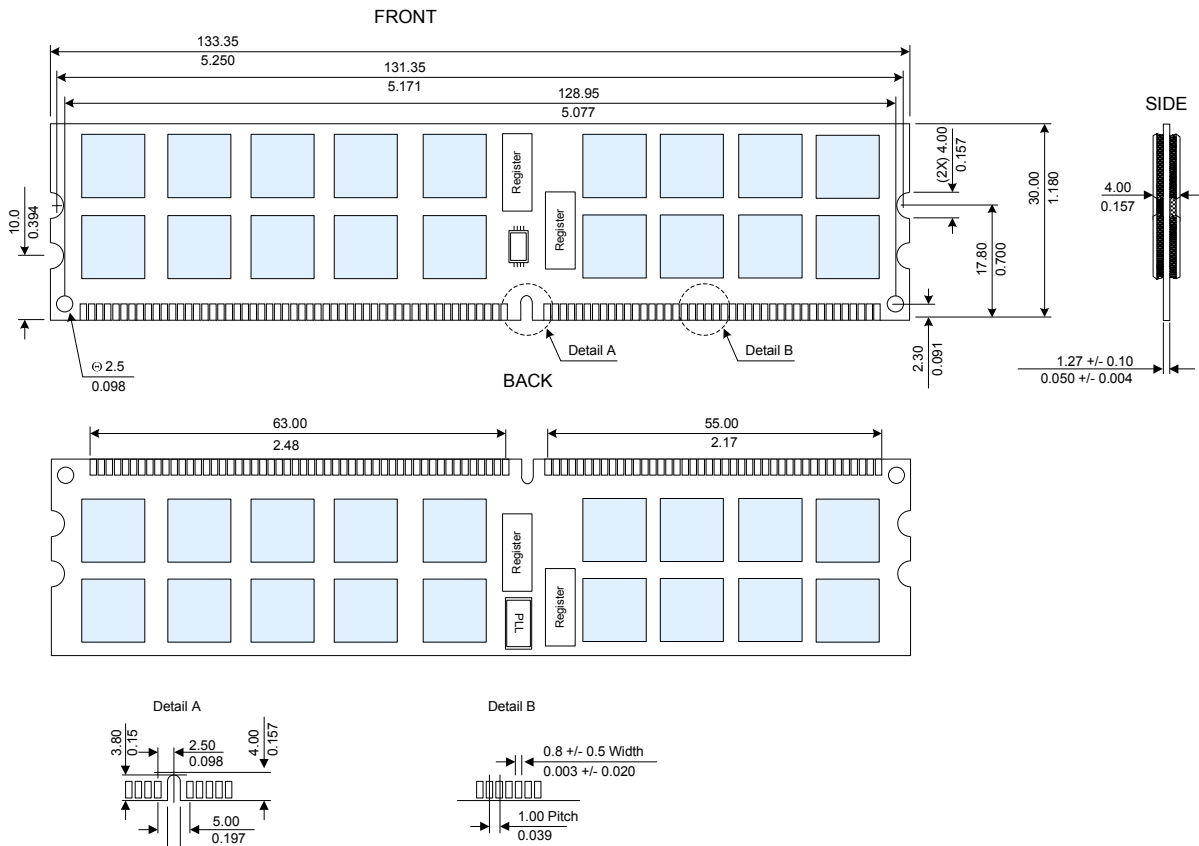
Detail A

Detail B

Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

*Device position is only for reference.

Package Dimensions

(2GB, 2 Ranks, 128Mx4 DDR2-800 SDRAMs)
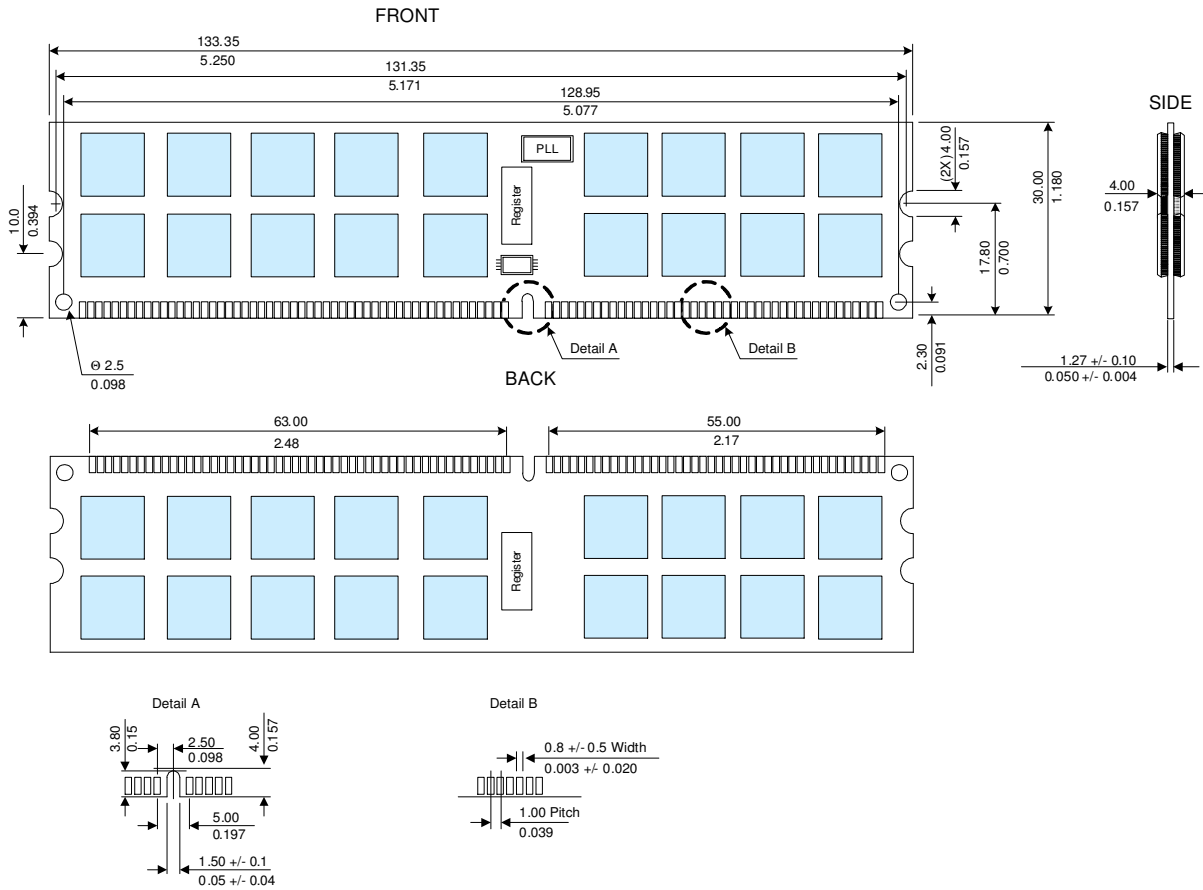
FRONT

SIDE

BACK

Detail A

Detail B

Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

*Device position is only for reference.

Revision Log

Rev	Date	Modification
0.1	09/2006	Preliminary Release.
1.0	09/2006	Official Release
1.1	02/2007	Update operating condition.
1.2	04/2007	Update SPD code (Byte 21 & Byte 63)
1.3	04/2007	Added DDR2-800 information and 1st Version PCB item information.