MOTOROLA

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input Nor Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B
8-Input NOR Gate

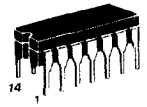
MC14081B
Quad 2-Input AND Gate

MC14082B
Dual 4-Input AND Gate

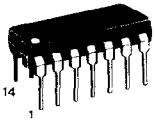
B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating Plastic "P" Package −12mW/°C from 65°C to 85°C
Ceramic "L" Package −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

CMOS SSI
(LOW-POWER COMPLEMENTARY MOS)
B-SERIES GATES

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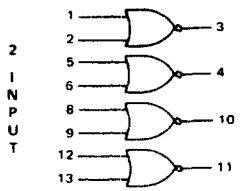
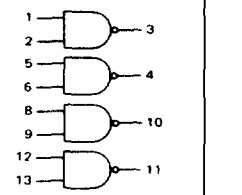
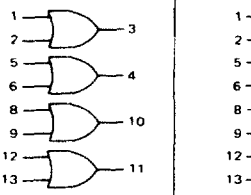
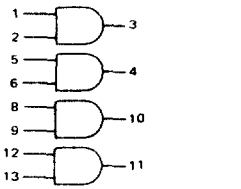
LOGIC DIAGRAMS

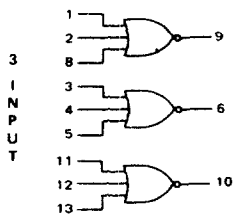
	NOR	NAND	OR	AND
2 INPUT	**MC14001B** Quad 2-Input NOR Gate	**MC14011B** Quad 2-Input NAND Gate	**MC14071B** Quad 2-Input OR Gate	**MC14081B** Quad 2-Input AND Gate
3 INPUT	**MC14025B** Triple 3-Input NOR Gate	**MC14023B** Triple 3-Input NAND Gate	**MC14075B** Triple 3-Input OR Gate	**MC14073B** Triple 3-Input AND Gate
4 INPUT	**MC14002B** Dual 4-Input NOR Gate	**MC14012B** Dual 4-Input NAND Gate	**MC14072B** Dual 4-Input OR Gate	**MC14082B** Dual 4-Input AND Gate
8 INPUT	**MC14078B** 8-Input NOR Gate	**MC14068B** 8-Input NAND Gate		

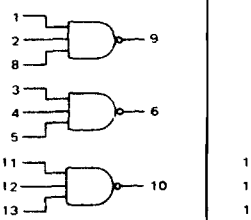


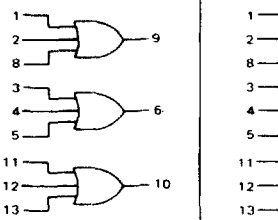


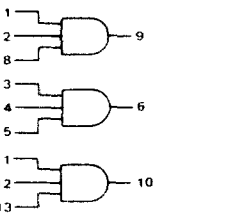


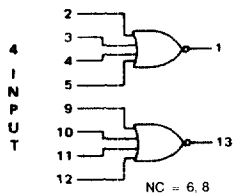


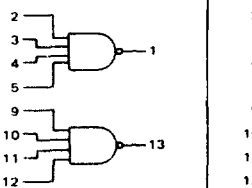


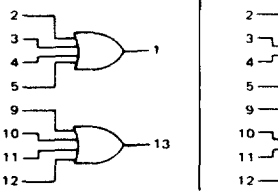


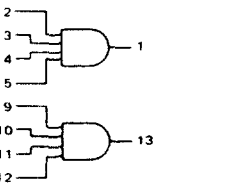


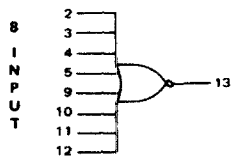


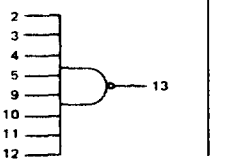












V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

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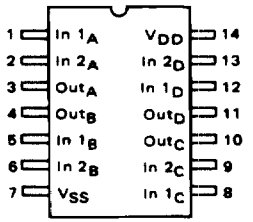
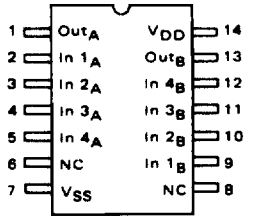
PIN ASSIGNMENTS

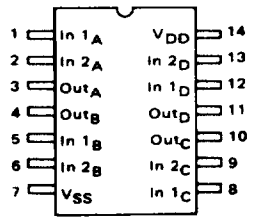
MC14001B
Quad 2-Input NOR Gate



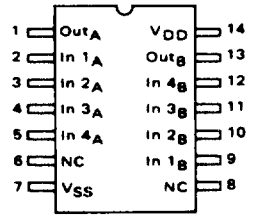
MC14002B
Dual 4-Input NOR Gate



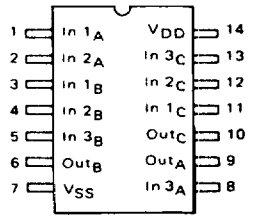
MC14011B
Quad 2-Input NAND Gate



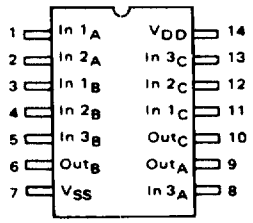
MC14012B
Dual 4-Input NAND Gate



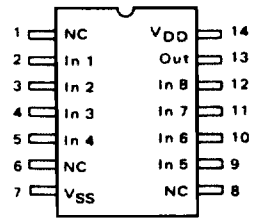
MC14023B
Triple 3-Input NAND Gate



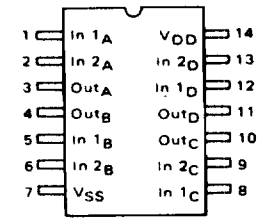
MC14025B
Triple 3-Input NOR Gate



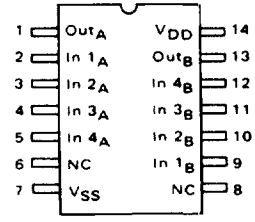
MC14068B
8-Input NAND Gate



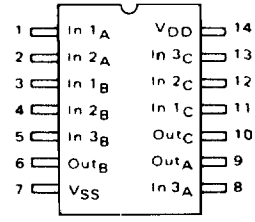
MC14071B
Quad 2-Input OR Gate



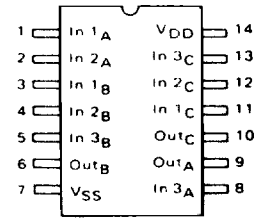
MC14072B
Dual 4-Input OR Gate



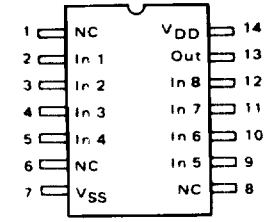
MC14073B
Triple 3-Input AND Gate



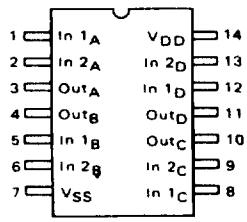
MC14075B
Triple 3-Input OR Gate



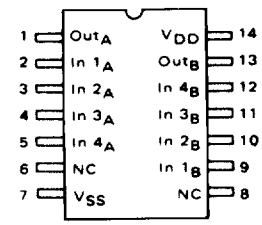
MC14078B
8-Input NOR Gate



MC14081B
Quad 2-Input AND Gate



MC14082B
Dual 4-Input AND Gate



NC = No Connection

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	0.64	–	-0.51	-0.88	–	0.36	–	
(V_{OH} = 9.5 Vdc)		10	1.6	–	-1.3	-2.25	–	0.9	–	
(V_{OH} = 13.5 Vdc)		15	4.2	–	-3.4	-8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.9 µA/kHz) f + I_{DD}/N							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

**The formulas given are for the typical characteristics only at 25°C

†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ V^2 k$$

where I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 is the number of exercised gates per package

6

B-SERIES GATE SWITCHING TIMES

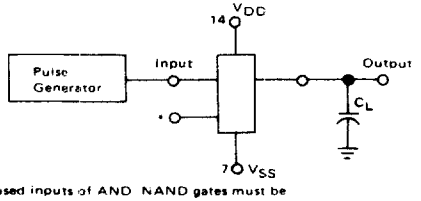
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	—	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	—	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	—	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	—	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	—	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	—	50	100	
8-Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	—	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	—	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	—	60	110	

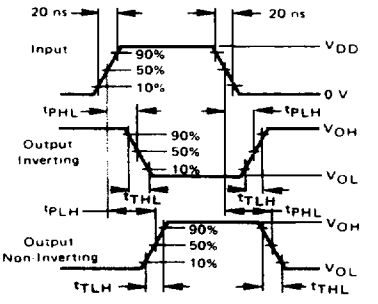
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

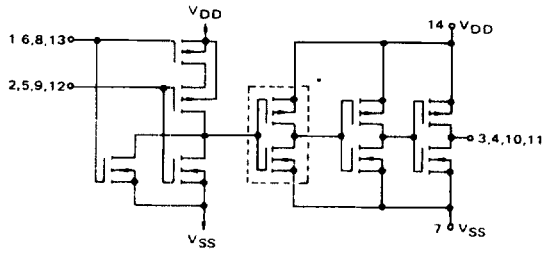


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.



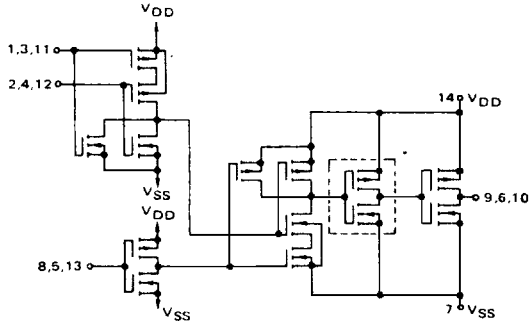
CIRCUIT SCHEMATIC
NOR, OR Gates

MC14001B
MC14071B
One of Four
Gates Shown



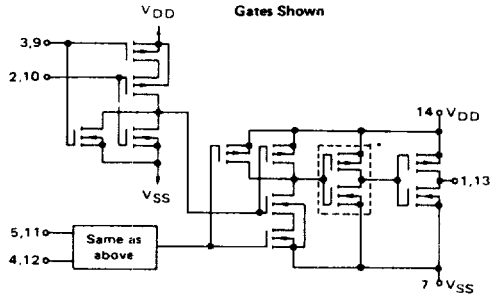
*Inverter Omitted in MC14001B

MC14025B
MC14075B
One of Three
Gates Shown

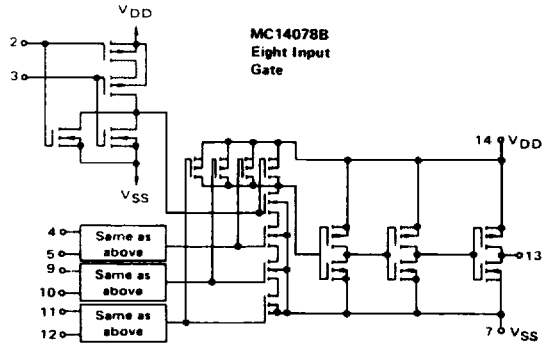


*Inverter Omitted in MC14025B

MC14002B
MC14072B
One of Two
Gates Shown



*Inverter Omitted in MC14002B

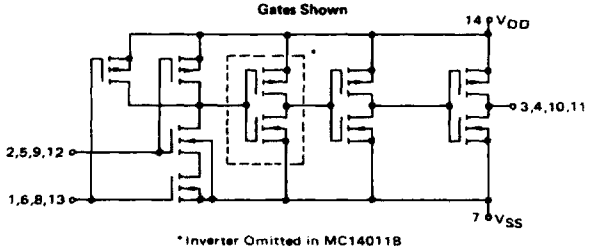


MC14078B
Eight Input
Gate

6

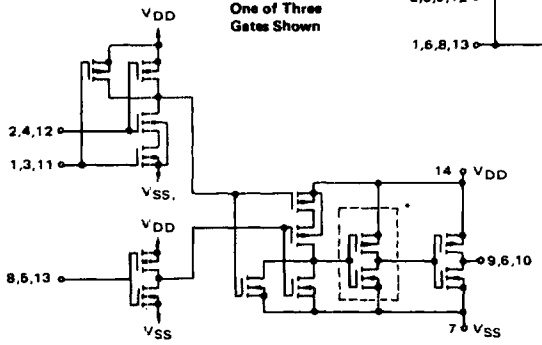
CIRCUIT SCHEMATICS
NAND, AND Gates

MC14011B
MC14081B
One of Four Gates Shown



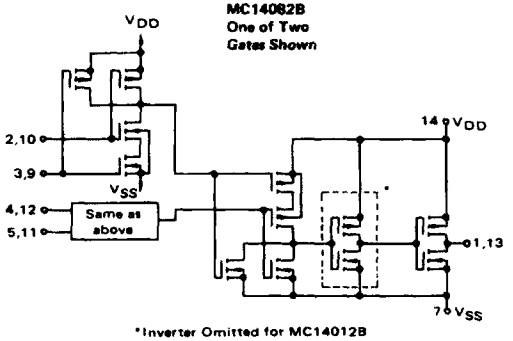
*Inverter Omitted in MC14011B

MC14023B
MC14073B
One of Three Gates Shown



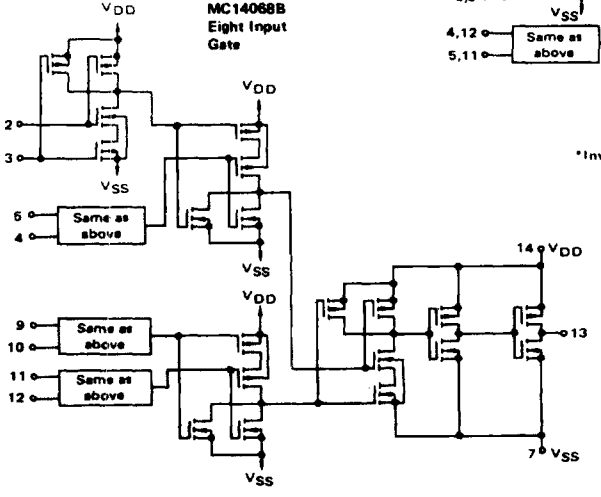
*Inverter Omitted in MC14023B

MC14012B
MC14082B
One of Two Gates Shown



*Inverter Omitted for MC14012B

MC14068B
Eight Input Gate

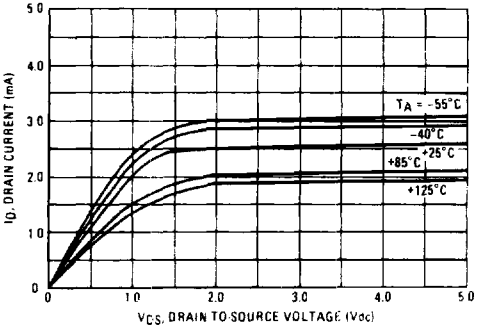


6

TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)

FIGURE 2 – V_{GS} = 5.0 Vdc



P-CHANNEL DRAIN CURRENT (SOURCE)

FIGURE 3 – V_{GS} = −5.0 Vdc

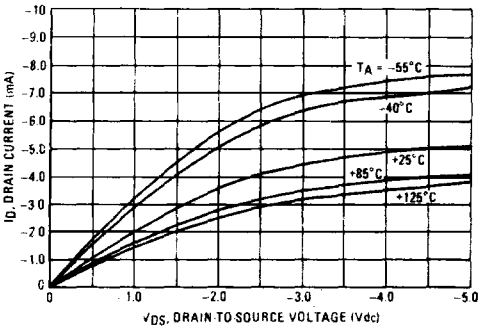


FIGURE 4 – V_{GS} = 10 Vdc

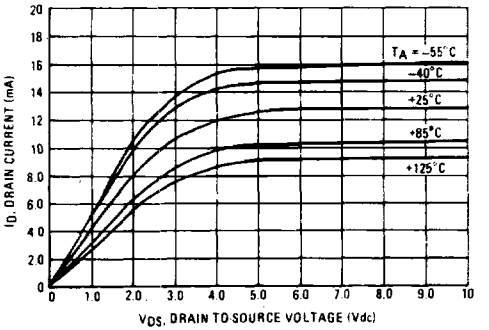


FIGURE 5 – V_{GS} = −10 Vdc

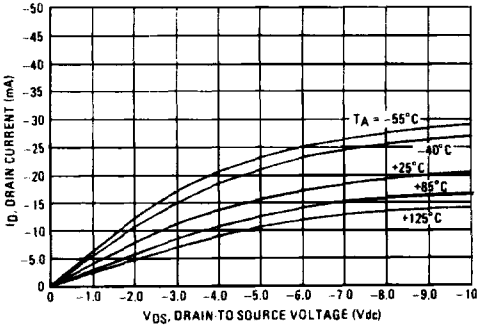


FIGURE 6 – V_{GS} = 15 Vdc

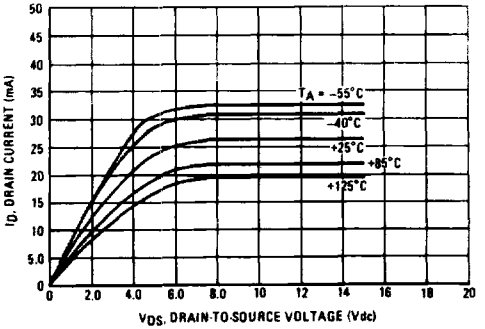
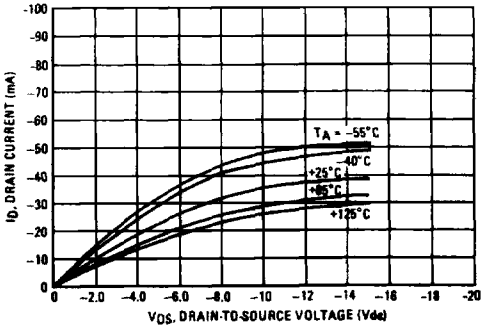


FIGURE 7 – V_{GS} = −15 Vdc



These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 – V_{DD} = 5.0 Vdc

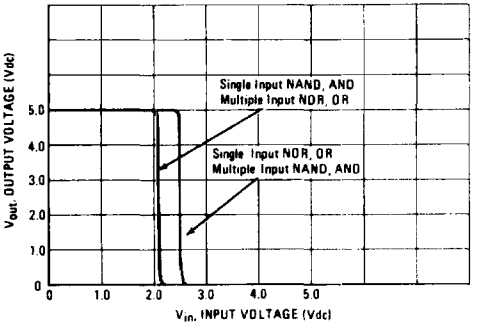


FIGURE 9 – V_{DD} = 10 Vdc

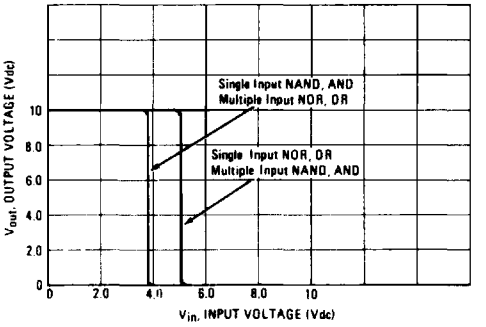
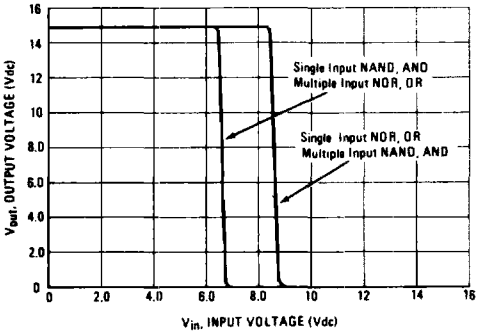


FIGURE 10 – V_{DD} = 15 Vdc



DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

1.0 V with a 5.0 V supply
2.0 V with a 10.0 V supply
2.5 V with a 15.0 V supply

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FIGURE 11 – DC NOISE IMMUNITY