

### FEATURES

- Allows Safe Board Insertion and Removal from a Live Backplane
- Controls Supply Voltages from 0.6 V to 16.5V
- Adjustable Analog Current Limit with Circuit Breaker
- Fast Response Limits Peak Fault Current
- Automatic Retry or Latch-Off On Current Fault
- Adjustable Supply Voltage Power-Up Rate
- Charge Pumped Gate Drive for External N-FET Switch
- True Soft Start control of Initial Current Profile
- TIMER pin allows control over timing functions
- Undervoltage Lockout
- Adjustable Overvoltage Protection
- 8-pin TSOT Package

### APPLICATIONS

- Hot Swap Board Insertion – Line Cards, Raid systems
- Electronic Circuit Breaker
- Industrial High Side Switch/Circuit Breaker

### GENERAL DESCRIPTION

The ADM1170 is a Hot Swap controller that allows a board to be safely inserted and removed from a live backplane. The device is capable of hot swapping a supply as low as 0.6V. An internal charge pumped driver controls the GATE of an external high side N-channel FET for a supply voltage ranging from 2.7V to 16.5V. The ADM1170 provides the initial timing cycle and allows the GATE to be ramped up at an adjustable rate.

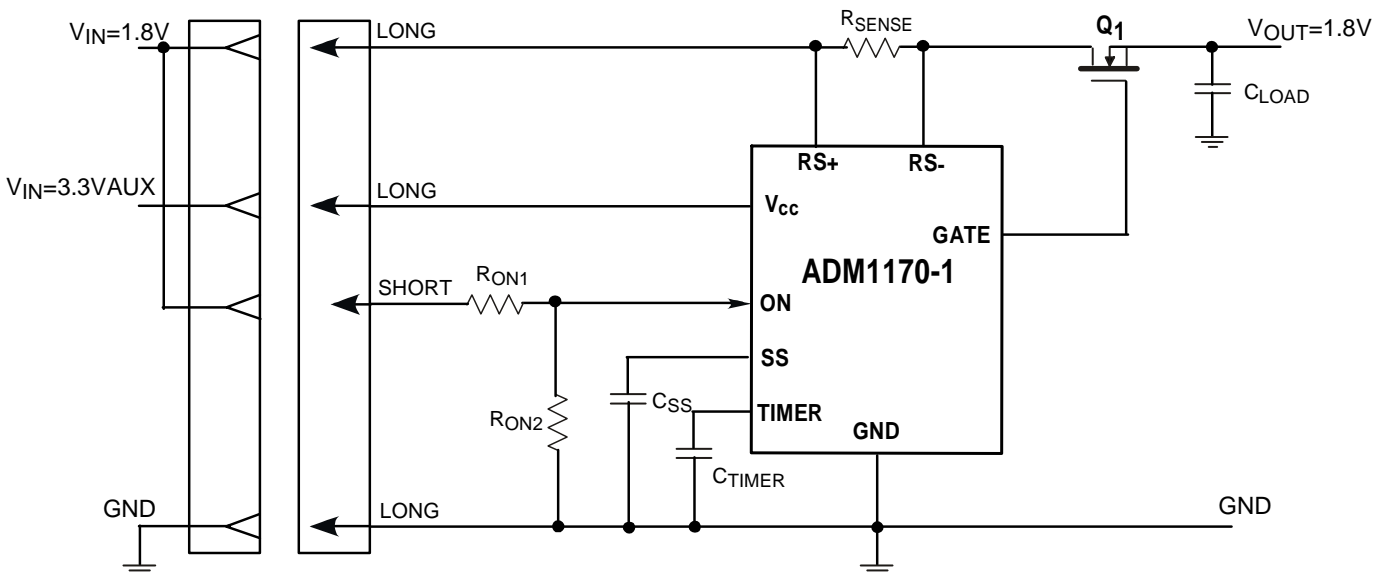
The ADM1170 features a fast current limit loop providing active current limiting together with a circuit breaker timer. The signal at the ON pin turns the part on and off and is also used for the reset function.

The SS pin allows the user to control the soft start profile of the current ramp at start-up via an external capacitor. A capacitor connected to the TIMER pin gives the user control over the duty cycle of the PWM retry ratio during current fault.

This part is available in two options: the ADM1170-1 will automatic retry for over-current fault and the ADM1170-2 will latch-off for an over-current fault.

The ADM1170 is packaged in an 8-lead TSOT package.

### APPLICATIONS DIAGRAM



### Rev.PrF

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## ADM1170—SPECIFICATIONS

Table 1.  $V_{CC} = 2.7V$  to  $16.5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Typical Values at  $T_A = 25^{\circ}C$  unless otherwise noted.

Parameter	Min	Typ	Max	Units	Conditions
<b>V<sub>CC</sub> Pin</b>					
Operating Voltage Range, $V_{CC}$	2.7		16.5	V	
Supply Current, $I_{CC}$		0.5	1.0	mA	
Undervoltage Lockout, $V_{UVLO}$	2.4	2.525	2.65	V	$V_{CC}$ Rising
Undervoltage Lockout Hysteresis, $V_{UVLOHYS}$		25		mV	
<b>ON Pin</b>					
ON Pin Input Current, $I_{INON}$	-100	0	100	nA	
On Pin Threshold, $V_{ON}$	1.26	1.3	1.34	V	ON rising
ON Pin Threshold Hysteresis, $V_{ONHYS}$		80		mV	
<b>RS+/RS- Pin</b>					
Hot Swap Voltage	0.6		16.5	V	
SENSE Pin Input Current, $I_{INSENSE}$	TBD	-200	TBD	$\mu A$	$V_{SENSE} = V_{CC}$ , $V_{HOTSWAP} = 0.6 V$ , Note
		20	30	$\mu A$	$V_{SENSE} = V_{CC}$ , $V_{HOTSWAP} > 2.2 V$
Circuit Breaker Limit Voltage, $V_{CB}$	34	47	60	mV	$V_{CB} = (V_{CC} - V_{SENSE})$ , $V_{HOTSWAP} = 0.6 V$
	44	47	53	mV	$V_{CB} = (V_{CC} - V_{SENSE})$ , $V_{HOTSWAP} > 2.2 V$
Over Current Limit Voltage, $V_{OC}$	40	53	66	mV	$V_{HOTSWAP} = 0.6 V$ , Note
	50	53	59	mV	$V_{HOTSWAP} > 2.2 V$
<b>GATE Pin</b>					
GATE Drive Voltage, $V_{GATE}$	5	6.5	10	V	$V_{GATE} - V_{CC}$ , $V_{CC} = 2.7V$
GATE Drive Voltage, $V_{GATE}$	6	8	12	V	$V_{GATE} - V_{CC}$ , $V_{CC} = 5V$
GATE Drive Voltage, $V_{GATE}$	5	6.5	10	V	$V_{GATE} - V_{CC}$ , $V_{CC} = 16.5V$
<b>Gate Pullup Current</b>	10	12	14	$\mu A$	$V_{GATE} = 0V$
<b>Gate Pulldown Current</b>		2		mA	$V_{GATE} = 3V$ , $V_{CC} > UVLO$
<b>Gate Pulldown Current</b>		25		mA	$V_{GATE} = 3V$ , $V_{CC} < UVLO$
<b>Soft Start (SS) Pin</b>					
Soft Start Pullup Current		10		$\mu A$	
Current Setting Gain		20		V/V	$V_{SS}/V_{SENSE}$
Soft Start Completion Voltage		1		V	
Pull-Down Current		100		$\mu A$	Fault
<b>TIMER Pin</b>					
TIMER Pin Pull-Up Current, $I_{TIMERUP}$	-4	-5	-6	$\mu A$	Initial Cycle, $V_{TIMER} = 1V$
	-48	-60	-72	$\mu A$	During Current Fault, $V_{TIMER} = 1V$
TIMER Pin Pull-Down Current, $I_{TIMERDN}$		2	2.5	$\mu A$	After Current Fault, $V_{TIMER} = 1V$
		100		$\mu A$	Normal Operation, $V_{TIMER} = 1V$
TIMER Pin Threshold High, $V_{TIMERH}$	1.235	1.3	1.365	V	TIMER rising
TIMER Pin Threshold Low, $V_{TIMERL}$	0.18	0.2	0.22	V	TIMER falling

## Absolute Maximum Ratings

**Table 2. ADM1170 Absolute Maximum Ratings**

Parameter	Rating
V <sub>CC</sub> Pin	20V
RS+, RS- Pins	-0.3V to 20V
V <sub>SENSE</sub> = (RS+ - RS-)	1V
TIMER Pin	-0.3V to 20V
SS Pin	-0.3V to 20V
ON Pin	-0.3V to 20V
GATE Pin	V <sub>CC</sub> + 11V
Power Dissipation	TBD
Storage Temperature	-65°C to +125°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature Range (10 sec)	300°C
Junction Temperature	150°C

## HOT CIRCUIT INSERTION

When circuit boards are inserted into live backplanes, the supply bypass capacitors can draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, glitches on the system supply or reset other boards in the system.

The ADM1170 is designed to turn a printed circuit board's supply voltage ON and OFF in a controlled manner, allowing the circuit board to be safely inserted into or removed from a live backplane. The ADM1170 can reside either on the backplane or on the daughter board for hot circuit insertion applications.

## OVERVIEW

The ADM1170 is designed to operate over a range of supplies from 2.7V to 16.5V and is capable of hot swapping as low as 0.6V. Upon insertion, an undervoltage lockout circuit determines if sufficient supply voltage is present. When the ON pin goes high an initial timing cycle assures that the board is fully seated in the backplane before the FET is turned on. A single timer capacitor sets the periods for all of the timer functions. After the initial timing cycle the ADM1170 can either start up in current limit or with a lower load current. Once the external FET is fully enhanced and the supply has ramped up, the ADM1170 monitors the load current through an external sense resistor. Overcurrent faults are actively limited to  $47\text{mV}/R_{\text{SENSE}}$  for a specified circuit breaker timer limit. The ADM1170-1 will automatically retry after a current limit fault while the ADM1170-2 latches off. The ADM1170-1 timer function limits the retry duty cycle to 3.8% for FET cooling.

## UNDervOLTAGE LOCKOUT

An internal undervoltage lockout (UVLO) circuit resets the ADM1170 if the  $V_{\text{CC}}$  supply is too low for normal operation. The UVLO has a low-to-high threshold of 2.525V, a 25mV hysteresis. Above 2.525V supply voltage, the ADM1170 will start if the ON pin conditions are met.

## ON FUNCTION

The ON pin is the input to a comparator which has a low-to-high threshold of 1.3V, an 80mV hysteresis and a high-to-low glitch filter of 30 $\mu\text{s}$  and a low-to-high glitch filter of 3 $\mu\text{s}$ . A low input on the ON pin resets the ADM1170 TIMER status and turns off the external FET by pulling the GATE pin to ground. A low-to-high transition on the ON pin starts an initial cycle followed by a start-up cycle. A 10k pull-up resistor connecting the ON pin to the supply is recommended. The 10k resistor shunts any potential static charge on the backplane and reduces the overvoltage stress at the ON pin during live insertion.

Alternatively, an external resistor divider at the ON pin can be used to program an undervoltage lockout value higher than the internal UVLO circuit. An RC filter can be added at the ON pin to increase the delay time at card insertion if the internal glitch filter delay is insufficient.

## GATE FUNCTION

During hot insertion of the PCB, an abrupt application of supply voltage charges the external FET drain/gate capacitance. This can cause an unwanted gate voltage spike. An internal circuit holds GATE low before the internal circuitry wakes up. This reduces the FET current surges substantially at insertion. The GATE pin is held low in reset mode and during the initial timing cycle. In the start-up cycle the GATE pin is pulled up by a 12 $\mu\text{A}$  current source. During an over-current fault condition, the error amplifier servos the GATE pin to maintain a constant current to the load until the circuit breaker trips. When the circuit breaker trips, the GATE pin shuts down abruptly.

## CURRENT LIMIT CIRCUIT BREAKER FUNCTION

The ADM1170 features a current limiting circuit breaker. When there is a sudden load current surge, such as a low impedance fault, the bus supply voltage can drop significantly to a point where the power to an adjacent card is affected, causing system malfunctions. The ADM1170 high bandwidth current control loop limits current by reducing the external FET GATE pin voltage. This minimizes the bus supply voltage drop and permits power budgeting and fault isolation without affecting neighbouring cards.

## CALCULATING CURRENT LIMIT

The nominal fault current limit is determined by a sense resistor connected between  $V_{\text{CC}}$  and the SENSE pin as given by the equation below:

$$I_{\text{LIMIT(NOM)}} = V_{\text{CB(NOM)}} / R_{\text{SENSE}} \quad (1)$$

The minimum load current is given by Equation 2:

$$I_{\text{LIMIT(MIN)}} = V_{\text{CB(MIN)}} / R_{\text{SENSE(MAX)}} \quad (2)$$

The maximum load current is given by Equation 3:

$$I_{\text{LIMIT(MAX)}} = V_{\text{CB(MAX)}} / R_{\text{SENSE(MIN)}} \quad (3)$$

Note: The power rating of the sense resistor should be rated at the fault current level.

For proper operation, the minimum current limit must exceed the circuit maximum operating load current with margin. The sense resistor power rating must exceed  $V_{\text{CB(MAX)}}^2 / R_{\text{SENSE(MIN)}}$ .

**TIMER FUNCTION**

The TIMER pin handles several key functions with an external capacitor,  $C_{TIMER}$ . There are two comparator thresholds: COMP1 (0.2V) and COMP2 (1.3V). The four timing current sources are:

- 5 $\mu$ A pull-up
- 60 $\mu$ A pull-up
- 2 $\mu$ A pull-down
- 100 $\mu$ A pull-down

The 100 $\mu$ A is a non-ideal current source approximating a 7k resistor below 0.4V.

**INITIAL TIMING CYCLE**

When the card is being inserted into the bus connector, the long pins mate first which brings up the supply  $V_{IN}$  at time point 1 of Figure 3. The ADM1170 is in reset mode as the ON pin is low. GATE is pulled low and the TIMER pin is pulled low with a 100 $\mu$ A source. At time point 2, the short pin makes contact and ON is pulled high. At this instant, a start-up check requires that the supply voltage be above  $UVLO$ , the ON pin be above 1.3V and the TIMER pin voltage be less than 0.2V. When these three conditions are fulfilled, the initial cycle begins and the TIMER pin is pulled high with 5 $\mu$ A. At time point 3, the TIMER reaches the COMP2 threshold and the first portion of the initial cycle ends. The 100 $\mu$ A current source then pulls down the TIMER pin until it reaches 0.2V at time point 4. The initial cycle delay (time point 2 to time point 4) is related to  $C_{TIMER}$  by equation:

$$t_{INITIAL} \sim 272.9 \times C_{TIMER} \text{ ms}/\mu\text{F} \tag{4}$$

When the initial cycle terminates, a start-up cycle is activated and the GATE pin ramps high. The TIMER pin continues to be pulled down towards ground.

**SOFT START (SS PIN)**

The SS pin is used to determine the inrush current profile. A capacitor should be attached to this pin. Whenever the FET is requested to turn on, the SS pin is held at ground until the SENSE voltage reaches a few mV. A current source is then turned on, which linearly ramps the capacitor up to 1V. The reference voltage for the GATE linear control amplifier is derived from the soft start voltage, such that the inrush linear current limit is defined as:  $I_{LIMIT} = V_{SS} / (20 \times R_{SENSE})$

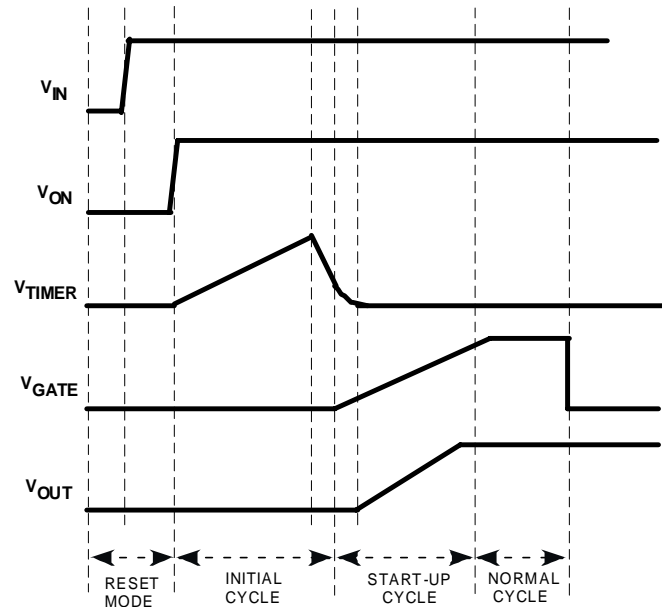


Figure 1: Normal Start-up

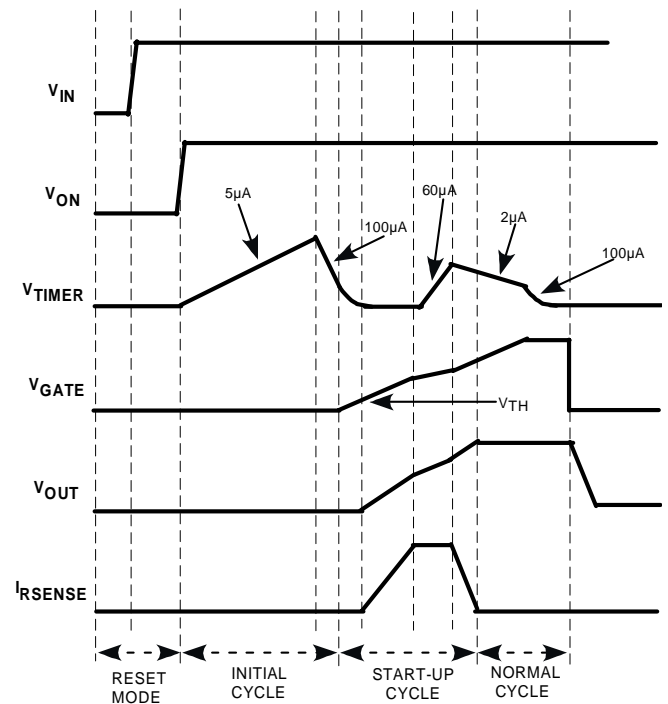
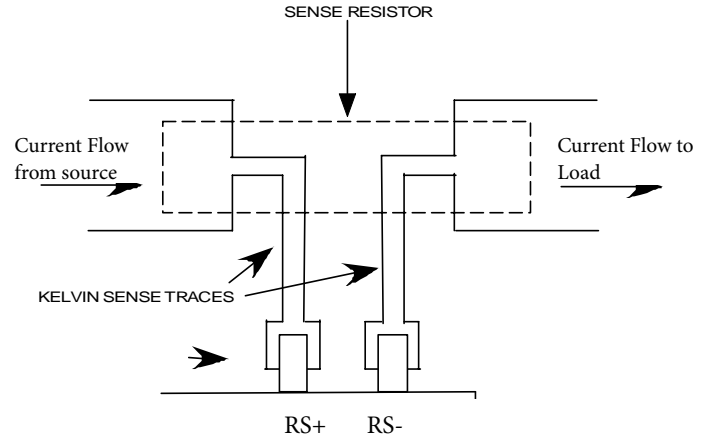


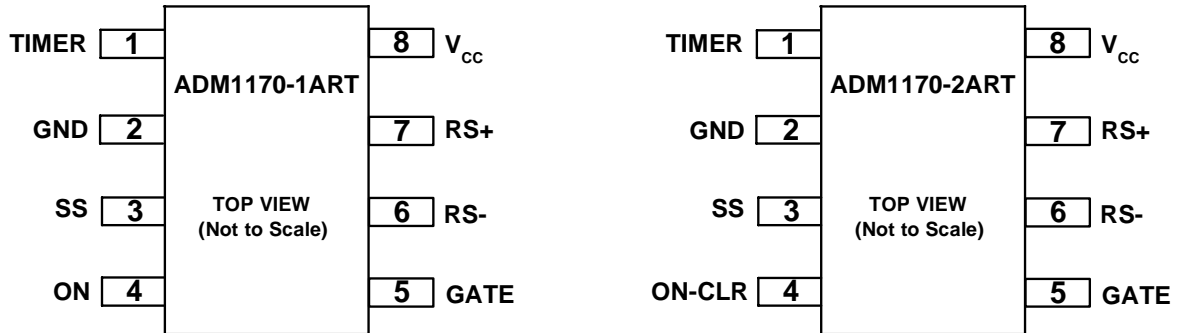
Figure 2: Current Limiting at Start-up

### KELVIN SENSE RESISTOR CONNECTION

When using a low-value sense resistor for high current measurement the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 18 below shows the correct way to connect the sense resistor between the RS+ and RS- pins of the ADM1170.



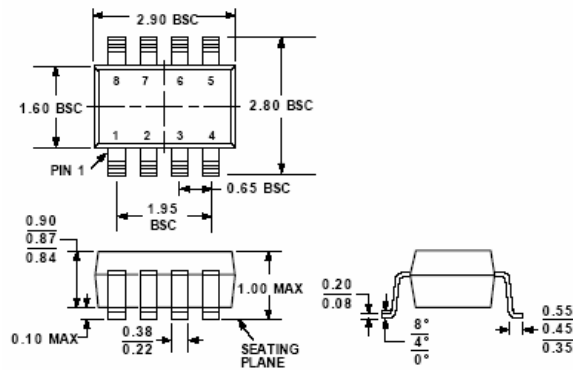
## PIN CONFIGURATIONS



## PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Name	Description
1	TIMER	Timer Input Pin. An external capacitor $C_{TIMER}$ sets a 272.9ms/ $\mu$ F initial timing delay and a 21.7ms/ $\mu$ F circuit breaker delay. The GATE pin turns off whenever the TIMER pin is pulled beyond the upper threshold, such as for overvoltage detection with an external zener.
2	GND	Chip Ground Pin
3	SS	Soft Start pin. An external capacitor between the SS pin and GND sets the ramp rate of the load current profile at initial connection.
4	ON (ON-CLR)	Input Pin. The ON pin comparator has a low-to-high threshold of 1.3V with 80mV hysteresis and a glitch filter. When the ON pin is low, the ADM1170 is reset. When the ON pin goes high, the GATE turns on after the initial timing cycle. On the ADM1170-2, a rising edge on this pin has the added function of clearing a fault and restarting the device
5	GATE	GATE Output Pin. This pin is the high side gate drive of an external N-channel FET. An internal charge pump provides a 12 $\mu$ A pull-up current with Zener clamps to RS+ and ground. In overload, the error amplifier (EA) controls the external FET to maintain a constant load current.
6,7	RS+, RS-	Current Limit Sense Input Pins. A sense resistor between the RS+ and RS- pins sets the analog current limit. In overload, the EA controls the external FET gate to maintain the SENSE voltage at 47mV. When the EA is maintaining current limit, the TIMER circuit breaker mode is activated. The current limit loop/circuit breaker mode can be disabled by connecting the RS+ pin and RS- pin together.
8	V <sub>cc</sub>	Positive Supply Input Pin. The operating supply voltage range is between 2.7V to 16.5V. An undervoltage lockout (UVLO) circuit with a glitch filter resets the ADM1170 when a low supply voltage is detected.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-193BA

Figure 3. 8-Lead TSOT Package (UJ-8)—Dimensions shown in millimeters

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 3. Ordering Guide

Part Number	Version	Temperature Package	Package Description	Package Outline
ADM1170-1AUJ	Automatic Retry Version	-40°C to +85°C	TSOT	UJ-8
ADM1170-2AUJ	Latched Off Version	-40°C to +85°C	TSOT	UJ-8