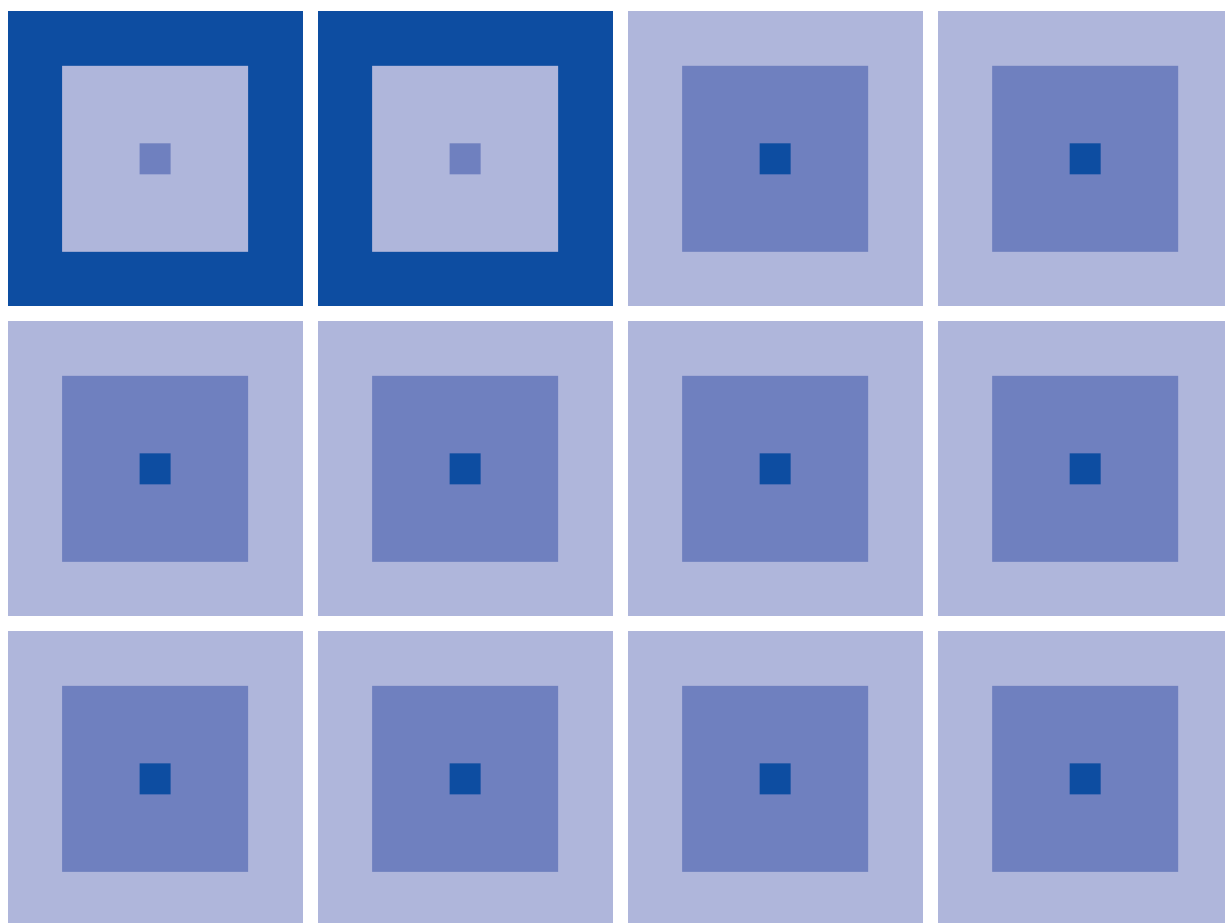


CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

**S1C63657**

Technical Manual



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# Configuration of product number

## Devices

S1 C 63158 F 0A01 00

### Packing specifications

[00 : Besides tape & reel  
0A : TCP BL 2 directions  
0B : Tape & reel BACK  
0C : TCP BR 2 directions  
0D : TCP BT 2 directions  
0E : TCP BD 2 directions  
0F : Tape & reel FRONT  
0G : TCP BT 4 directions  
0H : TCP BD 4 directions  
0J : TCP SL 2 directions  
0K : TCP SR 2 directions  
0L : Tape & reel LEFT  
0M : TCP ST 2 directions  
0N : TCP SD 2 directions  
0P : TCP ST 4 directions  
0Q : TCP SD 4 directions  
0R : Tape & reel RIGHT  
99 : Specs not fixed

### Specification

### Package

[D: die form; F: QFP, B: BGA]

### Model number

### Model name

[C: microcomputer, digital products]

### Product classification

[S1: semiconductor]

## Development tools

S5U1 C 63000 A1 1 00

### Packing specifications

[00: standard packing]

### Version

[1: Version 1]

### Tool type

[Hx : ICE  
Ex : EVA board  
Px : Peripheral board  
Wx: Flash ROM writer for the microcomputer  
Xx : ROM writer peripheral board  
Cx : C compiler package  
Ax : Assembler package  
Dx : Utility tool by the model  
Qx : Soft simulator

### Corresponding model number

[63000: common to S1C63 Family]

### Tool classification

[C: microcomputer use]

### Product classification

[S5U1: development tool for semiconductor products]



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# CHAPTER 1 OUTLINE

The S1C63657 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (8,192 words  $\times$  13 bits), RAM (1,024 words  $\times$  4 bits), multiply-divide circuit, watchdog timer, programmable timer, time base counter, an LCD driver that can drive a maximum 56 segments  $\times$  8 commons, sound generator and R/f converter built-in. The S1C63657 features low current consumption, this makes it suitable for battery driven portable equipment with R/f converter.

## 1.1 Features

---

OSC1 oscillation circuit .....	32.768 kHz (Typ.) crystal oscillation circuit
OSC3 oscillation circuit .....	4 MHz (Max.) ceramic (2 MHz Max. when OSC3 is used as the R/f converter operating clock) or 1.1 MHz (Typ.) CR oscillation circuit (*1)
Instruction set .....	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time .....	During operation at 32.768 kHz: 61 $\mu$ sec    122 $\mu$ sec    183 $\mu$ sec During operation at 4 MHz:    0.5 $\mu$ sec    1 $\mu$ sec    1.5 $\mu$ sec
ROM capacity .....	Code ROM:    8,192 words $\times$ 13 bits Data ROM:    2,048 words $\times$ 4 bits
RAM capacity .....	Data memory: 1,024 words $\times$ 4 bits Display memory: 160 words $\times$ 4 bits
Input port .....	8 bits (Pull-down resistors may be supplemented *1)
Output port .....	8 bits (It is possible to switch the 2 bits to special output *2)
I/O port .....	8 bits
LCD driver .....	56 segments $\times$ 4, 5 or 8 commons (*2)
Time base counter .....	Clock timer
Programmable timer .....	8-bit timer $\times$ 3 ch., 16-bit timer $\times$ 1 ch. + 8-bit timer $\times$ 1 ch., 8-bit PWM $\times$ 2 ch. + 8-bit timer $\times$ 1 ch. or 16-bit PWM $\times$ 1 ch. + 8-bit timer $\times$ 1 ch. (*2)
Watchdog timer .....	Built-in
Sound generator .....	With envelope and 1-shot output functions
R/f converter .....	2 ch., CR oscillation type, 20-bit counter Supports resistive humidity sensors
Multiply-divide circuit .....	8-bit accumulator $\times$ 1 ch. Multiplication: 8 bits $\times$ 8 bits $\rightarrow$ 16-bit product Division:    16 bits $\div$ 8 bits $\rightarrow$ 8-bit quotient and 8-bit remainder
External interrupt .....	Input port interrupt:    2 systems
Internal interrupt .....	Clock timer interrupt:    4 systems Programmable timer interrupt: 5 systems R/f converter interrupt:    2 systems
Power supply voltage .....	2.4 to 3.6 V: Max. 4 MHz operation in normal mode 2.4 to 3.6 V: 32 kHz operation in halver mode 1.8 to 3.6 V: 32 kHz operation in normal mode
Operating temperature range .....	-20 to 70°C
Current consumption (Typ.) .....	Low-speed operation (OSC1 = 32 kHz crystal oscillation): During HALT    3.0 V (LCD ON, halver mode)    0.65 $\mu$ A During operation    3.0 V (LCD ON, halver mode)    2.5 $\mu$ A High-speed operation (OSC3 = 4 MHz ceramic oscillation): During operation    3.0 V (LCD ON)    800 $\mu$ A
Package .....	Chip (no Polyimide)

\*1: Can be selected with mask option    \*2: Can be selected with software

## 1.2 Block Diagram

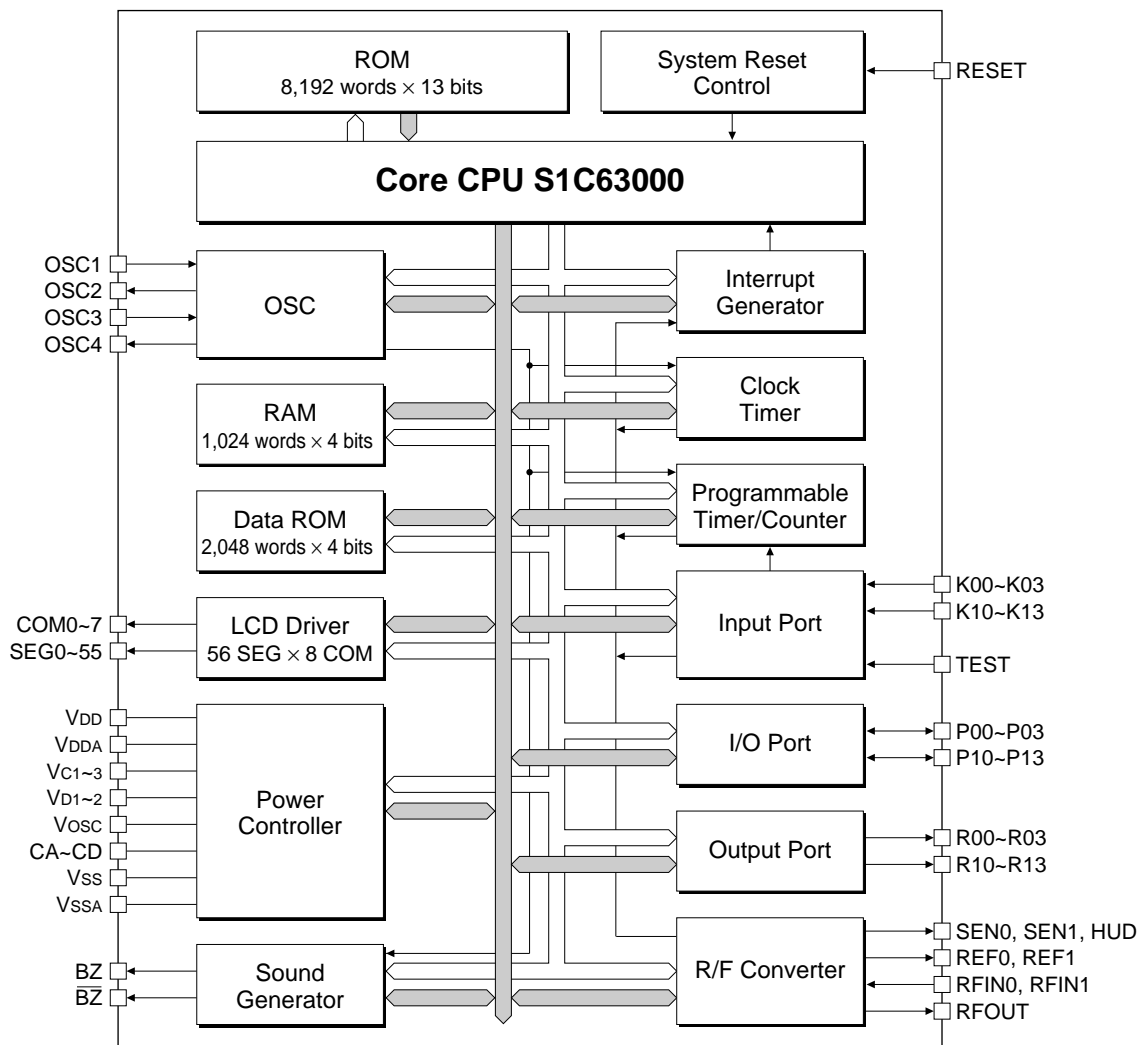


Fig. 1.2.1 Block diagram

## 1.3 Pad

### 1.3.1 Diagram of pad layout

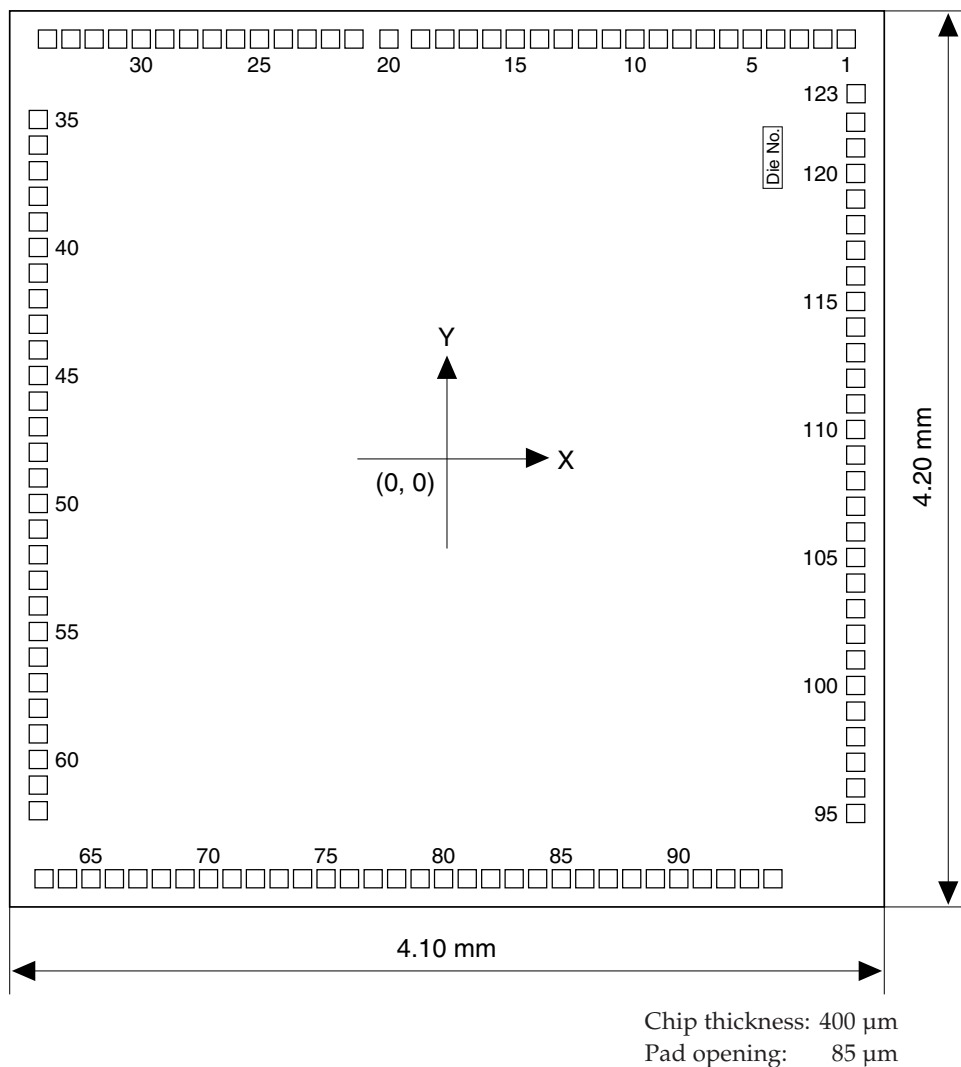


Fig. 1.3.1.1 Pad layout diagram

### 1.3.2 Pad coordinates

Table 1.3.2.1 Pin coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	COM1	1.872	1.968	42	SEG35	-1.916	0.751	83	P13	0.315	-1.968
2	COM2	1.762	1.968	43	SEG36	-1.916	0.631	84	R00	0.425	-1.968
3	COM3	1.652	1.968	44	SEG37	-1.916	0.511	85	R01	0.536	-1.968
4	CA	1.541	1.968	45	SEG38	-1.916	0.391	86	R02	0.646	-1.968
5	CB	1.431	1.968	46	SEG39	-1.916	0.271	87	R03	0.756	-1.968
6	VC1	1.321	1.968	47	SEG40	-1.916	0.151	88	R10	0.866	-1.968
7	VC2	1.211	1.968	48	SEG41	-1.916	0.031	89	R11	0.977	-1.968
8	VC3	1.101	1.968	49	SEG42	-1.916	-0.089	90	R12	1.087	-1.968
9	N.C.	0.991	1.968	50	SEG43	-1.916	-0.209	91	R13	1.197	-1.968
10	N.C.	0.881	1.968	51	SEG44	-1.916	-0.329	92	BZ	1.307	-1.968
11	N.C.	0.771	1.968	52	SEG45	-1.916	-0.449	93	BZ	1.418	-1.968
12	VSSA	0.659	1.968	53	SEG46	-1.916	-0.569	94	Vss	1.528	-1.968
13	RFOUT	0.545	1.968	54	SEG47	-1.916	-0.689	95	SEG0	1.916	-1.662
14	RFIN0	0.434	1.968	55	SEG48	-1.916	-0.809	96	SEG1	1.916	-1.542
15	RFIN1	0.320	1.968	56	SEG49	-1.916	-0.929	97	SEG2	1.916	-1.422
16	REF0	0.210	1.968	57	SEG50	-1.916	-1.049	98	SEG3	1.916	-1.302
17	SEN0	0.100	1.968	58	SEG51	-1.916	-1.169	99	SEG4	1.916	-1.182
18	REF1	-0.010	1.968	59	SEG52	-1.916	-1.289	100	SEG5	1.916	-1.062
19	SEN1	-0.124	1.968	60	SEG53	-1.916	-1.409	101	SEG6	1.916	-0.942
20	HUD	-0.272	1.968	61	SEG54	-1.916	-1.529	102	SEG7	1.916	-0.822
21	VDDA	-0.436	1.968	62	SEG55	-1.916	-1.649	103	SEG8	1.916	-0.702
22	CC	-0.546	1.968	63	COM4	-1.889	-1.968	104	SEG9	1.916	-0.582
23	CD	-0.656	1.968	64	COM5	-1.779	-1.968	105	SEG10	1.916	-0.462
24	Vd2	-0.767	1.968	65	COM6	-1.669	-1.968	106	SEG11	1.916	-0.342
25	VDD	-0.879	1.968	66	COM7	-1.559	-1.968	107	SEG12	1.916	-0.222
26	VOsc	-0.991	1.968	67	VDD	-1.449	-1.968	108	SEG13	1.916	-0.102
27	OSC1	-1.101	1.968	68	K00	-1.339	-1.968	109	SEG14	1.916	0.018
28	OSC2	-1.211	1.968	69	K01	-1.228	-1.968	110	SEG15	1.916	0.138
29	Vd1	-1.323	1.968	70	K02	-1.118	-1.968	111	SEG16	1.916	0.258
30	OSC3	-1.433	1.968	71	K03	-1.008	-1.968	112	SEG17	1.916	0.378
31	OSC4	-1.544	1.968	72	K10	-0.898	-1.968	113	SEG18	1.916	0.498
32	Vss	-1.654	1.968	73	K11	-0.787	-1.968	114	SEG19	1.916	0.618
33	TEST	-1.763	1.968	74	K12	-0.677	-1.968	115	SEG20	1.916	0.738
34	RESET	-1.873	1.968	75	K13	-0.567	-1.968	116	SEG21	1.916	0.858
35	SEG28	-1.916	1.591	76	P00	-0.457	-1.968	117	SEG22	1.916	0.978
36	SEG29	-1.916	1.471	77	P01	-0.346	-1.968	118	SEG23	1.916	1.098
37	SEG30	-1.916	1.351	78	P02	-0.236	-1.968	119	SEG24	1.916	1.218
38	SEG31	-1.916	1.231	79	P03	-0.126	-1.968	120	SEG25	1.916	1.338
39	SEG32	-1.916	1.111	80	P10	-0.016	-1.968	121	SEG26	1.916	1.458
40	SEG33	-1.916	0.991	81	P11	0.095	-1.968	122	SEG27	1.916	1.578
41	SEG34	-1.916	0.871	82	P12	0.205	-1.968	123	COM0	1.918	1.712

## 1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pad No.	I/O	Function
VDD	25, 67	–	Power (+) supply pin
VSS	32, 94	–	Power (–) supply pin
VDDA	21	–	Analog system power (+) supply pin (=VDD)
VSSA	12	–	Analog system power (–) supply pin (=VSS)
VD1	29	–	Internal logic system regulated voltage output pin
VD2	24	–	1/2VDD voltage halver output pin
VOsc	26	–	Oscillation system regulated voltage output pin
VC1–VC3	6–8	–	LCD system power supply pin
CA, CB	4, 5	–	LCD system voltage booster capacitor connecting pin
CC, CD	22, 23	–	Voltage halver capacitor connecting pin
OSC1	27	I	Crystal oscillation input pin
OSC2	28	O	Crystal oscillation output pin
OSC3	30	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	31	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	68–71	I	Input port pins
K10–K13	72–75	I	Input port pins
P00–P03	76–79	I/O	I/O port pins
P10–P13	80–83	I/O	I/O port pins
R00	84	O	Output port pin
R01	85	O	Output port pin
R02	86	O	Output port or TOUT output pin (selected by software)
R03	87	O	Output port or FOUT output pin (selected by software)
R10–R13	88–91	O	Output port pins
COM0–COM7	123, 1–3, 63–66	O	LCD common output pin (1/4, 1/5 or 1/8 duty is selectable by software)
SEG0–SEG55	95–122, 35–62	O	LCD segment output pin
SEN0	17	O	R/f converter Ch. 0 CR oscillation output pin
SEN1	19	O	R/f converter Ch. 1 CR oscillation output pin
REF0	16	O	R/f converter Ch. 0 reference resistor CR oscillation output pin
REF1	18	O	R/f converter Ch. 1 reference resistor CR oscillation output pin
HUD	20	O	R/f converter AC-bias oscillation output pin for humidity sensor
RFIN0	14	I	R/f converter Ch. 0 CR oscillation input pin
RFIN1	15	I	R/f converter Ch. 1 CR oscillation input pin
RFOUT	13	O	R/f converter oscillation frequency output pin
BZ	92	O	Sound output pin
BZ	93	O	Sound inverted output pin
RESET	34	I	Initial reset input pin
TEST	33	I	Testing input pin

## 1.5 Mask Option

---

Mask options shown below are provided for the S1C63657. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog and segment option generator winsog, that have been prepared as the development software tool of S1C63657, are used for this selection. Mask pattern of the IC is finally generated based on the data created by winfog and winsog. Refer to the "S5U1C63000A Manual" for winfog and winsog.

### <Outline of the mask option>

#### (1) *OSC1 oscillation circuit*

The OSC1 oscillation circuit is fixed at crystal oscillation. Refer to Section 4.4.2, "OSC1 oscillation circuit", for details.

#### (2) *OSC3 oscillation circuit*

The OSC3 oscillator type can be selected from ceramic oscillation, CR oscillation (external R) and CR oscillation (built-in R). Refer to Section 4.4.3, "OSC3 oscillation circuit", for details.

#### (3) *Input port pull-down resistor*

The mask option is used to select whether the pull-down resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports.  
Refer to Section 4.5.3, "Mask option", for details.

#### (4) *RESET terminal pull-down resistor*

This option is used to select whether the pull-down resistor is supplemented to the RESET terminal or not. Refer to Section 2.2.1, "Reset terminal (RESET)", for details.

#### (5) *I/O port pull-down resistor*

The mask option is used to select whether the pull-down resistor working in the input mode is supplemented to the I/O ports or not. It is possible to select for each bit of the input ports.  
Refer to Section 4.7.2, "Mask option", for details.

#### (6) *Output specification of the output port*

Either complementary output or P-channel open drain output can be selected as the output specification for the output ports R00–R03 and R10–R13. The selection is done in 1-bit units.  
Refer to Section 4.6.2, "Mask option", for details.

#### (7) *Output specification of the I/O port*

For the output specification when the I/O ports P00–P03 and P10–P13 are in the output mode, either complementary output or P-channel open drain output can be selected in 1-bit units.  
Refer to Section 4.7.2, "Mask option", for details.

#### (8) *External reset by simultaneous high input to the input port (K00–K03)*

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected.  
Refer to Section 2.2.2, "Simultaneous high input to terminals K00–K03", for details.

**(9) Time authorize circuit for the simultaneous high input reset function**

When the external reset function (shown in 8 above) is used, the time authorize circuit is enabled. The reset function works only when the input time of simultaneous low is more than the rule time if the time authorize circuit is being used. When the external reset function is not used, the time authorize circuit cannot be used. Refer to Section 2.2.2, "Simultaneous high input to terminals K00–K03", for details.

**(10) LCD drive power**

Either the internal power supply or an external power supply can be selected for driving LCD. Refer to Section 4.8.2, "Power supply for LCD driving", for details.

**(11) LCD segment specification**

The display memory can be allocated to the optional SEG terminal. It is also possible to set the optional SEG terminal for DC output.

Refer to Section 4.8.5, "Segment option", for details.

**<Option list>**

The following is the option list for the S1C63657.

Multiple selections are available in each option item as indicated in the option list. Select the specifications that meet the target system and check the appropriate box. Be sure to record the specifications for unused functions too.

**1. OSC1 SYSTEM CLOCK**

- ☐ 1. Crystal

**2. OSC3 SYSTEM CLOCK**

- ☐ 1. CR (built-in R)  
☐ 2. CR (external R)  
☐ 3. Ceramic

**3. INPUT PORT PULL DOWN RESISTOR**

- |       |   |   |
|-------|---|---|
| • K00 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K01 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K02 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K03 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K10 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K11 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K12 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • K13 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |

**4. RESET PORT PULL DOWN RESISTOR**

- RESET ☐ 1. With Resistor ☐ 2. Gate Direct

**5. I/O PORT PULL DOWN RESISTOR**

- |       |   |   |
|-------|---|---|
| • P00 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P01 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P02 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P03 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P10 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P11 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P12 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |
| • P13 | <input type="checkbox"/> 1. With Resistor | <input type="checkbox"/> 2. Gate Direct |

**6. OUTPUT PORT OUTPUT SPECIFICATION**

- |       |   |   |
|-------|---|---|
| • R00 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R01 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R02 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R03 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R10 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R11 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R12 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • R13 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |

**7. I/O PORT OUTPUT SPECIFICATION**

- |       |   |   |
|-------|---|---|
| • P00 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P01 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P02 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P03 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P10 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P11 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P12 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |
| • P13 | <input type="checkbox"/> 1. Complementary | <input type="checkbox"/> 2. Pch-OpenDrain |

**8. MULTIPLE KEY ENTRY RESET COMBINATION**

- ☐ 1. Not Use
- ☐ 2. Use (K00, K01)
- ☐ 3. Use (K00, K01, K02)
- ☐ 4. Use (K00, K01, K02, K03)

**9. MULTIPLE KEY ENTRY RESET TIME AUTHORIZE**

- ☐ 1. Not Use
- ☐ 2. Use

**10. LCD DRIVING POWER**

- ☐ 1. Internal Power (3.0 V panel)
- ☐ 2. External Power 1/3 bias,  $V_{DD}=V_{C2}$  (4.5 V panel)
- ☐ 3. External Power 1/3 bias,  $V_{DD}=V_{C3}$  (3.0 V panel)
- ☐ 4. External Power 1/2 bias,  $V_{DD}=V_{C3}$ ,  $V_{C1}=V_{C2}$  (3.0 V panel)



## 11. SEGMENT OPTION

Pin name	Address (F0xx)																					Output specification			
	COM0			COM1			COM2			COM3			COM4			COM5			COM6				COM7		
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D		H	L	D
SEG0																									SEG output <input type="checkbox"/> S
SEG1																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG2																									SEG output <input type="checkbox"/> S
SEG3																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG4																									SEG output <input type="checkbox"/> S
SEG5																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG6																									SEG output <input type="checkbox"/> S
SEG7																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG8																									SEG output <input type="checkbox"/> S
SEG9																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG10																									SEG output <input type="checkbox"/> S
SEG11																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG12																									SEG output <input type="checkbox"/> S
SEG13																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG14																									SEG output <input type="checkbox"/> S
SEG15																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG16																									SEG output <input type="checkbox"/> S
SEG17																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG18																									SEG output <input type="checkbox"/> S
SEG19																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG20																									SEG output <input type="checkbox"/> S
SEG21																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG22																									SEG output <input type="checkbox"/> S
SEG23																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG24																									SEG output <input type="checkbox"/> S
SEG25																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG26																									SEG output <input type="checkbox"/> S
SEG27																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG28																									SEG output <input type="checkbox"/> S
SEG29																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG30																									SEG output <input type="checkbox"/> S
SEG31																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG32																									SEG output <input type="checkbox"/> S
SEG33																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG34																									SEG output <input type="checkbox"/> S
SEG35																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG36																									SEG output <input type="checkbox"/> S
SEG37																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG38																									SEG output <input type="checkbox"/> S
SEG39																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG40																									SEG output <input type="checkbox"/> S
SEG41																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG42																									SEG output <input type="checkbox"/> S
SEG43																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG44																									SEG output <input type="checkbox"/> S
SEG45																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG46																									SEG output <input type="checkbox"/> S
SEG47																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG48																									SEG output <input type="checkbox"/> S
SEG49																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG50																									SEG output <input type="checkbox"/> S
SEG51																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG52																									SEG output <input type="checkbox"/> S
SEG53																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
SEG54																									SEG output <input type="checkbox"/> S
SEG55																									DC output <input type="checkbox"/> C <input type="checkbox"/> N
<address> H: RAM data high-order address (0–9) L: RAM data low-order address (0–F) D: Data bit (0–3)  <Output specification> S: Segment output C: Complementary output N: Nch open drain output																									

# CHAPTER 2 POWER SUPPLY AND INITIAL RESET

## 2.1 Power Supply

The S1C63657 operating power voltage is as follows:

Table 2.1.1 Operating voltage

Operating mode	Maximum operating frequency	Operating voltage
Normal mode	4 MHz (OSC3)	2.4 V to 3.6 V
Halver mode	32 kHz (OSC1 only)	2.4 V to 3.6 V
Normal mode	32 kHz (OSC1 only)	1.8 V to 3.6 V

The S1C63657 operates by applying a single power supply within the above range between VDD and VSS. The S1C63657 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.2.

Table 2.1.2 Power supply circuits

Circuit	Power supply	Output voltage
OSC1 circuit	Voltage regulator for OSC1 oscillation circuit	VOSC
Internal circuits (low-speed operation)	Low-speed operation voltage regulator	VD1L
OSC3 and internal circuits (high-speed operation)	High-speed operation voltage regulator	VD3
LCD driver	LCD system voltage circuit	VC1–VC3

Note: • Do not drive external loads with the output voltage from the internal power supply circuits.  
• See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.

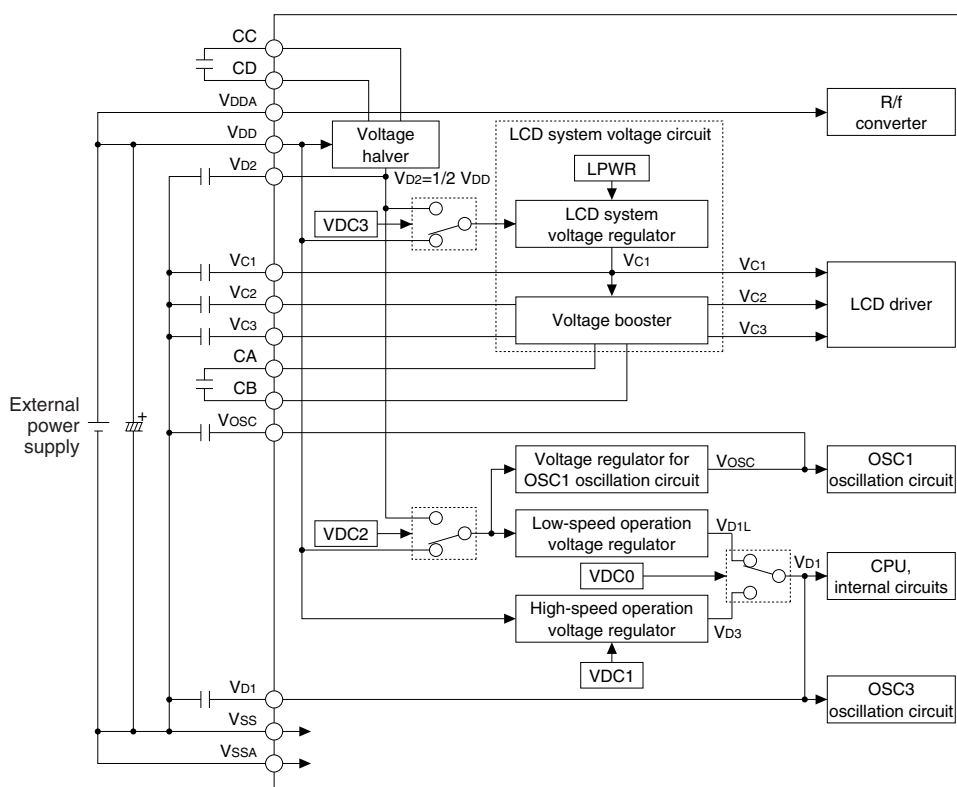


Fig. 2.1.1 Configuration of power supply

### ***2.1.1 Voltage regulator for OSC1 oscillation circuit***

This voltage regulator generates the VOSC voltage (0.98 V Typ.) for driving the OSC1 oscillation circuit. This regulator always operates to drive the OSC1 oscillation circuit.

### ***2.1.2 Low-speed operation voltage regulator***

The low-speed operation voltage regulator generates the VD1L voltage (1.25 V Typ.) for driving the internal logic circuits in low-speed mode. This regulator always operates and the output voltage is used as the operating voltage of the CPU and internal logic circuits when they are driven with the OSC1 clock (32 kHz).

### ***2.1.3 High-speed operation voltage regulator***

The high-speed operation voltage regulator generates the VD3 voltage (2.0 V Typ.) for driving the OSC3 oscillation circuit and the internal logic circuits in high-speed mode. Since this regulator stops normally, it should be turned it on using software before switching to the high-speed mode. Refer to Section 4.4, "Oscillation Circuit", for the control method.

### ***2.1.4 Internal operating voltage VD1***

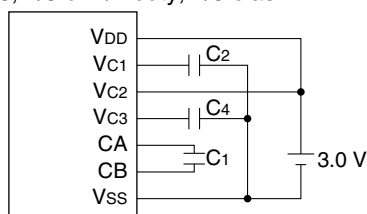
The internal operating voltage VD1 is the voltage for driving the CPU and internal logic circuits. The S1C63657 is designed with twin clock specifications; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch to OSC3 using software when high-speed operation is necessary. When switching the clock, the operating voltage VD1 must be switched using software to stabilize the operation of the oscillation circuit and internal circuits. In low-speed operation, VD1L generated by the low-speed operation voltage regulator is used as VD1. In high-speed operation, VD3 generated by the high-speed operation voltage regulator is used as VD1. Refer to Section 4.4, "Oscillation Circuit", for the control method.

### ***2.1.5 LCD system voltage circuit***

The LCD system voltage circuit generates the LCD drive voltage. This circuit allows the software to turn on and off. Turn this circuit on before starting display on the LCD. The LCD system voltage circuit generates VC1 with the voltage regulator built-in, and generates two other voltages ( $VC2 = 2VC1$ ,  $VC3 = 3VC1$ ) by boosting VC1. The VC1 voltage value can be adjusted using software in 16 steps (0.95 to 1.40 V). The LCD system voltage regulator can be disabled by mask option. In this case, external elements can be minimized because the external capacitors for the LCD system voltage regulator are not necessary. However when the LCD system voltage regulator is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system voltage regulator is used. Figure 2.1.5.1 shows the external element configuration when the LCD system voltage regulator is not used.

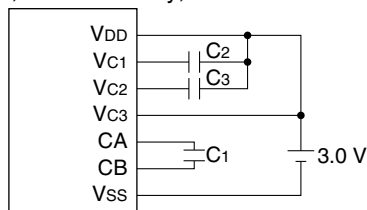
4.5 V LCD panel

1/8, 1/5 or 1/4 duty, 1/3 bias



3 V LCD panel

1/8, 1/5 or 1/4 duty, 1/3 bias



3 V LCD panel

1/8, 1/5 or 1/4 duty, 1/2 bias

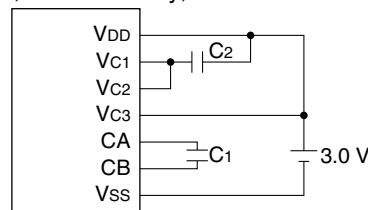


Fig. 2.1.5.1 External elements when LCD system voltage regulator is not used

Refer to Section 4.8, "LCD Driver", for control of the LCD drive voltage.

### 2.1.6 Halver mode and saving power

When the supply voltage  $V_{DD}$  is 2.4 V or more, the low-speed operation voltage regulator and LCD system voltage circuit can be driven with the  $V_{DD}$  voltage halved. This status is the halver mode for reducing current consumption during HALT or low-speed operation. At initial reset, the low-speed operation voltage regulator and LCD system voltage circuit are set in the normal mode using  $V_{DD}$ . When necessary switch to the halver mode using software. The halver mode supports only low-speed operation using the OSC1 clock and cannot be set during high-speed operation using the OSC3 clock. The low-speed operation voltage regulator and the LCD system voltage circuit can be set to the halver mode independently. Refer to Section 4.2, "Power Control", for control of the halver mode.

### 2.1.7 Analog system power supply

The  $V_{DDA}$  and  $V_{SSA}$  power supply terminals are provided only for the R/f converter in order to avoid decreasing the conversion accuracy due to noise. However, the same voltage level as the  $V_{DD}$ – $V_{SS}$  must be supplied to the  $V_{DDA}$ – $V_{SSA}$ .

$V_{DDA} = V_{DD}$ ,  $V_{SSA} = V_{SS}$

## 2.2 Initial Reset

To initialize the S1C63657 circuits, initial reset must be executed. There are two ways of doing this.

- (1) External initial reset by the RESET terminal
- (2) External initial reset by simultaneous high input to terminals K00–K03 (mask option setting)

The circuits are initialized by either (1) or (2). When the power is turned on, be sure to initialize using the reset function. It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

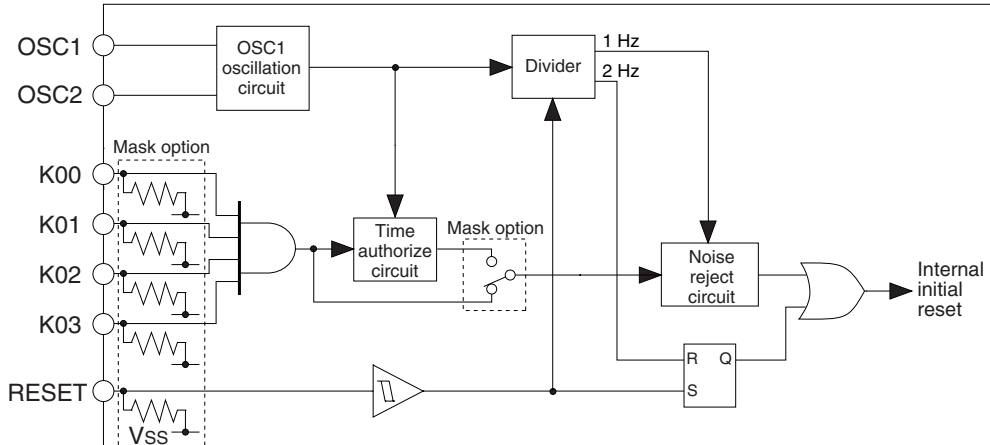


Fig. 2.2.1 Configuration of initial reset circuit

### 2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level ( $V_{DD}$ ). After that the initial reset is released by setting the reset terminal to a low level ( $V_{SS}$ ) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when  $f_{OSC1} = 32.768$  kHz) is needed until the internal initial reset is released after the reset terminal goes to low level. Be sure to maintain a reset input of 0.1 msec or more. However, when turning the power on, the reset terminal should be set at a high level as in the timing shown in Figure 2.2.1.1.

Note that a reset pulse shorter than 100 nsec is rejected as noise.

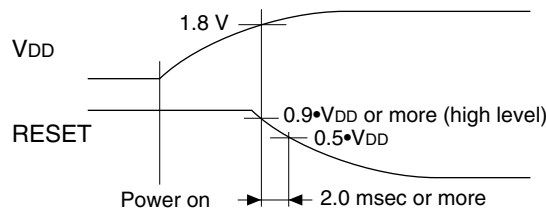


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to  $0.9 \cdot V_{DD}$  or more (high level) until the supply voltage becomes 1.8 V or more.

After that, a level of  $0.5 \cdot V_{DD}$  or more should be maintained more than 2.0 msec.

The reset terminal incorporates a pull-down resistor and a mask option is provided to select whether the resistor is used or not.

## 2.2.2 Simultaneous high input to terminals K00–K03

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option.

Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency  $f_{OSC1}$  is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency  $f_{OSC1}$  is 32.768 kHz) after oscillation starts.

Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00*K01
3	K00*K01*K02
4	K00*K01*K02*K03

When, for instance, mask option 4 (K00\*K01\*K02\*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time. When 2 or 3 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.

Further, the time authorize circuit mask option is selected when this reset function is selected. The time authorize circuit checks the input time of the simultaneous high input and performs initial reset if that time is the defined time (1 to 2 sec) or more.

If using this function, make sure that the specified ports do not go high at the same time during ordinary operation.

## 2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.3.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.

In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.

Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.3.1 Initial values

CPU core				Peripheral circuits		
Name	Symbol	Number of bits	Setting value	Name	Number of bits	Setting value
Data register A	A	4	Undefined	RAM	4	Undefined
Data register B	B	4	Undefined	Display memory	4	Undefined
Extension register EXT	EXT	8	Undefined	Other peripheral circuits	–	*
Index register X	X	16	Undefined			
Index register Y	Y	16	Undefined			
Program counter	PC	16	0110H			
Stack pointer SP1	SP1	8	Undefined			
Stack pointer SP2	SP2	8	Undefined			
Zero flag	Z	1	Undefined			
Carry flag	C	1	Undefined			
Interrupt flag	I	1	0			
Extension flag	E	1	0			
Queue register	Q	16	Undefined			

\* See Section 4.1, "Memory Map".

### 2.2.4 Terminal settings at initial resetting

The output port (R) terminals are shared with special output terminals. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.

Table 2.2.4.1 shows the list of the shared terminal settings.

*Table 2.2.4.1 List of shared terminal settings*

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (LOW output)		
R01	R01 (LOW output)		
R02	R02 (LOW output)	TOUT	
R03	R03 (LOW output)		FOUT
R10–R13	R10–R13 (LOW output)		

For setting procedure of the functions, see explanations for each of the peripheral circuits.

## 2.3 Test Terminal (TEST)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the TEST terminal to Vss.

# CHAPTER 3 CPU, ROM, RAM

## 3.1 CPU

The S1C63657 has a 4-bit core CPU S1C63000 built-in as its CPU part. Refer to the "S1C63000 Core CPU Manual" for the S1C63000.

*Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the S1C63657.*

## 3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 8,192 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C63657 is step 0000H to step 1FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

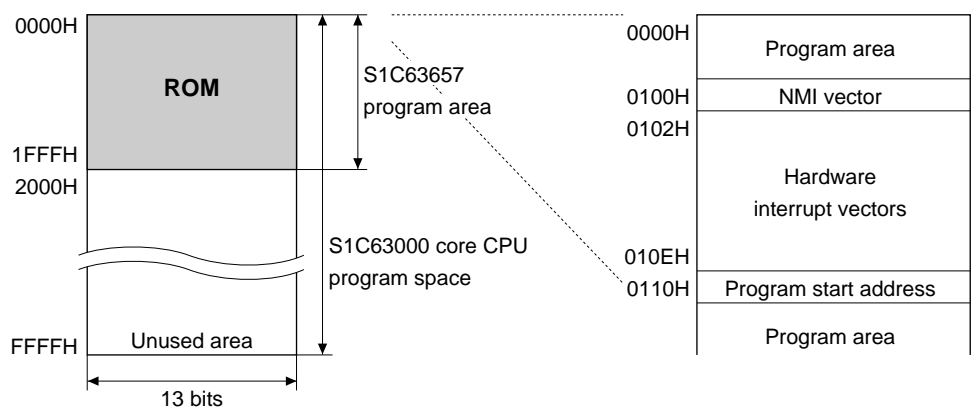


Fig. 3.2.1 Configuration of code ROM

## 3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 1,024 words × 4 bits. The RAM area is assigned to addresses 0000H to 03FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

- (1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.
- (2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).

16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63657 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.

After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.



- (3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

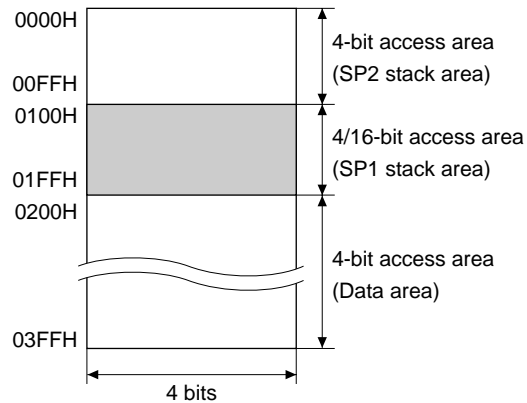


Fig. 3.3.1 Configuration of data RAM

### 3.4 Data ROM

The data ROM is a mask ROM for loading various static data such as a character generator, and has a capacity of 2,048 words  $\times$  4 bits. The data ROM is assigned to addresses 8000H to 87FFH on the data memory map, and the data can be read using the same data memory access instructions as the RAM.

# CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of S1C63657 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

## 4.1 Memory Map

The S1C63657 data memory consists of 1,024-word RAM, 2,048-word data ROM, 160-word display memory and 84-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the S1C63657, and Table 4.1.1 the peripheral circuits' (I/O space) memory maps.

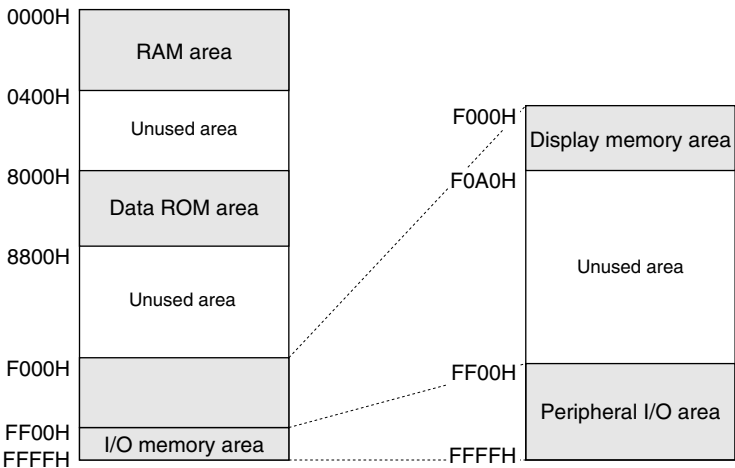


Fig. 4.1.1 Memory map

*Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.*

Table 4.1.1 (a) I/O memory map (FF00H–FF33H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	VDC3	VDC2	VDC1	VDC0	VDC3	0	1/2V <sub>DD</sub>	V <sub>DD</sub>	LCD system voltage regulator power source switch
					VDC2	0	1/2V <sub>DD</sub>	V <sub>DD</sub>	Low-speed operation voltage regulator power source switch
					VDC1	0	On	Off	High-speed operation voltage regulator on/off
					VDC0	0	V <sub>D3</sub>	V <sub>D1L</sub>	Logic system power source switch
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
					0 *3	–*2			Unused
					0 *3	–*2			Unused
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					SWDIR	0	1	0	General-purpose register
					FOFQ1	0			FOUT frequency selection [FOFQ1, 0]      0      1      2      3 Frequency      fosc1/64      fosc1/8      fosc1      fosc3
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	–*2			Unused
					0 *3	–*2			Unused
					WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	–*2	High	Low	K00–K03 input port data
					K02	–*2	High	Low	
					K01	–*2	High	Low	
					K00	–*2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
					KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
					SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	–*2	High	Low	K10–K13 input port data
					K12	–*2	High	Low	
					K11	–*2	High	Low	
					K10	–*2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
					KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	Hi-Z	Output	R03 (FOUTE=0)/FOUT (FOUTE=1) Hi-Z control
					R02HIZ	0	Hi-Z	Output	R02 (PTOUT=0)/TOUT (PTOUT=1) Hi-Z control
					R01HIZ	0	Hi-Z	Output	R01 Hi-Z control
					R00HIZ	0	Hi-Z	Output	R00 Hi-Z control
FF31H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used.
					R02	0	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used.
					R01	0	High	Low	R01 output port data
					R00	0	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	–*2			Unused
					0 *3	–*2			Unused
					0 *3	–*2			Unused
					R1HIZ	0	Hi-Z	Output	R10–R13 Hi-Z control
FF33H	R13	R12	R11	R10	R13	0	High	Low	R10–R13 output port data
					R12	0	High	Low	
					R11	0	High	Low	
					R10	0	High	Low	

**Remarks**

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF40H–FF74H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
					IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
					PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	–*2	High	Low	P00–P03 I/O port data
					P02	–*2	High	Low	
					P01	–*2	High	Low	
					P00	–*2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P10–P13 I/O control register
					IOC12	0	Output	Input	
					IOC11	0	Output	Input	
					IOC10	0	Output	Input	
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P10–P13 pull-down control register
					PUL12	1	On	Off	
					PUL11	1	On	Off	
					PUL10	1	On	Off	
FF46H	P13	P12	P11	P10	P13	–*2	High	Low	P10–P13 I/O port data
					P12	–*2	High	Low	
					P11	–*2	High	Low	
					P10	–*2	High	Low	
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 Duty 1/4 1/5 1/8
					LDUTY0	0			
					STCD	0	Static	Dynamic	
					LPWR	0	On	Off	
FF61H	0	ALOFF	ALON	0	0 *3	–*2			Unused LCD all Off control LCD all On control Unused
					ALOFF	1	All Off	Normal	
					ALON	0	All On	Normal	
					0 *3	–*2			
FF62H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment [LC3–0] 0 – 15 Contrast Light – Dark
					LC2	0			
					LC1	0			
					LC0	0			
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection Envelope reset (writing) Envelope On/Off Buzzer output enable
					ENRST*3	Reset	Reset	Invalid	
					ENON	0	On	Off	
					BZE	0	Enable	Disable	
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	–*2			Unused 1-shot buzzer stop (writing) 1-shot buzzer trigger (writing) 1-shot buzzer status (reading) 1-shot buzzer pulse width setting
					BZSTP*3	0	Stop	Invalid	
					BZSHT	0	Trigger	Invalid	
					SHTPW	0	Busy	Ready	
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	–*2			Unused Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3 Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 [BZFQ2, 1, 0] 4 5 6 7 Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
					BZFQ2	0			
					BZFQ1	0			
					BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	–*2			Unused Buzzer signal duty ratio selection (refer to main manual)
					BDTY2	0			
					BDTY1	0			
					BDTY0	0			
FF74H	0	0	TMRST	TMRUN	0 *3	–*2			Unused Unused Clock timer reset (writing) Clock timer Run/Stop
					0 *3	–*2			
					TMRST*3	Reset	Reset	Invalid	
					TMRUN	0	Run	Stop	

Table 4.1.1 (c) I/O memory map (FF75H–FF94H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF75H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF76H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FF80H	SR3	SR2	SR1	SR0	SR3	–*2			Source register (low-order 4 bits) LSB
					SR2	–*2			
	R/W				SR1	–*2			
					SR0	–*2			
FF81H	SR7	SR6	SR5	SR4	SR7	–*2			MSB Source register (high-order 4 bits)
					SR6	–*2			
	R/W				SR5	–*2			
					SR4	–*2			
FF82H	DRL3	DRL2	DRL1	DRL0	DRL3	–*2			Low-order 8-bit destination register (low-order 4 bits) LSB
					DRL2	–*2			
	R/W				DRL1	–*2			
					DRL0	–*2			
FF83H	DRL7	DRL6	DRL5	DRL4	DRL7	–*2			MSB Low-order 8-bit destination register (high-order 4 bits)
					DRL6	–*2			
	R/W				DRL5	–*2			
					DRL4	–*2			
FF84H	DRH3	DRH2	DRH1	DRH0	DRH3	–*2			High-order 8-bit destination register (low-order 4 bits) LSB
					DRH2	–*2			
	R/W				DRH1	–*2			
					DRH0	–*2			
FF85H	DRH7	DRH6	DRH5	DRH4	DRH7	–*2			MSB High-order 8-bit destination register (high-order 4 bits)
					DRH6	–*2			
	R/W				DRH5	–*2			
					DRH4	–*2			
FF86H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
					ZF	0	Zero	No	Zero flag
	R			R/W	CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)
FF90H	0	RFCLK	RFSEL	SENSEL	0 *3	–*2			Unused
					RFCLK	0	OSC3	OSC1	R/f conversion clock selection
					RFSEL	0	AC	DC	Ch.1 sensor type selection
	R	R/W			SENSEL	0	Ch.1	Ch.0	Conversion channel selection
FF91H	OVTBC	OVMC	RFRUNR	RFRUNS	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag
	R/W				RFRUNR	0	Run	Stop	Reference oscillation Run control/status (writing "0" is ineffective)
					RFRUNS	0	Run	Stop	Sensor oscillation Run control/status (writing "0" is ineffective)
FF92H	MC3	MC2	MC1	MC0	MC3	–*2			Measurement counter MC0–MC3 LSB
					MC2	–*2			
	R/W				MC1	–*2			
					MC0	–*2			
FF93H	MC7	MC6	MC5	MC4	MC7	–*2			Measurement counter MC4–MC7
					MC6	–*2			
	R/W				MC5	–*2			
					MC4	–*2			
FF94H	MC11	MC10	MC9	MC8	MC11	–*2			Measurement counter MC8–MC11
					MC10	–*2			
	R/W				MC9	–*2			
					MC8	–*2			

Table 4.1.1 (d) I/O memory map (FF95H–FFC6H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF95H	MC15	MC14	MC13	MC12	MC15	–*2			Measurement counter MC12–MC15
					MC14	–*2			
					MC13	–*2			
	R/W				MC12	–*2			
FF96H	MC19	MC18	MC17	MC16	MC19	–*2			MSB Measurement counter MC16–MC19
					MC18	–*2			
					MC17	–*2			
	R/W				MC16	–*2			
FF97H	TC3	TC2	TC1	TC0	TC3	–*2			Time base counter TC0–TC3 LSB
					TC2	–*2			
					TC1	–*2			
	R/W				TC0	–*2			
FF98H	TC7	TC6	TC5	TC4	TC7	–*2			Time base counter TC4–TC7
					TC6	–*2			
					TC5	–*2			
	R/W				TC4	–*2			
FF99H	TC11	TC10	TC9	TC8	TC11	–*2			Time base counter TC8–TC11
					TC10	–*2			
					TC9	–*2			
	R/W				TC8	–*2			
FF9AH	TC15	TC14	TC13	TC12	TC15	–*2			Time base counter TC12–TC15
					TC14	–*2			
					TC13	–*2			
	R/W				TC12	–*2			
FF9BH	TC19	TC18	TC17	TC16	TC19	–*2			MSB Time base counter TC16–TC19
					TC18	–*2			
					TC17	–*2			
	R/W				TC16	–*2			
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
					FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
	R/W				PLPOL	0	⌵	⌶	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	0	CHSEL1	CHSEL0	PTOUT	0 *3	–*2			Unused
					CHSEL1	0			TOUT output selection TOUT output control
					CHSEL0	0			
	R	R/W			PTOUT	0	On	Off	
FFC2H	0	CKSEL2	CKSEL1	CKSEL0	0 *3	–*2			Unused
					CKSEL2	0	OSC3	OSC1	Prescaler 2 source clock selection
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
	R	R/W			CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC3H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection Timer 0 reset (reload) Timer 0 Run/Stop
					PTPS00	0			
					PTRST0*3	–*2	Reset	Invalid	
	R/W		W	R/W	PTRUN0	0	Run	Stop	
FFC4H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection Timer 1 reset (reload) Timer 1 Run/Stop
					PTPS10	0			
					PTRST1*3	–*2	Reset	Invalid	
	R/W		W	R/W	PTRUN1	0	Run	Stop	
FFC5H	PTPS21	PTPS20	PTRST2	PTRUN2	PTPS21	0			Prescaler 2 division ratio selection Timer 2 reset (reload) Timer 2 Run/Stop
					PTPS20	0			
					PTRST2*3	–*2	Reset	Invalid	
	R/W		W	R/W	PTRUN2	0	Run	Stop	
FFC6H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB Programmable timer 0 reload data (low-order 4 bits) LSB
					RLD02	0			
					RLD01	0			
	R/W				RLD00	0			

Table 4.1.1 (e) I/O memory map (FFC7H–FFD4H)

Address	Register				Comment				
	D3	D2	D1	D0	Name	Init *1	1	0	
FFC7H	RLD07	RLD06	RLD05	RLD04	RLD07	0			] MSB Programmable timer 0 reload data (high-order 4 bits) LSB
					RLD06	0			
	R/W				RLD05	0			
					RLD04	0			
FFC8H	RLD13	RLD12	RLD11	RLD10	RLD13	0			] MSB Programmable timer 1 reload data (low-order 4 bits) LSB
					RLD12	0			
	R/W				RLD11	0			
					RLD10	0			
FFC9H	RLD17	RLD16	RLD15	RLD14	RLD17	0			] MSB Programmable timer 1 reload data (high-order 4 bits) LSB
					RLD16	0			
	R/W				RLD15	0			
					RLD14	0			
FFCAH	RLD23	RLD22	RLD21	RLD20	RLD23	0			] MSB Programmable timer 2 reload data (low-order 4 bits) LSB
					RLD22	0			
	R/W				RLD21	0			
					RLD20	0			
FFCBH	RLD27	RLD26	RLD25	RLD24	RLD27	0			] MSB Programmable timer 2 reload data (high-order 4 bits) LSB
					RLD26	0			
	R/W				RLD25	0			
					RLD24	0			
FFCCH	PTD03	PTD02	PTD01	PTD00	PTD03	0			] MSB Programmable timer 0 data (low-order 4 bits) LSB
					PTD02	0			
	R				PTD01	0			
					PTD00	0			
FFCDH	PTD07	PTD06	PTD05	PTD04	PTD07	0			] MSB Programmable timer 0 data (high-order 4 bits) LSB
					PTD06	0			
	R				PTD05	0			
					PTD04	0			
FFCEH	PTD13	PTD12	PTD11	PTD10	PTD13	0			] MSB Programmable timer 1 data (low-order 4 bits) LSB
					PTD12	0			
	R				PTD11	0			
					PTD10	0			
FFCFH	PTD17	PTD16	PTD15	PTD14	PTD17	0			] MSB Programmable timer 1 data (high-order 4 bits) LSB
					PTD16	0			
	R				PTD15	0			
					PTD14	0			
FFD0H	PTD23	PTD22	PTD21	PTD20	PTD23	0			] MSB Programmable timer 2 data (low-order 4 bits) LSB
					PTD22	0			
	R				PTD21	0			
					PTD20	0			
FFD1H	PTD27	PTD26	PTD25	PTD24	PTD27	0			] MSB Programmable timer 2 data (high-order 4 bits) LSB
					PTD26	0			
	R				PTD25	0			
					PTD24	0			
FFD2H	CD03	CD02	CD01	CD00	CD03	0			] MSB Programmable timer 0 compare data (low-order 4 bits) LSB
					CD02	0			
	R/W				CD01	0			
					CD00	0			
FFD3H	CD07	CD06	CD05	CD04	CD07	0			] MSB Programmable timer 0 compare data (high-order 4 bits) LSB
					CD06	0			
	R/W				CD05	0			
					CD04	0			
FFD4H	CD13	CD12	CD11	CD10	CD13	0			] MSB Programmable timer 1 compare data (low-order 4 bits) LSB
					CD12	0			
	R/W				CD11	0			
					CD10	0			

Table 4.1.1 (f) I/O memory map (FFD5H–FFF7H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFD5H	CD17	CD16	CD15	CD14	CD17	0			MSB Programmable timer 1 compare data (high-order 4 bits) LSB
					CD16	0			
					CD15	0			
					CD14	0			
FFD8H	0	0	PTSEL1	PTSEL0	0 *3	– *2			Unused Unused Programmable timer 1 PWM output selection Programmable timer 0 PWM output selection
					0 *3	– *2			
					PTSEL1	0	PWM	Normal	
					PTSEL0	0	PWM	Normal	
FFE0H	0	0	ECTC1	ECTC0	0 *3	– *2			Unused Unused Interrupt mask register (Programmable timer 1 compare match) Interrupt mask register (Programmable timer 0 compare match)
					0 *3	– *2			
					ECTC1	0	Enable	Mask	
					ECTC0	0	Enable	Mask	
FFE1H	0	EIPT2	EIPT1	EIPT0	0 *3	– *2			Unused Interrupt mask register (Programmable timer 2 underflow) Interrupt mask register (Programmable timer 1 underflow) Interrupt mask register (Programmable timer 0 underflow)
					EIPT2	0	Enable	Mask	
					EIPT1	0	Enable	Mask	
					EIPT0	0	Enable	Mask	
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused Unused Unused Interrupt mask register (K00–K03)
					0 *3	– *2			
					0 *3	– *2			
					EIK0	0	Enable	Mask	
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused Unused Unused Interrupt mask register (K10–K13)
					0 *3	– *2			
					0 *3	– *2			
					EIK1	0	Enable	Mask	
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE7H	0	0	EIRFB	EIRFM	0 *3	– *2			Unused Unused Interrupt mask register (R/f converter reference oscillate completion) Interrupt mask register (R/f converter sensor oscillate completion)
					0 *3	– *2			
					EIRFB	0	Enable	Mask	
					EIRFM	0	Enable	Mask	
FFF0H	0	0	ICTC1	ICTC0	0 *3	– *2	(R)	(R)	Unused Unused Interrupt factor flag (Programmable timer 1 compare match) Interrupt factor flag (Programmable timer 0 compare match)
					0 *3	– *2	Yes	No	
					ICTC1	0	(W)	(W)	
					ICTC0	0	Reset	Invalid	
FFF1H	0	IPT2	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused Interrupt factor flag (Programmable timer 2 underflow) Interrupt factor flag (Programmable timer 1 underflow) Interrupt factor flag (Programmable timer 0 underflow)
					IPT2	0	Yes	No	
					IPT1	0	(W)	(W)	
					IPT0	0	Reset	Invalid	
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused Unused Unused Interrupt factor flag (K00–K03)
					0 *3	– *2	Yes	No	
					0 *3	– *2	(W)	(W)	
					IK0	0	Reset	Invalid	
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused Unused Unused Interrupt factor flag (K10–K13)
					0 *3	– *2	Yes	No	
					0 *3	– *2	(W)	(W)	
					IK1	0	Reset	Invalid	
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF7H	0	0	IRFB	IRFM	0 *3	– *2	(R)	(R)	Unused Unused Interrupt factor flag (R/f converter reference oscillate completion) Interrupt factor flag (R/f converter sensor oscillate completion)
					0 *3	– *2	Yes	No	
					IRFB	0	(W)	(W)	
					IRFM	0	Reset	Invalid	



## 4.2 Power Control

### 4.2.1 Configuration of power supply circuit

The S1C63657 has built-in power supply circuits shown in Figure 4.2.1.1 so the voltages to drive the CPU, internal logic circuits, oscillation circuits and LCD driver can be generated on the chip.

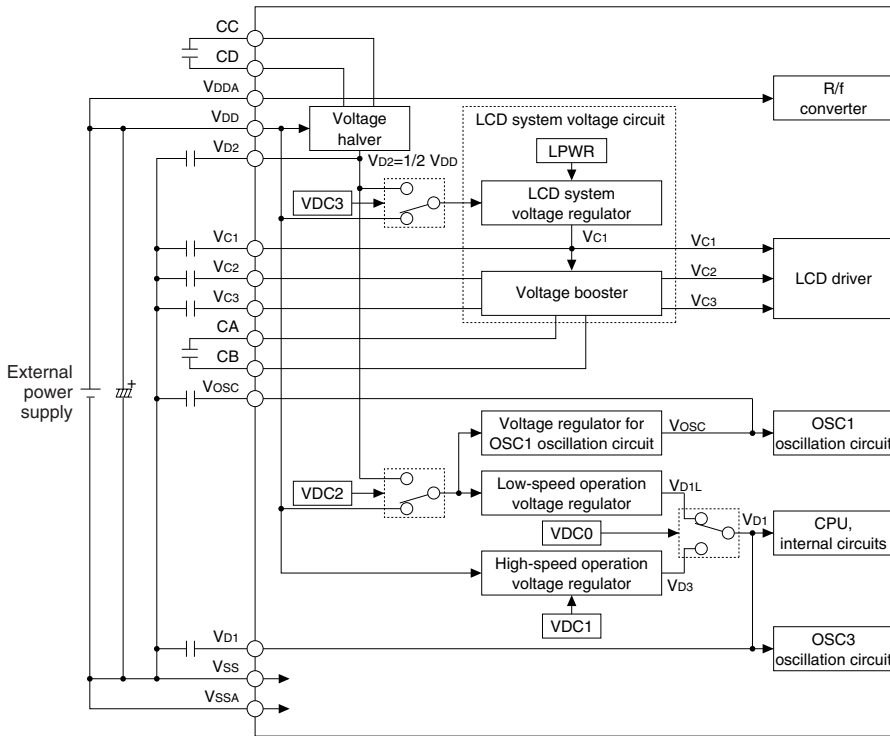


Fig. 4.2.1.1 Built-in power supply circuit

#### Voltage regulator for OSC1 oscillation circuit

This voltage regulator always operates to generate the Vosc voltage (0.98 V Typ.) for driving the OSC1 oscillation circuit.

#### Low-speed operation voltage regulator

The low-speed operation voltage regulator always operates to generate the Vd1L voltage (1.25 V Typ.) for driving the internal logic circuits. The Vd1L voltage is used as the Vd1 operating voltage of the CPU and internal logic circuits when they are driven with the OSC1 clock (32 kHz). Vd1 should be switched using software according to the operating clock.

#### High-speed operation voltage regulator

The high-speed operation voltage regulator generates the Vd3 voltage (2.0 V Typ.) for driving the OSC3 oscillation circuit and the internal logic circuits in high-speed mode. Since this regulator stops normally, turn it on using the VDC1 register (VDC1 = "1") and switch the internal logic operating voltage to Vd3 using the VDC0 register before starting the OSC3 oscillation.

#### LCD system voltage circuit

The LCD system voltage circuit generates the LCD drive voltage. This circuit can be turned on and off using the LPWR register. Turn this circuit on (LPWR = "1") before starting display on the LCD.

The LCD system voltage circuit generates VC1 with the built-in voltage regulator, and generates two other voltages (VC2 = 2VC1, VC3 = 3VC1) by boosting VC1. The VC1 voltage value can be adjusted using software in 16 steps (0.95 to 1.40 V). Refer to Section 4.8, "LCD Driver", for control of the VC1 voltage (contrast). This circuit does not operate when an external power supply is selected by mask option for driving the LCD.

## Voltage halver

The voltage halver generates  $V_{D2}$  by halving the supply voltage  $V_{DD}$ . Using this halved supply voltage to drive the low-speed operation voltage regulator and LCD system voltage circuit reduces current consumption during HALT or low-speed operation. This status is the halver mode and the VDC2 register is used to set the low-speed operation voltage regulator into the halver mode and the VDC3 register is used to set the LCD system voltage circuit. However, the supply voltage must be 2.4 V or more to set the halver mode. Furthermore, the halver mode cannot be set during high-speed operation using the OSC3 clock.

In the normal mode, the low-speed operation voltage regulator and LCD system voltage circuit operate with the supply voltage  $V_{DD}$  directly.

At initial reset, the normal mode is set by hardware.

The voltage halver always operates regardless of the mode set.

### 4.2.2 Power control procedure

At initial reset, the power supply, operating voltage and oscillation circuit are set as follows:

- Low-speed operation voltage regulator: ON  
Normal mode (VDC2 = "0")
- LCD system voltage circuit: OFF (LPWR = "0")  
Normal mode (VDC3 = "0")
- High-speed operation voltage regulator: OFF (VDC1 = "0")
- CPU/internal logic operating voltage:  $V_{D1L}$  (VDC0 = "0")
- CPU system clock: OSC1 (CLKCHG = "0")
- OSC3 oscillation circuit: OFF (OSCC = "0")

## Setting halver mode

The low-speed operation voltage regulator and the LCD system voltage circuit can be set into the halver mode independently.

### Setting the low-speed operation voltage regulator

The low-speed operation voltage regulator can be set into the halver mode under the conditions below.

- When the supply voltage  $V_{DD}$  is 2.4 V or higher.
- When the CPU/internal circuits operate with the  $V_{D1L}$  operating voltage and OSC1 operating clock.

The following shows the switching procedure from normal mode to halver mode.

1. Switch the CPU clock from OSC3 to OSC1 (CLKCHG = "0", when OSC3 is used as the CPU clock)
2. Stop the OSC3 oscillation (OSCC = "0")
3. Switch the internal operating voltage from  $V_{D3}$  to  $V_{D1L}$  (VDC0 = "0")
4. Turn the high-speed operation voltage circuit off (VDC1 = "0")
5. Set the halver mode (VDC2 = "1")

Steps 1 to 4 are necessary during high-speed operation.

### Setting the LCD system voltage circuit

The LCD system voltage circuit can be set into the halver mode under the conditions below.

- When the supply voltage  $V_{DD}$  is 2.4 V or higher.
- When the VC1 setup value for driving the LCD is 1.13 V or lower.

The following shows the switching procedure.

1. Set the LCD drive voltage VC1 to 1.13 V or lower ( $LC3-LC0 \leq 6$ )
2. Set the halver mode (VDC3 = "1")

## Switching to high-speed operation

The S1C63657 is designed with twin clock specifications; it has two types of oscillation circuits OSC1 (for low-speed operation) and OSC3 (for high-speed operation) built-in. Use OSC1 clock for normal operation, and switch it to OSC3 using software when high-speed operation is necessary. When switching the clock, the operating voltage  $V_{D1}$  must be switched using software to stabilize the operation of the oscillation circuit and internal circuits.

The following shows the switching procedure. Refer to Section 4.4, "Oscillation Circuit", for control of the oscillation circuit.

### Switching from low-speed operation to high-speed operation

1. Set VDC2 to "0". (low-speed operation voltage regulator: halver mode → normal mode)
2. Set VDC1 to "1". (high-speed operation voltage regulator: off → on)
3. Set VDC0 to "1". (internal logic operating voltage:  $V_{D1L}$  →  $V_{D3}$ )
4. Wait 2.5 msec or more.
5. Set OSCC to "1". (OSC3 oscillation: off → on)
6. Wait 5 msec or more.
7. Set CLKCHG to "1". (CPU clock: OSC1 → OSC3)

To switch from high-speed operation to low-speed operation, follow the procedure to set the halver mode (see the previous page).

## 4.2.3 I/O memory for power control

Table 4.2.3.1 shows the I/O address and the control bits for power control.

Table 4.2.3.1 Power control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	VDC3	VDC2	VDC1	VDC0	VDC3	0	1/2 $V_{DD}$	$V_{DD}$	LCD system voltage regulator power source switch
					VDC2	0	1/2 $V_{DD}$	$V_{DD}$	Low-speed operation voltage regulator power source switch
					VDC1	0	On	Off	High-speed operation voltage regulator on/off
					VDC0	0	$V_{D3}$	$V_{D1L}$	Logic system power source switch
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			LCD drive duty switch
					LDUTY0	0			
					STCD	0	Static	Dynamic	LCD drive switch
					LPWR	0	On	Off	LCD power On/Off

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

### VDC0: Internal logic system power switching register (FF00H•D0)

It is used to switch the operating voltage for the CPU and internal circuit.

When "1" is written:  $V_{D3}$  (for OSC3 operation)

When "0" is written:  $V_{D1L}$  (for OSC1 operation)

Reading: Valid

When "1" is written to VDC0, the internal operating voltage is switched to  $V_{D3}$ . After switching to  $V_{D3}$ , the OSC3 oscillation can be started.

When the low-speed operation voltage regulator is in the halver mode, return it to the normal mode before switching to  $V_{D3}$ .

When "0" is written to VDC0, the internal operating voltage is switched to  $V_{D1L}$ . Stop the OSC3 oscillation before switching to  $V_{D1L}$ .

At initial reset, this register is set to "0".

**VDC1: High-speed operation voltage regulator control (ON/OFF) register (FF00H•D1)**

Turns the high-speed operation voltage regulator on and off.

When "1" is written: On

When "0" is written: Off

Reading: Valid

When "1" is written to VDC1, the high-speed operation voltage regulator goes to generate the high-speed operation voltage  $V_{D3}$  for the internal logic circuits.

When "0" is written to VDC1, the high-speed operation voltage regulator stops operating. Do not write "0" to VDC1 while the CPU is operating with the OSC3 clock.

At initial reset, this register is set to "0".

**VDC2: Low-speed operation voltage regulator power control register (FF00H•D2)**

Sets the low-speed operation voltage regulator to the halver mode.

When "1" is written: Halver mode (driven with  $1/2 V_{DD}$ )

When "0" is written: Normal mode (driven with  $V_{DD}$ )

Reading: Valid

When "1" is written to VDC2, the low-speed operation voltage regulator enters the halver mode. In this mode, the low-speed operation voltage regulator operates with  $1/2$  the  $V_{DD}$  voltage, this makes it possible to reduce current consumption. However, the supply voltage  $V_{DD}$  must be 2.4 V or higher. Furthermore, this mode does not allow high-speed operation using the OSC3 clock.

When "0" is written to VDC2, the low-speed operation voltage regulator enters the normal mode and operates with the supply voltage  $V_{DD}$ .

At initial reset, the hardware sets the normal mode and this register is set to "0".

**VDC3: LCD system voltage circuit power control register (FF00H•D3)**

Sets the LCD system voltage circuit to the halver mode.

When "1" is written: Halver mode (driven with  $1/2 V_{DD}$ )

When "0" is written: Normal mode (driven with  $V_{DD}$ )

Reading: Valid

When "1" is written to VDC3, the LCD system voltage circuit enters the halver mode. In this mode, the LCD system voltage circuit operates with  $1/2$  the  $V_{DD}$  voltage, this makes it possible to reduce current consumption. However, the supply voltage  $V_{DD}$  must be 2.4 V or higher and the  $V_{C1}$  setup voltage must be 1.13 V or lower. Furthermore, this mode does not allow high-speed operation using the OSC3 clock.

When "0" is written to VDC3, the LCD system voltage circuit enters the normal mode and operates with the supply voltage  $V_{DD}$ .

At initial reset, the hardware sets the normal mode and this register is set to "0".

**LPWR: LCD power control (ON/OFF) register (FF60H•D0)**

Turns the LCD system voltage circuit on and off.

When "1" is written: On

When "0" is written: Off

Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes on and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to  $V_{SS}$  level.

It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.

At initial reset, this register is set to "0".

#### ***4.2.4 Programming notes***

- (1) When setting the low-speed operation voltage regulator to the halver mode, switch the CPU clock to OSC1 before writing "1" to VDC2.
- (2) When setting the LCD system voltage circuit to the halver mode, set the VC1 voltage (contrast) to 1.13 V or lower (LC register = 6 or less) before writing "1" to VDC3.

## 4.3 Watchdog Timer

### 4.3.1 Configuration of watchdog timer

The S1C63657 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.

Figure 4.3.1.1 is the block diagram of the watchdog timer.

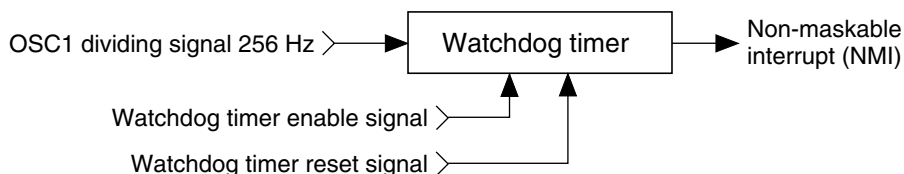


Fig. 4.3.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.

Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.

The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

### 4.3.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

### 4.3.3 I/O memory of watchdog timer

Table 4.3.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.3.3.1 Control bits of watchdog timer

Address	Register									Comment
	D3	D2	D1	D0	Name	Init *1	1	0		
FF07H	0	0	WDEN	WDRST	0 *3	— *2			Unused	
					0 *3	— *2			Unused	
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable	
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)	

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled

When "0" is written: Disabled

Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).

At initial reset, this register is set to "1".

#### WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset

When "0" is written: No operation

Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.

This bit is dedicated for writing, and is always "0" for reading.

### 4.3.4 Programming notes

- (1) When the watchdog timer is being used, the software must reset it within 3-second cycles.
- (2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

## 4.4 Oscillation Circuit

### 4.4.1 Configuration of oscillation circuit

The S1C63657 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the S1C63657 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage must be switched according to the oscillation circuit to be used. Figure 4.4.1.1 is the block diagram of this oscillation system.

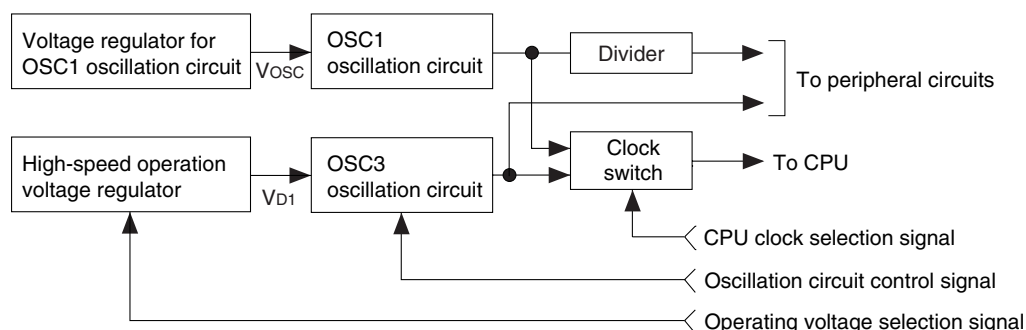


Fig. 4.4.1.1 Oscillation system block diagram

### 4.4.2 OSC1 oscillation circuit

The OSC1 crystal oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillation frequency is 32.768 kHz (Typ.).

Figure 4.4.2.1 is the block diagram of the OSC1 oscillation circuit.

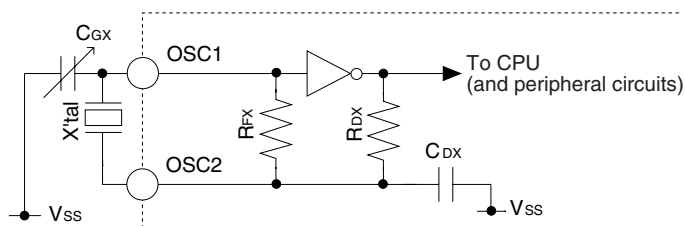


Fig. 4.4.2.1 OSC1 oscillation circuit

As shown in Figure 4.4.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator ( $X'_{tal}$ ) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor ( $C_{GX}$ ) between the OSC1 and  $V_{SS}$  terminals.



#### 4.4.3 OSC3 oscillation circuit

The S1C63657 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 4 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of the oscillator type from CR (external R type), CR (built-in R type) and ceramic oscillation circuit. When CR oscillation (external R type) is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required. When CR oscillation (built-in R type) is selected, no external element is required.

Figure 4.4.3.1 is the block diagram of the OSC3 oscillation circuit.

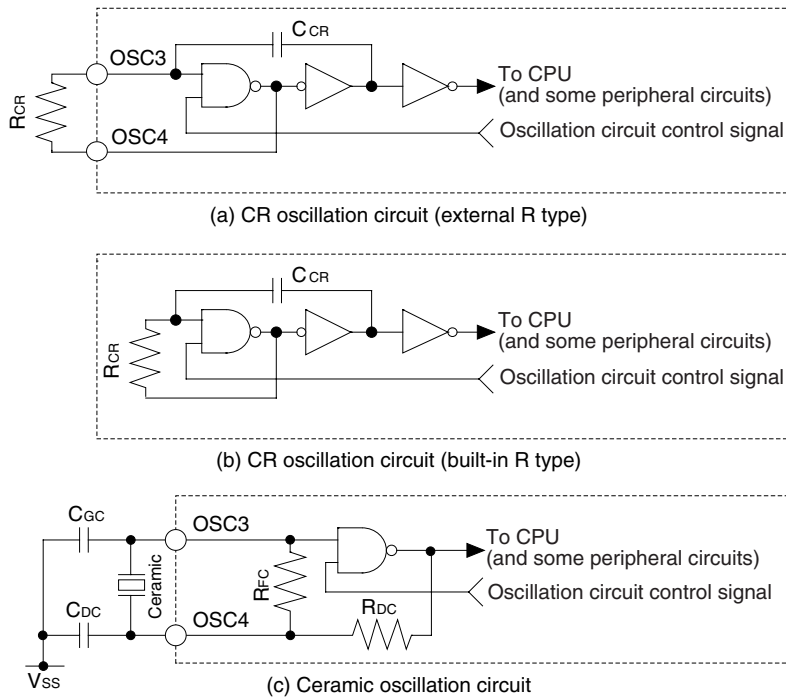


Fig. 4.4.3.1 OSC3 oscillation circuit

As shown in Figure 4.4.3.1, the CR oscillation circuit (external R type) can be configured simply by connecting the resistor  $R_{CR}$  between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of  $R_{CR}$ .

When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 4 MHz) between the OSC3 and OSC4 terminals, capacitor  $C_{GC}$  between the OSC3 and OSC4 terminals, and capacitor  $C_{DC}$  between the OSC4 and  $V_{SS}$  terminals. For both  $C_{GC}$  and  $C_{DC}$ , connect capacitors that are about 30 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

Table 4.4.3.1 OSC3 oscillation frequency

Oscillation circuit	Oscillation frequency
Ceramic oscillation	Max. 4 MHz (2 MHz <sup>Note</sup> )
CR oscillation (built-in R type)	Typ. 1.1 MHz $\pm 30\%$
CR oscillation (external R type)	200 kHz to 2 MHz

**Note:** When selecting OSC3 for the time base counter clock of the R/f converter, the maximum frequency of the OSC3 clock is limited to 2 MHz.

#### 4.4.4 Switching of operating voltage

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). In this case, to obtain stable operation, the operating voltage for the internal circuits must be switched by the software (VDC0 register).

When running with the OSC1 clock: Operating clock =  $V_{D1L}$  ( $VDC0 = "0"$ ,  $VDC1 = "0"$ )

When running with the OSC3 clock: Operating clock =  $V_{D3}$  ( $VDC0 = "1"$ ,  $VDC1 = "1"$ )

The CPU clock should be switched using the following procedure. Pay special attention to the stability waiting time for operating voltage and oscillation.

Note that the OSC3 clock cannot be used as the system clock in the halver mode. When the low-speed operation voltage regulator is in the halver mode, return it to the normal mode before switching the operating voltage.

##### OSC1 → OSC3

1. Set VDC2 to "0". (low-speed operation voltage regulator: halver mode → normal mode)
2. Set VDC1 to "1". (high-speed operation voltage regulator: off → on)
3. Set VDC0 to "1". (internal logic operating voltage:  $V_{D1L} \rightarrow V_{D3}$ )
4. Wait 2.5 msec or more.
5. Set OSCC to "1". (OSC3 oscillation: off → on)
6. Wait 5 msec or more.
7. Set CLKCHG to "1". (CPU clock: OSC1 → OSC3)

##### OSC3 → OSC1

1. Set CLKCHG to "0". (CPU clock: OSC3 → OSC1)
2. Set OSCC to "0". (OSC3 oscillation: on → off)
3. Set VDC0 to "0". (internal logic operating voltage:  $V_{D3} \rightarrow V_{D1L}$ )
4. Set the halver mode if necessary.

Refer to Section 4.2, "Power Control", for the halver mode.

*Note: If the HALT instruction is executed or HALT mode is canceled while the CPU is running with the high-speed clock generated by the OSC3 oscillation circuit, the internal logic operating voltage  $V_{D1}$  becomes unstable momentarily and it may cause unexpected problem, such as runaway, be occurred. Do not use the HALT instruction while the CPU is running with the OSC3 high-speed clock.*

#### 4.4.5 Clock frequency and instruction execution time

Table 4.4.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.4.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC3: 1.1 MHz	1.8	3.6	5.5
OSC3: 2 MHz	1	2	3
OSC3: 4 MHz	0.5	1	1.5

### 4.4.6 I/O memory of oscillation circuit

Table 4.4.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.4.6.1 Control bits of oscillation circuit

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF00H	VDC3	VDC2	VDC1	VDC0	VDC3	0	1/2V <sub>DD</sub>	V <sub>DD</sub>	LCD system voltage regulator power source switch
					VDC2	0	1/2V <sub>DD</sub>	V <sub>DD</sub>	Low-speed operation voltage regulator power source switch
	R/W				VDC1	0	On	Off	High-speed operation voltage regulator on/off
					VDC0	0	V <sub>D3</sub>	V <sub>D1L</sub>	Logic system power source switch
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### VDC0: Internal logic system power switching register (FF00H•D0)

It is used to switch the operating voltage for the CPU and internal circuit.

When "1" is written: V<sub>D3</sub> (for OSC3 operation)

When "0" is written: V<sub>D1L</sub> (for OSC1 operation)

Reading: Valid

When "1" is written to VDC0, the internal operating voltage is switched to V<sub>D3</sub>. After switching to V<sub>D3</sub>, the OSC3 oscillation can be started.

When the low-speed operation voltage regulator is in the halver mode, return it to the normal mode before switching to V<sub>D3</sub>.

When "0" is written to VDC0, the internal operating voltage is switched to V<sub>D1L</sub>. Stop the OSC3 oscillation before switching to V<sub>D1L</sub>.

At initial reset, this register is set to "0".

#### OSCC: OSC3 oscillation control register (FF01H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation On

When "0" is written: OSC3 oscillation Off

Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption. Furthermore, it is necessary to switch the operating voltage when turning the OSC3 oscillation circuit on and off.

At initial reset, this register is set to "0".

#### CLKCHG: CPU system clock switching register (FF01H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected

When "0" is written: OSC1 clock is selected

Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".

After turning the OSC3 oscillation on (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.

When VDC0 = "0" and OSCC = "0" (OSC3 oscillation is off), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed. Furthermore, do not switch the CPU clock to OSC3 in the halver mode.

At initial reset, this register is set to "0".

### 4.4.7 Programming notes

- (1) When switching the CPU system clock from OSC1 to OSC3, first set the operating voltage for high-speed operation (VD3). After that maintain 2.5 msec or more, and then turn the OSC3 oscillation on. When switching from OSC3 to OSC1, set the operating voltage for low-speed operation (VD1L) after switching to OSC1 and turning the OSC3 oscillation off.
- (2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on. Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.
- (3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.
- (4) When the low-speed operation voltage regulator is in the halver mode (VDC2 = "1"), the system can be operated only in low-speed using the OSC1 clock. Do not switch the system clock to OSC3.
- (5) Do not switch the operating voltage to VD1L while the CPU is operating with the OSC3 clock. Furthermore, do not stop the high-speed operating voltage regulator.
- (6) When selecting OSC3 for the time base counter clock of the R/f converter, the maximum frequency of the OSC3 clock is limited to 2 MHz.
- (7) If the HALT instruction is executed or HALT mode is canceled while the CPU is running with the high-speed clock generated by the OSC3 oscillation circuit, the internal logic operating voltage VD1 becomes unstable momentarily and it may cause unexpected problem, such as runaway, be occurred. Do not use the HALT instruction while the CPU is running with the OSC3 high-speed clock.

## 4.5 Input Ports (K00–K03 and K10–K13)

### 4.5.1 Configuration of input ports

The S1C63657 has eight bits of general-purpose input ports (K00–K03, K10–K13). Each input port terminal provides an internal pull-down resistor that can be enabled by mask option.

Figure 4.5.1.1 shows the configuration of input port.

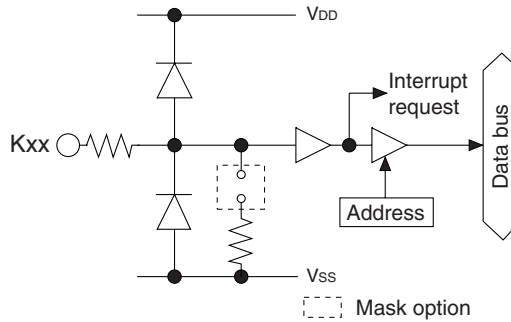


Fig. 4.5.1.1 Configuration of input port

Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

The K13 port can also be used as the event counter input for the programmable timer.

### 4.5.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.

Figure 4.5.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

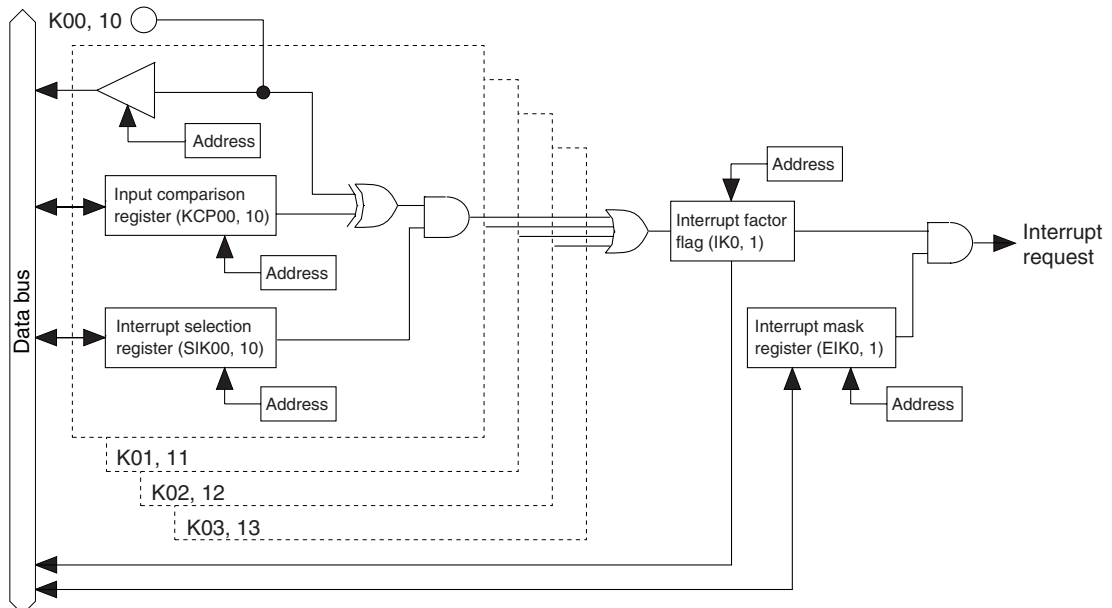


Fig. 4.5.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminals for generating interrupt and interrupt timing.

The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.

The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13).

By setting these two conditions, the interrupt for K00–K03 or K10–K13 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.

The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected for K00–K03 and K10–K13.

When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".

Figure 4.5.2.2 shows an example of an interrupt for K00–K03.

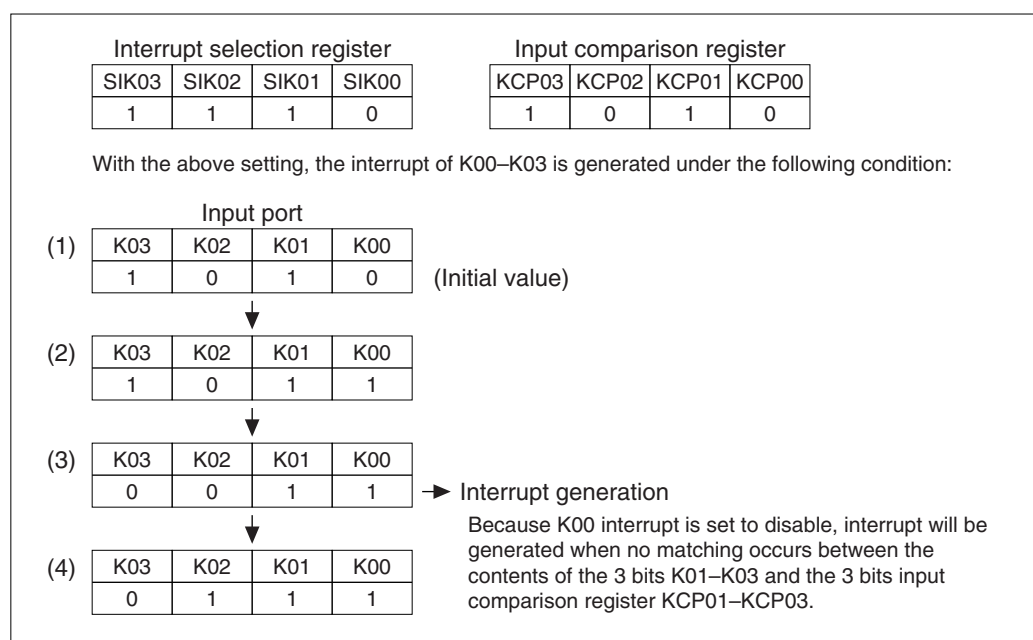


Fig. 4.5.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

### 4.5.3 Mask option

Internal pull-down resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.

When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

### 4.5.4 I/O memory of input ports

Table 4.5.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.5.4.1 Control bits of input ports

Address	Register				Name	Init #1	1	0	Comment
	D3	D2	D1	D0					
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	–*2	High	Low	K00–K03 input port data
					K02	–*2	High	Low	
	R				K01	–*2	High	Low	
					K00	–*2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	–*2	High	Low	K10–K13 input port data
					K12	–*2	High	Low	
	R				K11	–*2	High	Low	
					K10	–*2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FFE3H	0	0	0	EIK0	0 *3	–*2		Unused	Interrupt mask register (K00–K03)
					0 *3	–*2		Unused	
	R			R/W	0 *3	–*2		Unused	
					EIK0	0	Enable	Mask	
FFE4H	0	0	0	EIK1	0 *3	–*2		Unused	Interrupt mask register (K10–K13)
					0 *3	–*2		Unused	
	R			R/W	0 *3	–*2		Unused	
					EIK1	0	Enable	Mask	
FFF3H	0	0	0	IK0	0 *3	–*2	(R)	(R)	Unused
					0 *3	–*2	Yes	No	Unused
	R			R/W	0 *3	–*2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	–*2	(R)	(R)	Unused
					0 *3	–*2	Yes	No	Unused
	R			R/W	0 *3	–*2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### K00–K03: K0 port input port data (FF21H)

#### K10–K13: K1 port input port data (FF25H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level

When "0" is read: Low level

Writing: Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (VDD), and "0" when the voltage goes low (VSS).

These bits are dedicated for reading, so writing cannot be done.

**SIK00–SIK03: K0 port interrupt selection register (FF20H)**

**SIK10–SIK13: K1 port interrupt selection register (FF24H)**

Selects the ports to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable

When "0" is written: Disable

Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.

At initial reset, these registers are set to "0".

**KCP00–KCP03: K0 port input comparison register (FF22H)**

**KCP10–KCP13: K1 port input comparison register (FF26H)**

Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written: Falling edge

When "0" is written: Rising edge

Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).

For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.

At initial reset, these registers are set to "1".

**EIK0: K0 input interrupt mask register (FFE3H•D0)**

**EIK1: K1 input interrupt mask register (FFE4H•D0)**

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable

When "0" is written: Mask

Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the two systems (K00–K03, K10–K13).

At initial reset, these registers are set to "0".

**IK0: K0 input interrupt factor flag (FFF3H•D0)**

**IK1: K1 input interrupt factor flag (FFF4H•D0)**

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.

The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".



### 4.5.5 Programming notes

- (1) When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF

R: pull-down resistance 375 kΩ (Max.)

- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

## 4.6 Output Ports (R00–R03 and R10–R13)

### 4.6.1 Configuration of output ports

The S1C63657 has eight bits of general output ports.

Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and P-channel open drain output.

Figure 4.6.1.1 shows the configuration of the output port.

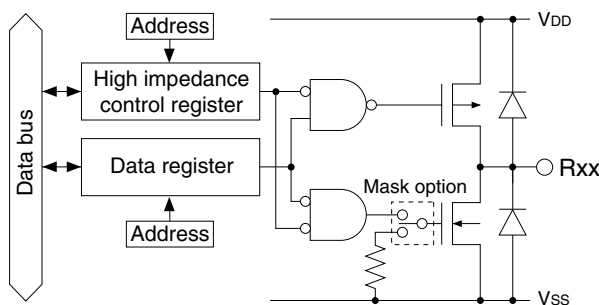


Fig. 4.6.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.

At initial reset, these are all set to the general purpose output port.

Table 4.6.1.1 shows the setting of the output terminals by function selection.

Table 4.6.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (Low output)	R00	R00
R01	R01 (Low output)	R01	R01
R02	R02 (Low output)	TOUT	
R03	R03 (Low output)		FOUT
R10–R13	R10–R13 (Low output)	R10–R13	R10–R13

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixed at "0" (data output).

**Note:** If an output terminal (including a special output terminal) of this IC is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

### 4.6.2 Mask option

Output specifications of the output ports are selected by mask option.

Either complementary output or P-channel open drain output can be selected individually (in 1-bit units). However, when P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

### 4.6.3 High impedance control

The output ports can be set into a high impedance status. This control is done using the high impedance control registers.

The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1 bit)
R01HIZ	R01 (1 bit)
R02HIZ	R02 (1 bit)
R03HIZ	R03 (1 bit)
R1HIZ	R10–R13 (4 bits)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

### 4.6.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.6.4.1 with the software.

Figure 4.6.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.6.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT

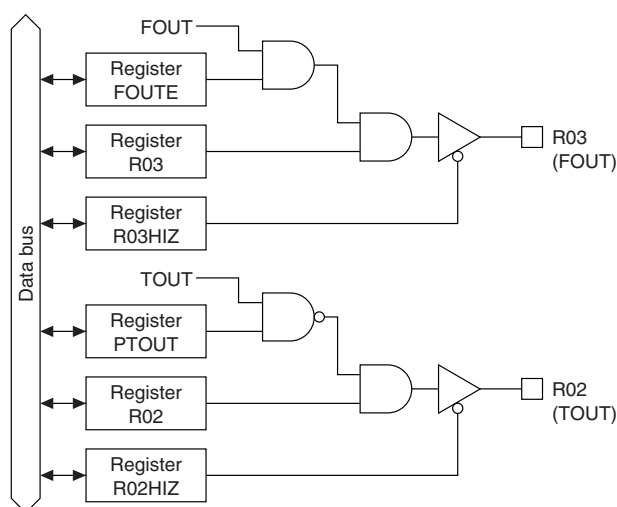


Fig. 4.6.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "0" and the high impedance control register is set to "0". Consequently, the output terminal goes low (Vss).

When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned on and off using the special output control register.

- Note:**
- Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
  - Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

### • TOUT (R02)

The R02 terminal can output a TOUT signal.

The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.

To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal on and off using the PTOUT register. It is, however, necessary to control the programmable timer.

Refer to Section 4.11, "Programmable Timer" for details of the programmable timer.

**Note:** A hazard may occur when the TOUT signal is turned on and off.

Figure 4.6.4.2 shows the output waveform of the TOUT signal.

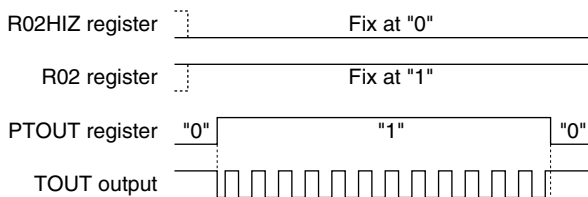


Fig. 4.6.4.2 Output waveform of TOUT signal

### • FOUT (R03)

The R03 terminal can output an FOUT signal.

The FOUT signal is a clock (fosc1 or fosc3) that is output from the oscillation circuit or a clock that the fosc1 clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.

To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal on and off using the FOUTE register.

The frequency of the output clock may be selected from among 4 types shown in Table 4.6.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.6.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	fosc3
1	0	fosc1
0	1	fosc1 × 1/8
0	0	fosc1 × 1/64

fosc1: Clock that is output from the OSC1 oscillation circuit

fosc3: Clock that is output from the OSC3 oscillation circuit

When fosc3 is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.

Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

**Note:** A hazard may occur when the FOUT signal is turned on and off.

Figure 4.6.4.3 shows the output waveform of the FOUT signal.

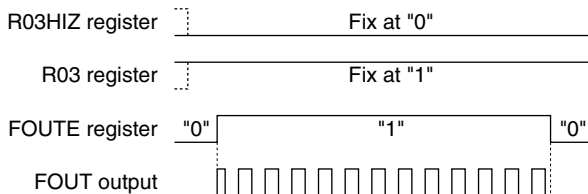


Fig. 4.6.4.3 Output waveform of FOUT signal

### 4.6.5 I/O memory of output ports

Table 4.6.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.6.5.1 Control bits of output ports

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable General-purpose register FOUT frequency selection [FOFQ1, 0] 0 1 2 3 Frequency fosc1/64 fosc1/8 fosc1 fosc3
					SWDIR	0	1	0	
					FOFQ1	0			
					FOFQ0	0			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	Hi-Z	Output	R03 (FOUTE=0)/FOUT (FOUTE=1) Hi-Z control R02 (PTOUT=0)/TOUT (PTOUT=1) Hi-Z control R01 Hi-Z control R00 Hi-Z control
					R02HIZ	0	Hi-Z	Output	
					R01HIZ	0	Hi-Z	Output	
					R00HIZ	0	Hi-Z	Output	
FF31H	R03	R02	R01	R00	R03	0	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used. R02 output port data (PTOUT=0) Fix at "1" when TOUT is used. R01 output port data R00 output port data
					R02	0	High	Low	
					R01	0	High	Low	
					R00	0	High	Low	
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused Unused Unused R10–R13 Hi-Z control
					0 *3	– *2			
					0 *3	– *2			
					R1HIZ	0	Hi-Z	Output	
FF33H	R13	R12	R11	R10	R13	0	High	Low	R10–R13 output port data
					R12	0	High	Low	
					R11	0	High	Low	
					R10	0	High	Low	
FFC1H	0	CHSEL1	CHSEL0	PTOUT	0 *3	– *2			Unused TOUT output selection [CHSEL1,0] 0 1 2 3 Timer Timer 0 Timer 1 Timer 2 Output="1" (fixed) TOUT output control
					CHSEL1	0			
					CHSEL0	0			
	R				PTOUT	0	On	Off	

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)

#### R1HIZ: R1 port high impedance control register (FF32H•D0)

Controls high impedance output of the output port.

When "1" is written: High impedance

When "0" is written: Data output

Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.

When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).

At initial reset, these registers are set to "0".

**R00–R03: R0 output port data register (FF31H)****R10–R13: R1 output port data register (FF33H)**

Set the output data for the output ports.

When "1" is written: High level output

When "0" is written: Low level output

Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (VDD), and when "0" is written, the output port terminal goes low (VSS).

When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02 register and the R03 register at "1".

At initial reset, these registers are all set to "0".

**FOUTE: FOUT output control register (FF06H•D3)**

Controls the FOUT output.

When "1" is written: FOUT output On

When "0" is written: FOUT output Off

Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", the FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes low (VSS).

When using the R03 output port for DC output, fix this register at "0".

At initial reset, this register is set to "0".

**FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)**

Selects a frequency of the FOUT signal.

*Table 4.6.5.2 FOUT clock frequency*

FOFQ1	FOFQ0	Clock frequency
1	1	fosc3
1	0	fosc1
0	1	fosc1 × 1/8
0	0	fosc1 × 1/64

At initial reset, this register is set to "0".

**PTOUT: TOUT output control register (FFC1H•D0)**

Controls the TOUT output.

When "1" is written: TOUT output On

When "0" is written: TOUT output Off

Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (VDD).

When using the R02 output port for DC output, fix this register at "0".

At initial reset, this register is set to "0".

#### 4.6.6 Programming notes

- (1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).  
Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.  
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).
- (2) A hazard may occur when the FOUT signal and the TOUT signal are turned on and off.
- (3) When fOSC3 is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.  
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

## 4.7 I/O Ports (P00–P03 and P10–P13)

### 4.7.1 Configuration of I/O ports

The S1C63657 has eight bits of general-purpose I/O ports. Figure 4.7.1.1 shows the configuration of the I/O port.

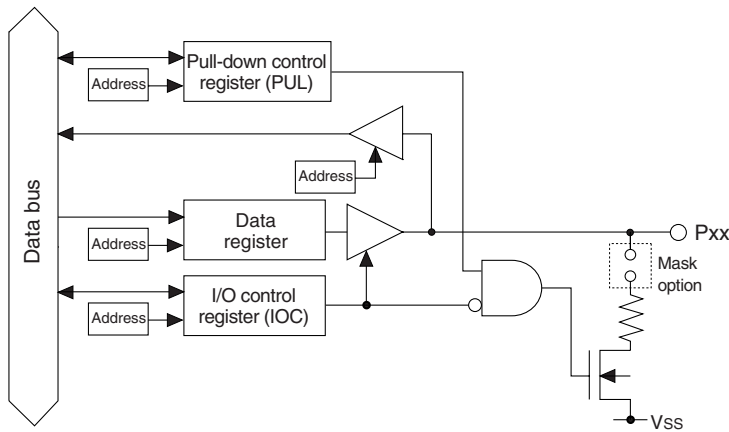


Fig. 4.7.1.1 Configuration of I/O port

The I/O ports can be set to either input mode or output mode individually (in 1-bit unit). Modes can be set by writing data to the I/O control registers.

**Note:** If an output of this IC is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

### 4.7.2 Mask option

The output specification of each I/O port during output mode can be selected from either complementary output or P-channel open drain output by mask option. This selection can be done in 1-bit units. When P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

The mask option also permits selection of whether the pull-down resistor is used or not during input mode. This selection can be done in 1-bit units.

When "without pull-down" during the input mode is selected, take care that the floating status does not occur.

### 4.7.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.

However, when the pull-down explained in the following section has been set by software, the input line is pulled down only during this input mode.

To set the output mode, write "1" to the I/O control register. When an I/O port is set to output mode, it works as an output port, it outputs a high level (VDD) when the port output data is "1", and a low level (VSS) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.



#### 4.7.4 Pull-down during input mode

A pull-down resistor that operates during the input mode is built into each I/O port of the S1C63657. Mask option can set the use or non-use of this pull-down.

The pull-down resistor becomes effective by writing "1" to the pull-down control register PULxx that corresponds to each port, and the input line is pulled down during the input mode. When "0" has been written, no pull-down is done.

At initial reset, the pull-down control registers are set to "1".

The pull-down control registers of the ports in which "gate direct" has been selected can be used as general purpose registers.

#### 4.7.5 I/O memory of I/O ports

Table 4.7.5.1 shows the I/O addresses and the control bits for the I/O ports.

Table 4.7.5.1 Control bits of I/O ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
					IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
					PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
					P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P10–P13 I/O control register
					IOC12	0	Output	Input	
					IOC11	0	Output	Input	
					IOC10	0	Output	Input	
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P10–P13 pull-down control register
					PUL12	1	On	Off	
					PUL11	1	On	Off	
					PUL10	1	On	Off	
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data
					P12	– *2	High	Low	
					P11	– *2	High	Low	
					P10	– *2	High	Low	

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### P00–P03: P0 I/O port data register (FF42H)

#### P10–P13: P1 I/O port data register (FF46H)

I/O port data can be read and output data can be set through these registers.

##### • When writing data

When "1" is written: High level

When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (VDD), and when "0" is written, the terminal goes low (Vss).

Port data can be written also in the input mode.

### • When reading data

When "1" is read: High level

When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (VDD) the port data that can be read is "1", and when the terminal voltage is low (VSS) the data is "0".

When "with pull-down resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-down resistor goes on during input mode, so that the I/O port terminal is pulled down.

*Note: When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.*

*Particular care needs to be taken of the key scan during key matrix configuration.*

*Make this waiting time the amount of time or more calculated by the following expression.*

$$10 \times C \times R$$

*C: terminal capacitance 5 pF + parasitic capacitance ? pF*

*R: pull-down resistance 375 kΩ (Max.)*

### **IOC00–IOC03: P0 port I/O control register (FF40H)**

### **IOC10–IOC13: P1 port I/O control register (FF44H)**

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode

When "0" is written: Input mode

Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.

Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.

At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.

### **PUL00–PUL03: P0 port pull-down control register (FF41H)**

### **PUL10–PUL13: P1 port pull-down control register (FF45H)**

The pull-down during the input mode are set with these registers.

When "1" is written: Pull-down On

When "0" is written: Pull-down Off

Reading: Valid

The built-in pull-down resistor which is turned on during input mode is set to enable in 1-bit units. (The pull-down resistor is included into the ports selected by mask option.)

By writing "1" to the pull-down control register, the corresponding I/O ports are pulled down (during input mode), while writing "0" disables the pull-down function.

At initial reset, these registers are all set to "1", so the pull-down function is enabled.

The pull-down control registers of the ports in which the pull-down resistor is not included become the general purpose register.

### **4.7.6 Programming note**

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF

R: pull-down resistance 375 kΩ (Max.)

## 4.8 LCD Driver (COM0–COM7, SEG0–SEG55)

### 4.8.1 Configuration of LCD driver

The S1C63657 has 8 common terminals (COM0–COM7) and 56 segment terminals (SEG0–SEG55), so that it can drive an LCD with a maximum of 448 ( $56 \times 8$ ) segments.

The driving method is 1/4 duty, 1/5 duty or 1/8 duty dynamic drive with three voltages (1/3 bias),  $V_{C1}$ ,  $V_{C2}$  and  $V_{C3}$ .

LCD display on/off can be controlled by the software.

### 4.8.2 Power supply for LCD driving

The power supply for driving LCD can be selected from the internal power supply and an external power supply.

When the internal power supply is selected, the LCD drive voltages  $V_{C1}$ – $V_{C3}$  are generated by the built-in LCD system voltage circuit. The LCD system voltage circuit is turned on and off using the LPWR register. When LPWR is set to "1", the LCD system voltage circuit outputs the LCD drive voltages  $V_{C1}$ – $V_{C3}$  to the LCD driver. The LCD system voltage circuit generates  $V_{C1}$  with the voltage regulator built-in, and generates two other voltages ( $V_{C2} = 2V_{C1}$ ,  $V_{C3} = 3V_{C1}$ ) by boosting  $V_{C1}$ .

When using an external power supply, select the voltage from the following 3 types and supply the LCD drive voltage to the  $V_{C1}$ – $V_{C3}$  terminals.

- 1) External power supply 1/3 bias (for 4.5 V panel)  $V_{DD} = V_{C2}$
- 2) External power supply 1/3 bias (for 3.0 V panel)  $V_{DD} = V_{C3}$
- 3) External power supply 1/2 bias (for 3.0 V panel)  $V_{DD} = V_{C3}$ ,  $V_{C1} = V_{C2}$  (static drive function is available)

Note that the power control using the LPWR register is necessary even if an external power supply is used. SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power on/off control by the LPWR register.

### 4.8.3 Control of LCD display and drive waveform

#### (1) Display on/off control

The S1C63657 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the segments go on, and when "1" is written to ALOFF, all the segments go off. At such a time, an on waveform or an off waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all on) has priority over the ALOFF (all off).

#### (2) Setting of drive duty

In the S1C63657, the drive duty can be set to 1/4, 1/5 or 1/8 using the LDUTY1 and LDUTY0 registers as shown in Table 4.8.3.1.

Table 4.8.3.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/8	COM0–COM7	448 ( $56 \times 8$ )
0	1	1/5	COM0–COM4	280 ( $56 \times 5$ )
0	0	1/4	COM0–COM3	224 ( $56 \times 4$ )

Table 4.8.3.2 shows the frame frequency corresponding to the drive duty.

Table 4.8.3.2 Frame frequency

OSC1 oscillation frequency	When 1/8 duty is selected	When 1/5 duty is selected	When 1/4 duty is selected
32.768 kHz	32 Hz	25 Hz	32 Hz

Figures 4.8.3.1 to 4.8.3.3 show the dynamic drive waveform according to the duty.

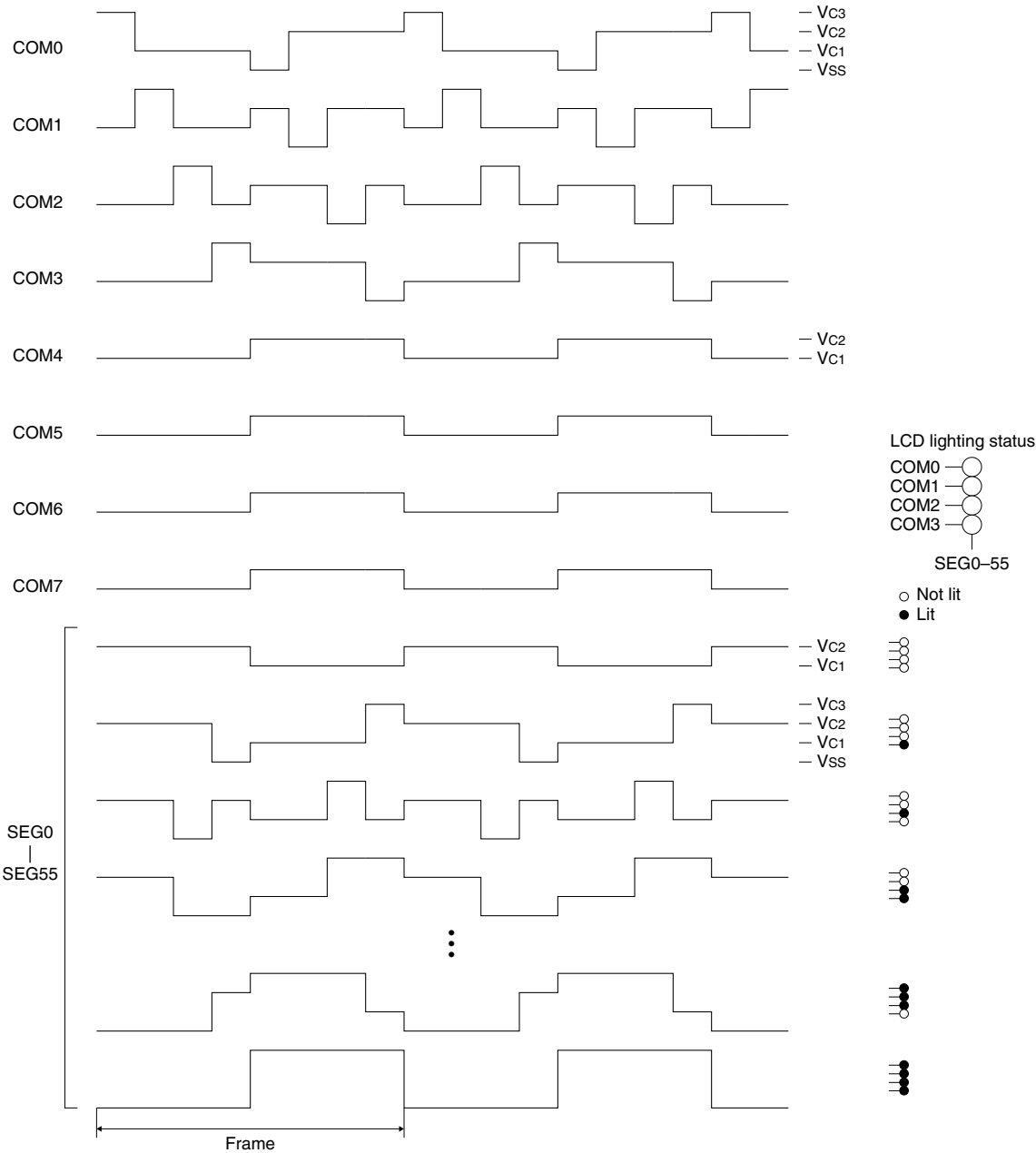


Fig. 4.8.3.1 Dynamic drive waveform for 1/4 duty

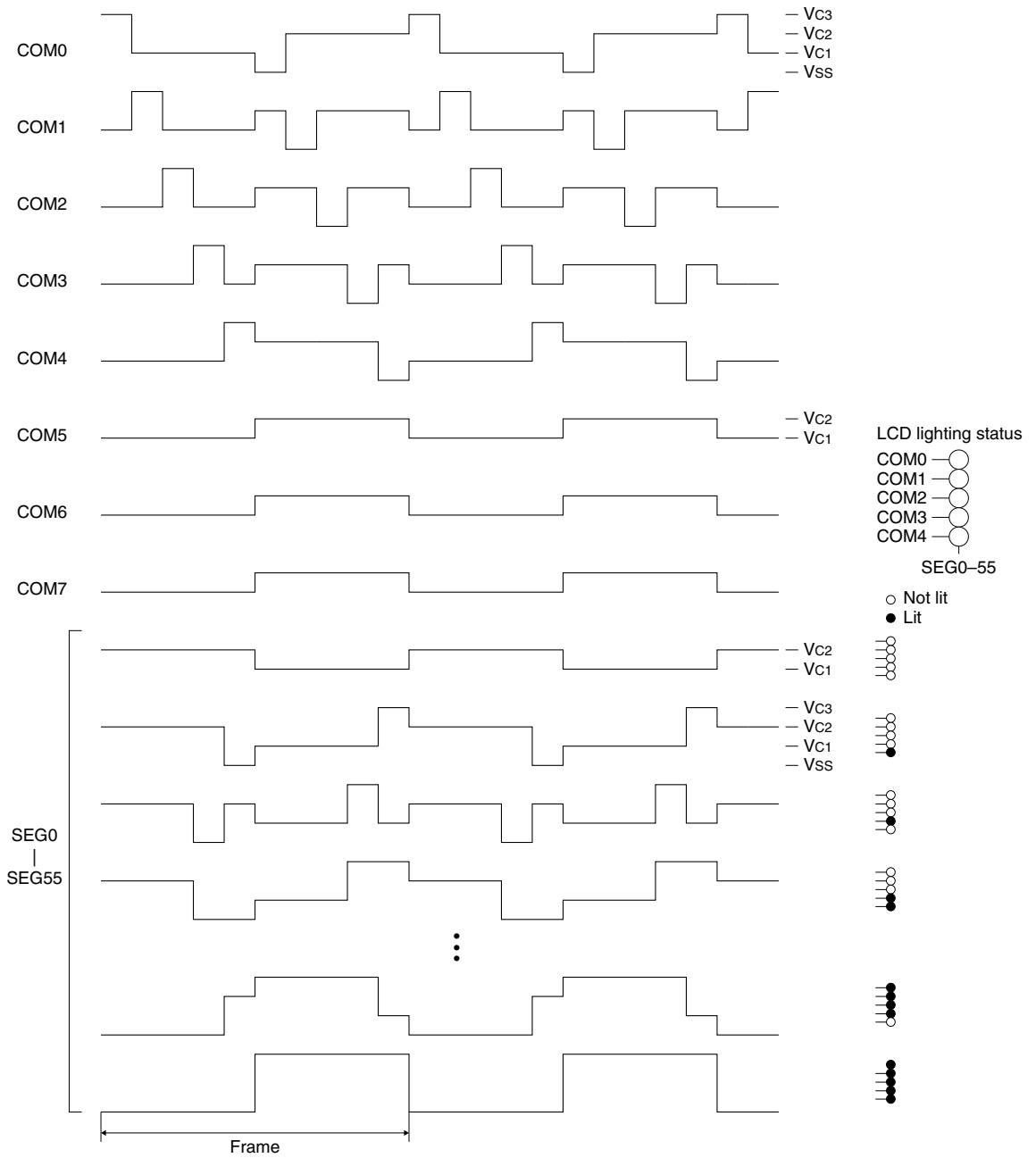


Fig. 4.8.3.2 Dynamic drive waveform for 1/5 duty

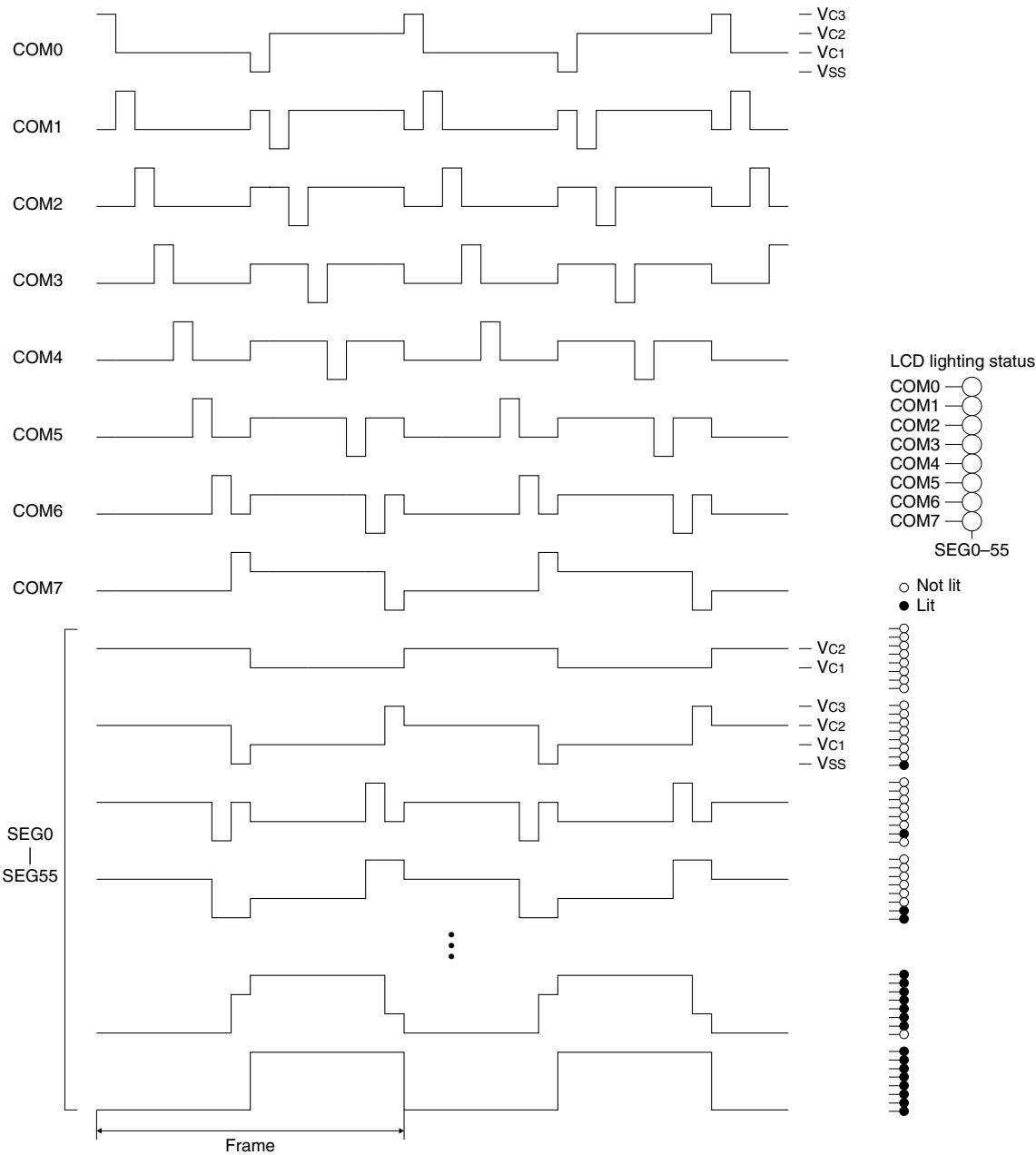


Fig. 4.8.3.3 Dynamic drive waveform for 1/8 duty

### (3) Static drive

The S1C63657 provides software setting of the LCD static drive. However, this function is available only when "External power supply 1/2 bias (for 3.0 V panel)" is selected by mask option. To set in static drive, write "1" to the common output signal control register STCD. Then, by writing "1" to any one of COM0 to COM7 (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static on waveform. When all the COM0 to COM7 bits are set to "0", the SEG terminal outputs a dynamic off waveform.

Figure 4.8.3.4 shows the static drive waveform.

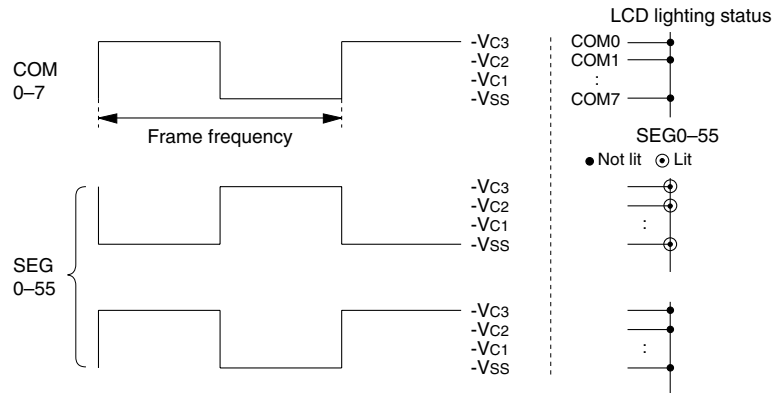


Fig. 4.8.3.4 Static drive waveform

**Note:** To use the static drive function, select the "External power supply 1/2 bias (for 3.0 V panel)" mask option. When an option for using the internal power supply or a 1/3 bias external power supply is selected, static drive cannot be set using the STCD register.

### 4.8.4 Display memory

The display memory is allocated to F000H–F09FH in the data memory area and each data bit can be allocated to an segment terminal (SEG0–SEG55) by mask option.

When a bit in the display memory is set to "1", the corresponding LCD segment goes on, and when it is set to "0", the segment goes off.

At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.

The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

### 4.8.5 Segment option

#### Segment allocation

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F09FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.8.5.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/4 duty.

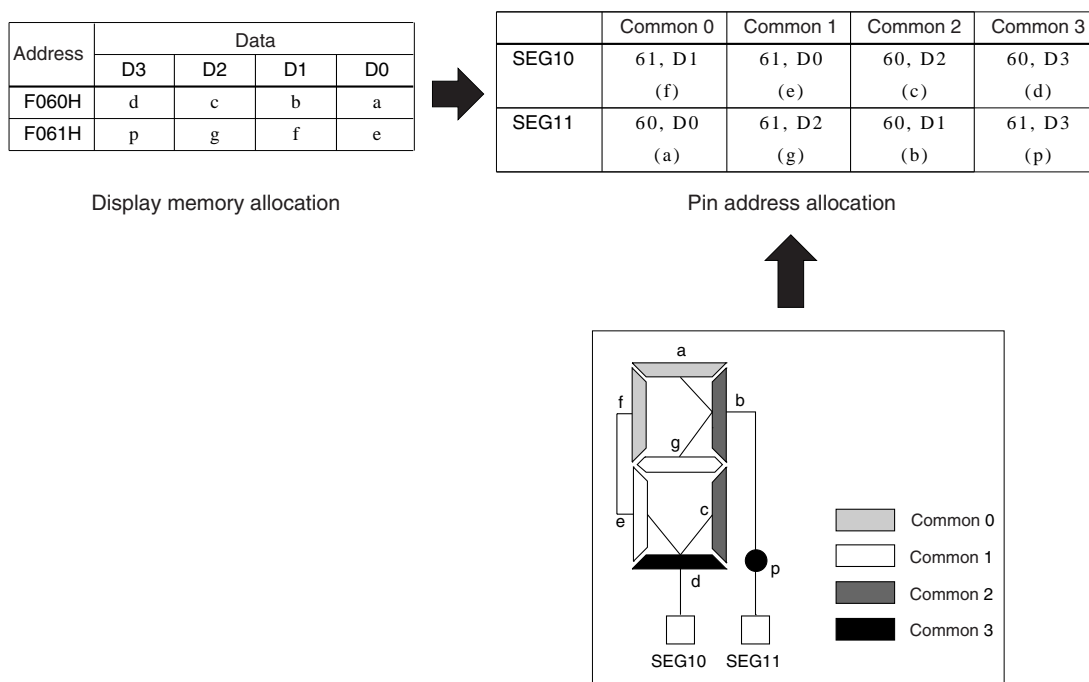


Fig. 4.8.5.1 Segment allocation

#### Output specification

1. The segment terminals (SEG0–SEG55) can be selected with the mask option in pairs\* for either segment signal output or DC output (VDD and VSS binary output).  
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
2. When DC output is selected, either complementary output or N-channel open drain output can be selected for each terminal with the mask option.

\* The terminal pairs are combination of  $SEG2 \times n$  and  $SEG2 \times n + 1$  (where  $n$  is an integer from 0 to 27).



Segment option list

Pin name	Address (F0xx)																								Output specification	
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7				
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D		
SEG0																									SEG output	<input type="checkbox"/> S
SEG1																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG2																									SEG output	<input type="checkbox"/> S
SEG3																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG4																									SEG output	<input type="checkbox"/> S
SEG5																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG6																									SEG output	<input type="checkbox"/> S
SEG7																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG8																									SEG output	<input type="checkbox"/> S
SEG9																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG10																									SEG output	<input type="checkbox"/> S
SEG11																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG12																									SEG output	<input type="checkbox"/> S
SEG13																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG14																									SEG output	<input type="checkbox"/> S
SEG15																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG16																									SEG output	<input type="checkbox"/> S
SEG17																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG18																									SEG output	<input type="checkbox"/> S
SEG19																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG20																									SEG output	<input type="checkbox"/> S
SEG21																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG22																									SEG output	<input type="checkbox"/> S
SEG23																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG24																									SEG output	<input type="checkbox"/> S
SEG25																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG26																									SEG output	<input type="checkbox"/> S
SEG27																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG28																									SEG output	<input type="checkbox"/> S
SEG29																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG30																									SEG output	<input type="checkbox"/> S
SEG31																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG32																									SEG output	<input type="checkbox"/> S
SEG33																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG34																									SEG output	<input type="checkbox"/> S
SEG35																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG36																									SEG output	<input type="checkbox"/> S
SEG37																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG38																									SEG output	<input type="checkbox"/> S
SEG39																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG40																									SEG output	<input type="checkbox"/> S
SEG41																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG42																									SEG output	<input type="checkbox"/> S
SEG43																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG44																									SEG output	<input type="checkbox"/> S
SEG45																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG46																									SEG output	<input type="checkbox"/> S
SEG47																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG48																									SEG output	<input type="checkbox"/> S
SEG49																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG50																									SEG output	<input type="checkbox"/> S
SEG51																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG52																									SEG output	<input type="checkbox"/> S
SEG53																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
SEG54																									SEG output	<input type="checkbox"/> S
SEG55																									DC output	<input type="checkbox"/> C <input type="checkbox"/> N
<address> H: RAM data high-order address (0–9) L: RAM data low-order address (0–F) D: Data bit (0–3)																									<Output specification> S: Segment output C: Complementary output N: Nch open drain output	

### 4.8.6 LCD contrast adjustment

In the S1C63657, the LCD contrast can be adjusted by the software.

It is realized by controlling the voltages  $V_{C1}$ ,  $V_{C2}$  and  $V_{C3}$  output from the LCD system voltage circuit.

The contrast can be adjusted to 16 levels as shown in Table 4.8.6.1.  $V_{C1}$  is changed within the range from 0.95 to 1.40 V (0.03 V step), and other voltages change according to  $V_{C1}$ .

Table 4.8.6.1 LCD contrast

No.	LC3	LC2	LC1	LC0	$V_{C1}$ (V)	Contrast
0	0	0	0	0	0.95 *	light
1	0	0	0	1	0.98 *	↑
2	0	0	1	0	1.01 *	
3	0	0	1	1	1.04 *	
4	0	1	0	0	1.07 *	
5	0	1	0	1	1.10 *	
6	0	1	1	0	1.13 *	
7	0	1	1	1	1.16	
8	1	0	0	0	1.19	
9	1	0	0	1	1.22	
10	1	0	1	0	1.25	
11	1	0	1	1	1.28	
12	1	1	0	0	1.31	
13	1	1	0	1	1.34	
14	1	1	1	0	1.37	↓
15	1	1	1	1	1.40	dark

\* Do not set  $V_{C1}$  to 1.16 V or more (LC = 7 or more) when the LCD system voltage regulator is driven in the halver mode.

At initial reset, the LC0–LC3 are set to 0000B. The software should initialize the register to get the desired contrast.

When an external power supply is selected by mask option, the LC0–LC3 register becomes invalid.

### 4.8.7 I/O memory of LCD driver

Table 4.8.7.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.8.7.1 shows the display memory map.

Table 4.8.7.1 Control bits of LCD driver

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			] LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 Duty 1/4 1/5 1/8
					LDUTY0	0			
	R/W				STCD	0	Static	Dynamic	LCD drive switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	0	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all Off control
	R	R/W		R	ALON	0	All On	Normal	LCD all On control
					0 *3	– *2			Unused
FF62H	LC3	LC2	LC1	LC0	LC3	0			] LCD contrast adjustment [LC3–0] 0 – 15 Contrast Light – Dark
					LC2	0			
					LC1	0			
	R/W				LC0	0			

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

Address Low Base	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000H	Display memory (160 words × 4 bits) R/W															
F010H																
F020H																
F030H																
F040H																
F050H																
F060H																
F070H																
F080H																
F090H																

Fig. 4.8.7.1 Display memory map

#### LPWR: LCD power control (on/off) register (FF60H•D0)

Turns the LCD system voltage circuit on and off.

When "1" is written: On

When "0" is written: Off

Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes on and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to Vss level.

It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.

This control does not affect to SEG terminals that have been set for DC output.

At initial reset, this register is set to "0".

#### LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.8.7.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/8	COM0–COM7	448 (56 × 8)
0	1	1/5	COM0–COM4	280 (56 × 5)
0	0	1/4	COM0–COM3	224 (56 × 4)

At initial reset, this register is set to "0".

#### STCD: LCD drive switch register (FF60H•D1)

Switches the LCD driving method.

When "1" is written: Static drive  
 When "0" is written: Dynamic drive  
 Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.  
 At initial reset, this register is set to "0".

#### ALON: LCD all on control register (FF61H•D1)

Displays the all LCD segments on.

When "1" is written: All LCD segments displayed  
 When "0" is written: Normal display  
 Reading: Valid

By writing "1" to the ALON register, all the LCD segments go on, and when "0" is written, it returns to normal display. This function outputs an on waveform to the SEG terminals, and segments not affect the content of the display memory. ALON has priority over ALOFF.  
 At initial reset, this register is set to "0".

#### ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out  
 When "0" is written: Normal display  
 Reading: Valid

By writing "1" to the ALOFF register, all the LCD segments go off, and when "0" is written, it returns to normal display. This function outputs an off waveform to the SEG terminals, and does not affect the content of the display memory.  
 ALON (FF61H•D1) has priority over ALOFF, so all the LCD segments go on when ALON and ALOFF are set to "1" simultaneously.  
 At initial reset, this register is set to "1".

#### LC3–LC0: LCD contrast adjustment register (FF62H)

Adjusts the LCD contrast.

LC3–LC0 = 0000B    light  
                   :       :  
 LC3–LC0 = 1111B    dark

When the LCD drive voltage is supplied from outside by mask option selection, this adjustment becomes invalid.  
 At initial reset, LC0–LC3 is set to 0000B.

### 4.8.8 Programming note

Because at initial reset, the contents of display memory are undefined and LC3–LC0 (LCD contrast) is set to 0000B, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes off.

## 4.9 Clock Timer

### 4.9.1 Configuration of clock timer

The S1C63657 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.

Figure 4.9.1.1 is the block diagram for the clock timer.

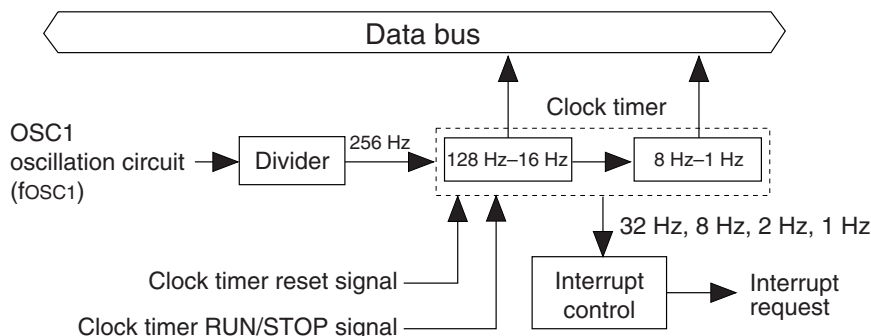


Fig. 4.9.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

### 4.9.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF75H and FF76H.

<FF75H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF76H>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).

The high-order data hold function in the S1C63657 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

*Note:* Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.9.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.

Figure 4.9.3.1 is the timing chart of the clock timer.

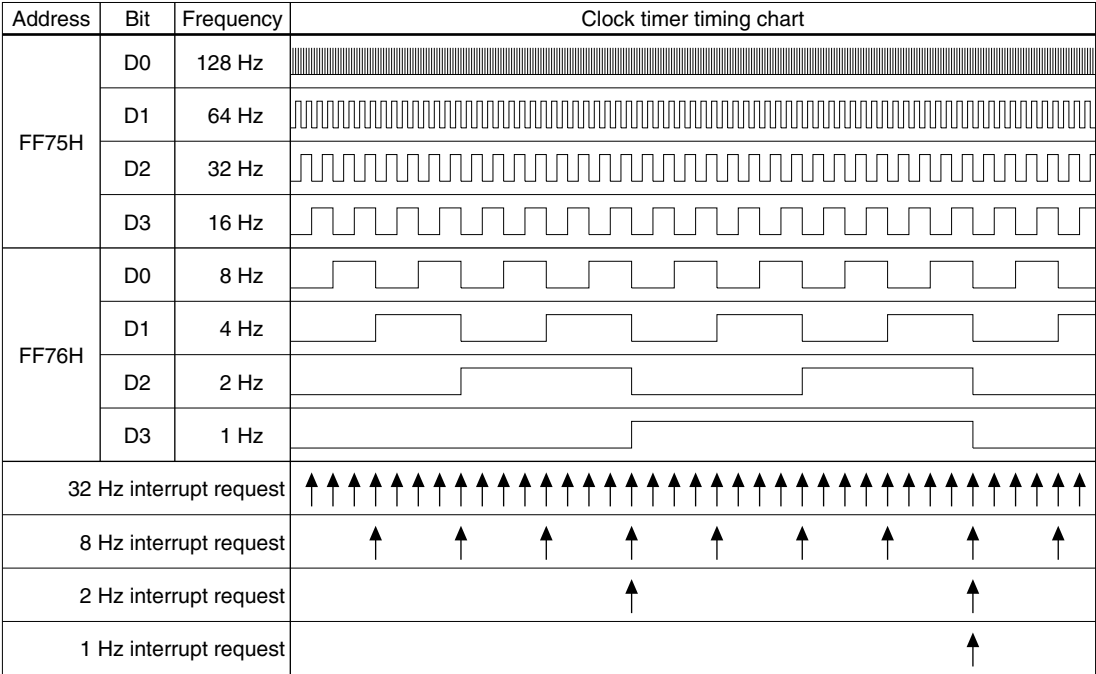


Fig. 4.9.3.1 Timing chart of clock timer

As shown in Figure 4.9.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

### 4.9.4 I/O memory of clock timer

Table 4.9.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.9.4.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF74H	0	0	TMRST	TMRUN	0 *3 0 *3	— *2 — *2			Unused Unused
	R		W	R/W	TMRST*3 TMRUN	Reset 0	Reset Run	Invalid Stop	Clock timer reset (writing) Clock timer Run/Stop
FF75H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF76H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### TM0–TM7: Timer data (FF75H, FF76H)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF75H), the high-order data (FF76H) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

#### TMRST: Clock timer reset (FF74H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset

When "0" is written: No operation

Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

#### TMRUN: Clock timer RUN/STOP control register (FF74H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN

When "0" is written: STOP

Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.

At initial reset, this register is set to "0".

**EIT0: 32 Hz interrupt mask register (FFE5H•D0)**

**EIT1: 8 Hz interrupt mask register (FFE5H•D1)**

**EIT2: 2 Hz interrupt mask register (FFE5H•D2)**

**EIT3: 1 Hz interrupt mask register (FFE5H•D3)**

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz).

At initial reset, these registers are set to "0".

**IT0: 32 Hz interrupt factor flag (FFF5H•D0)**

**IT1: 8 Hz interrupt factor flag (FFF5H•D1)**

**IT2: 2 Hz interrupt factor flag (FFF5H•D2)**

**IT3: 1 Hz interrupt factor flag (FFF5H•D3)**

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

#### **4.9.5 Programming notes**

- (1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.



## 4.10 Programmable Timer

### 4.10.1 Configuration of programmable timer

The S1C63657 has three 8-bit programmable timer systems (timer 0, timer 1 and timer 2) built-in. The timers are composed of 8-bit presettable down counters and they can be used as 8 bits  $\times$  3 channels or 16 bits  $\times$  1 channel + 8 bits  $\times$  1 channel of programmable timers. Timer 0 also has an event counter function using the K13 input port terminal.

Figure 4.10.1.1 shows the configuration of the programmable timer.

Each timer has an 8-bit down counter and an 8-bit reload data register. The down counter counts the input clock. When the down counter underflows, the timer outputs the underflow and interrupt signals and resets the counter to its initial value. The reload data register is used to store that initial value. Timers 0 and 1 have an 8-bit compare data register in addition to the above registers. This register is used to store data to be compared with the contents of the down counter. When the timer is set in the PWM mode, the timer outputs the compare match signal if the contents between the down counter and the compare data register are matched, and an interrupt occurs at the same time. Also the compare match signal is used with the underflow signal to generate a PWM waveform. The signal generated by the programmable timer can be output from the R02 output port terminal.

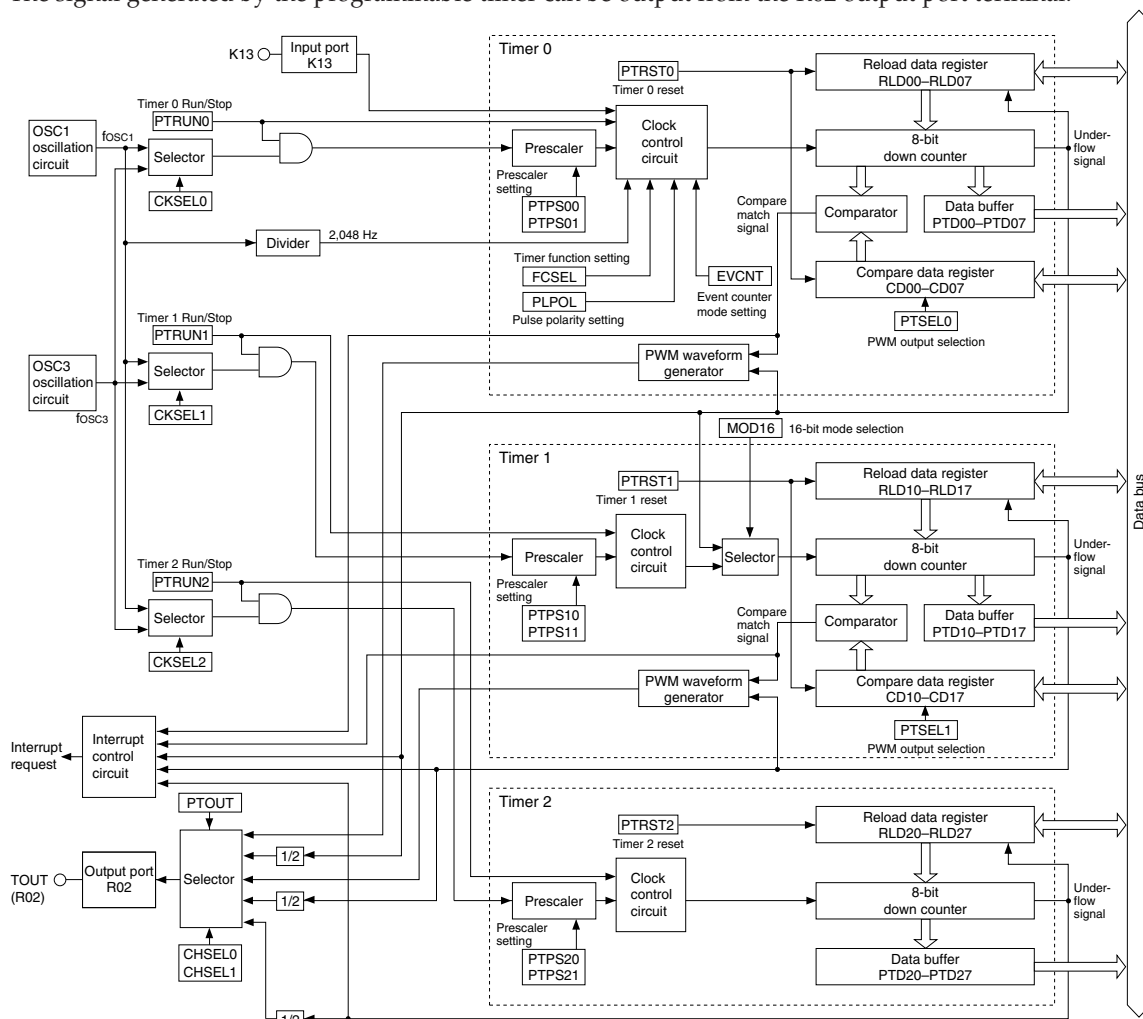


Fig. 4.10.1.1 Configuration of programmable timer

**Note:** If the TOUT terminal is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

### 4.10.2 Basic count operation

This section explains the basic count operation when each timer is used as an individual 8-bit timer.

Each timer has an 8-bit down counter and an 8-bit reload data register.

The reload data register RLDx0–RLDx7 (x = timer number) is used to set the initial value to the down counter.

By writing "1" to the timer reset bit PTRSTx, the down counter loads the initial value set in the reload register. Therefore, down-counting is executed from the stored initial value by the input clock.

The PTRUNx register is provided to control the RUN/STOP for each timer. By writing "1" to this register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffer PTDx0–PTDx7 in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data (PTDx4–PTDx7) when the low-order data (PTDx0–PTDx3) is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register when an underflow occurs through the count down. It continues counting down from the initial value after reloading.

In addition to reloading the counter, this underflow signal controls the interrupt generation and pulse (TOUT signal) output.

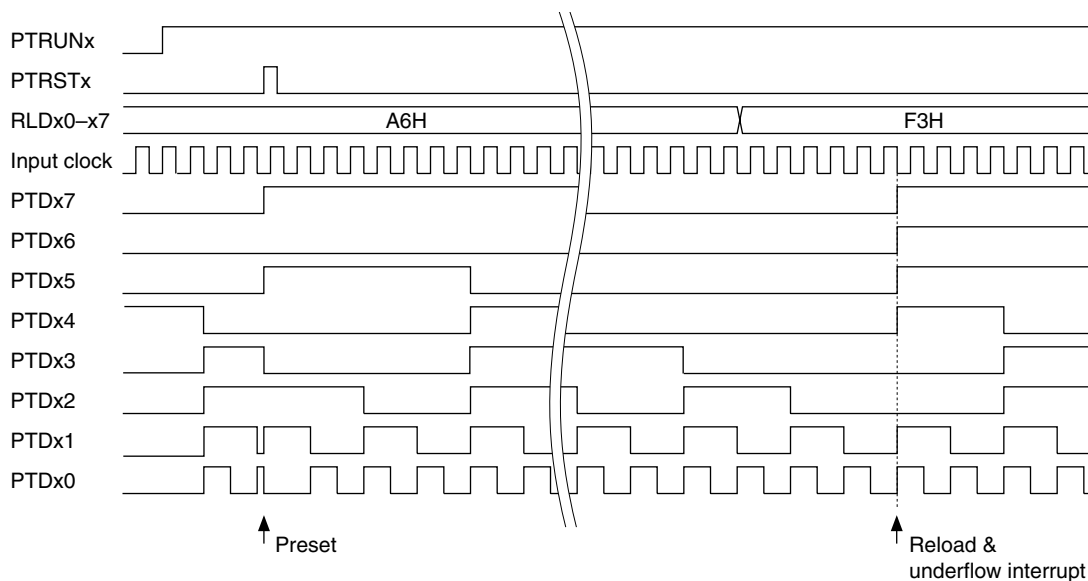


Fig. 4.10.2.1 Basic operation timing of down counter

### 4.10.3 Setting the input clock

A prescaler is provided for each timer. The prescaler generates the input clock for the timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.

The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for each timer individually.

The input clock is set in the following sequence.

#### Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSELx; when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.

When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation on, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit on until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit on to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.

At initial reset, the OSC3 oscillation circuit is set in off state.

#### Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection register PTPSx0/PTPSx1. Table 4.10.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.3.1 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the PTRUNx register, the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

### 4.10.4 Event counter mode (timer 0)

Timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to timer 0 counter mode selection register EVCNT. At initial reset, EVCNT is set to "0" and timer 0 is configured as a normal timer that counts the internal clock.

In the event counter mode, the clock is supplied to timer 0 from outside the IC, therefore, the settings of the timer 0 prescaler division ratio selection register PTPS00–PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.4.1.

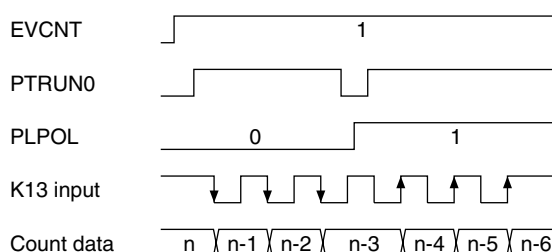


Fig. 4.10.4.1 Timing chart in event counter mode

The event counter mode also allows use of a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.

When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec\* or more to count reliably. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz\* signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec\* or less.

(\*: fosc1 = 32.768 kHz)

Figure 4.10.4.2 shows the count down timing with noise rejector.

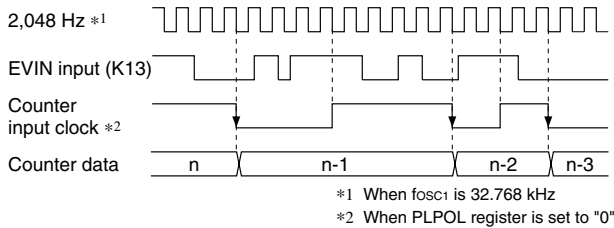


Fig. 4.10.4.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the normal timer except it uses the K13 input as the clock. Refer to Section 4.10.2, "Basic count operation" for basic operation and control.

4.10.5 PWM mode (timer 0, timer 1)

Timer 0 and timer 1 can generate a PWM waveform. When using this function, write "1" to the PTSEL0 register (for timer 0) or PTSEL1 register (for timer 1) to set the timer in the PWM mode.

The compare data register CDx0-CDx7 (x represents a timer number) is provided for timers 0 and 1 to control the PWM waveform. When the timer is set in the PWM mode, the timer compares data between the down counter and the compare data register and outputs the compare match signal if their contents are matched. At the same time a compare match interrupt occurs. Furthermore, the timer output signal rises with the underflow signal and falls with the compare match signal. As shown in Figure 4.10.5.1, the cycle and duty ratio of the output signal can be controlled using the reload data register and the compare data register, respectively, to generate a PWM signal. Note, however, the following condition must be met: RLD (reload data) > CD (compare data) and CD ≠ 0. If RLD ≤ CD, the output signal is fixed at "1" after the first underflow occurs and does not fall to "0".

The generated PWM signal can be output from the R02 output port terminal (see Section 4.10.8).

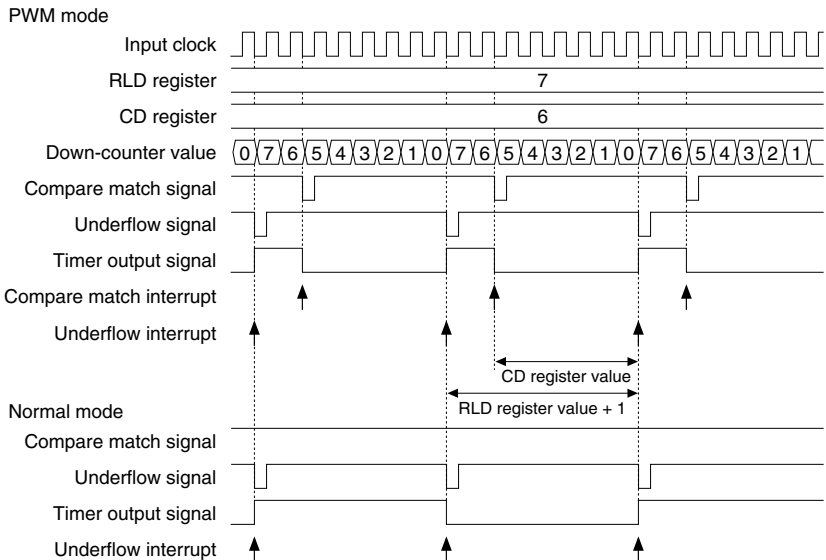


Fig. 4.10.5.1 Generating PWM waveform

### 4.10.6 16-bit timer (timer 0 + timer 1)

Timers 0 and 1 can be used as a 16-bit timer.

To use the 16-bit timer, write "1" to the timer 0 16-bit mode selection register MOD16.

The 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte as shown in Figure 4.10.6.1.

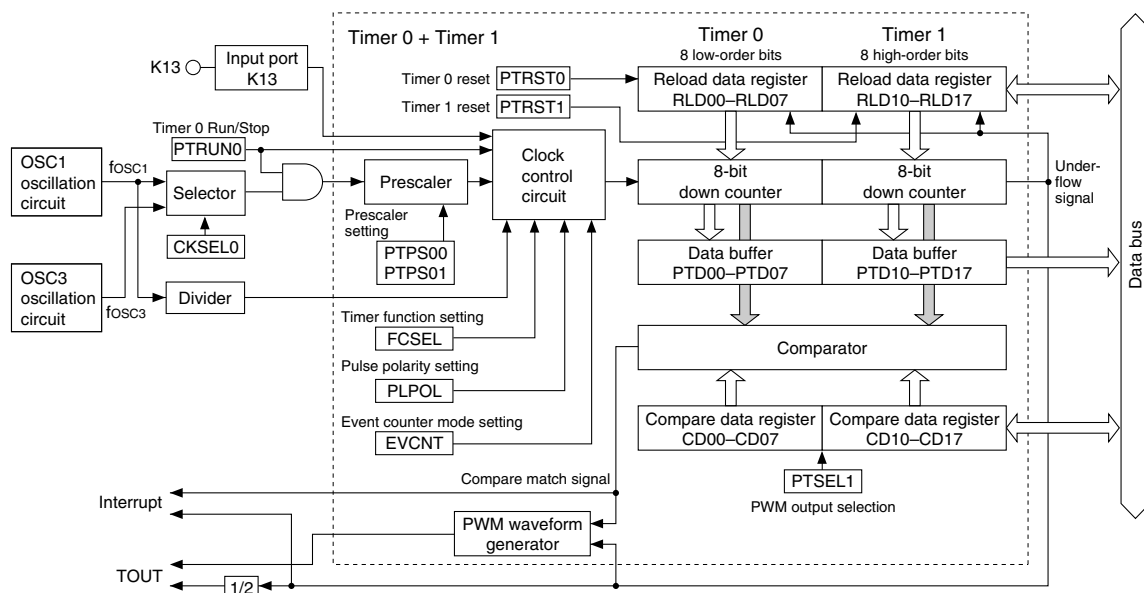


Fig. 4.10.6.1 Configuration of 16-bit timer

The registers for timer 0 are used to control the timer. The event counter and PWM output functions can also be used.

Timer 1 operates with the timer 0 underflow signal as the count clock, so the clock and RUN/STOP control registers for timer 1 become invalid. However, reload data (PTRSTx) must be preset to timers 0 and 1 separately.

The counter data in 16-bit mode must be read in the order below.

PTD00-PTD03 → PTD04-PTD07 → PTD10-PTD13 → PTD14-PTD17

### 4.10.7 Interrupt function

The programmable timer can generate an interrupt due to an underflow of each timer or a compare match of timers 0 and 1. See Figures 4.10.2.1 and 4.10.5.1 for the interrupt timing.

**Note:** The compare match interrupt can be generated only when timer 0 or 1 is set in PWM mode.

An underflow/compare match of timer x sets the corresponding interrupt factor flag IPTx/ICTCx to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPTx/ECTCx. However, the interrupt factor flag is set to "1" by an underflow/compare match of the corresponding timer regardless of the interrupt mask register setting.

When timers 0 and 1 are used as a 16-bit timer, an interrupt is generated by an underflow of timer 1. In this case, IPT0 is not set to "1" by a timer 0 underflow. The compare match interrupt uses ICTC1 of timer 1.

4.10.8 Control of TOUT output

The programmable timer can generate a TOUT signal from the timer underflow and compare match signals. The TOUT signal is generated by dividing the underflow signal by 2 in the normal mode. In the PWM mode, the PWM signal generated by timer 0/1 is output as the TOUT signal. It is possible to select which timer output is to be used by the TOUT output channel selection register CHSEL0–CHSEL1.

Table 4.10.8.1 Selecting a timer for TOUT output

CHSEL1	CHSEL0	TOUT output timer
1	1	None (TOUT is fixed at "1")
1	0	Timer 2
0	1	Timer 1
0	0	Timer 0

Setting CHSEL to "11" does not select a timer and the TOUT output will be fixed at "1". Select timer 1 when generating the TOUT signal from the 16-bit timer output.

The TOUT signal can be output from the R02 output port terminal. Figure 4.10.8.1 shows the configuration of the output port R02.

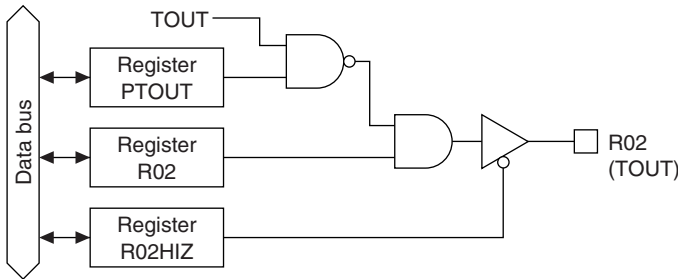


Fig. 4.10.8.1 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register. Figure 4.10.8.2 shows the output waveform of the TOUT signal.

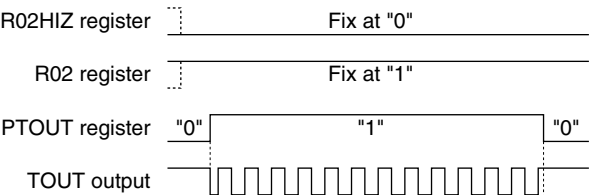


Fig. 4.10.8.2 Output waveform of the TOUT signal

### 4.10.9 I/O memory of programmable timer

Table 4.10.9.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.10.9.1(a) Control bits of programmable timer

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
					FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	0	CHSEL1	CHSEL0	PTOUT	0 *3	– *2			Unused
					CHSEL1	0			] TOUT output selection Timer      Timer 0    Timer 1    Timer 2    Output="1" (fixed)
	R				CHSEL0	0			
					PTOUT	0	On	Off	TOUT output control
FFC2H	0	CKSEL2	CKSEL1	CKSEL0	0 *3	– *2			Unused
					CKSEL2	0	OSC3	OSC1	Prescaler 2 source clock selection
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
	R				CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC3H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			] Prescaler 0 division ratio selection Division ratio    0    1    2    3 1/1    1/4    1/32    1/256
					PTPS00	0			
					PTRST0 *3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC4H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			] Prescaler 1 division ratio selection Division ratio    0    1    2    3 1/1    1/4    1/32    1/256
					PTPS10	0			
					PTRST1 *3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC5H	PTPS21	PTPS20	PTRST2	PTRUN2	PTPS21	0			] Prescaler 2 division ratio selection Division ratio    0    1    2    3 1/1    1/4    1/32    1/256
					PTPS20	0			
					PTRST2 *3	– *2	Reset	Invalid	Timer 2 reset (reload)
					PTRUN2	0	Run	Stop	Timer 2 Run/Stop
FFC6H	RLD03	RLD02	RLD01	RLD00	RLD03	0			] MSB Programmable timer 0 reload data (low-order 4 bits)
					RLD02	0			
					RLD01	0			] LSB Programmable timer 0 reload data (high-order 4 bits)
					RLD00	0			
FFC7H	RLD07	RLD06	RLD05	RLD04	RLD07	0			] MSB Programmable timer 0 reload data (high-order 4 bits)
					RLD06	0			
					RLD05	0			] LSB Programmable timer 1 reload data (low-order 4 bits)
					RLD04	0			
FFC8H	RLD13	RLD12	RLD11	RLD10	RLD13	0			] MSB Programmable timer 1 reload data (high-order 4 bits)
					RLD12	0			
					RLD11	0			] LSB Programmable timer 2 reload data (low-order 4 bits)
					RLD10	0			
FFC9H	RLD17	RLD16	RLD15	RLD14	RLD17	0			] MSB Programmable timer 2 reload data (high-order 4 bits)
					RLD16	0			
					RLD15	0			] LSB Programmable timer 0 data (low-order 4 bits)
					RLD14	0			
FFCAH	RLD23	RLD22	RLD21	RLD20	RLD23	0			] MSB Programmable timer 0 data (high-order 4 bits)
					RLD22	0			
					RLD21	0			] LSB Programmable timer 0 data (high-order 4 bits)
					RLD20	0			
FFCBH	RLD27	RLD26	RLD25	RLD24	RLD27	0			] MSB Programmable timer 0 data (high-order 4 bits)
					RLD26	0			
					RLD25	0			] LSB Programmable timer 0 data (high-order 4 bits)
					RLD24	0			
FFCCH	PTD03	PTD02	PTD01	PTD00	PTD03	0			] MSB Programmable timer 0 data (low-order 4 bits)
					PTD02	0			
					PTD01	0			] LSB Programmable timer 0 data (high-order 4 bits)
					PTD00	0			
FFCDH	PTD07	PTD06	PTD05	PTD04	PTD07	0			] MSB Programmable timer 0 data (high-order 4 bits)
					PTD06	0			
					PTD05	0			] LSB Programmable timer 0 data (high-order 4 bits)
					PTD04	0			

\*1 Initial value at initial reset

\*3 Constantly "0" when being read

\*2 Not set in the circuit

*Table 4.10.9.1(b) Control bits of programmable timer*

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFCEH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB Programmable timer 1 data (low-order 4 bits) LSB
	R				PTD12	0			
					PTD11	0			
					PTD10	0			
FFCFH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB Programmable timer 1 data (high-order 4 bits) LSB
	R				PTD16	0			
					PTD15	0			
					PTD14	0			
FFD0H	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB Programmable timer 2 data (low-order 4 bits) LSB
	R				PTD22	0			
					PTD21	0			
					PTD20	0			
FFD1H	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB Programmable timer 2 data (high-order 4 bits) LSB
	R				PTD26	0			
					PTD25	0			
					PTD24	0			
FFD2H	CD03	CD02	CD01	CD00	CD03	0			MSB Programmable timer 0 compare data (low-order 4 bits) LSB
	R/W				CD02	0			
					CD01	0			
					CD00	0			
FFD3H	CD07	CD06	CD05	CD04	CD07	0			MSB Programmable timer 0 compare data (high-order 4 bits) LSB
	R/W				CD06	0			
					CD05	0			
					CD04	0			
FFD4H	CD13	CD12	CD11	CD10	CD13	0			MSB Programmable timer 1 compare data (low-order 4 bits) LSB
	R/W				CD12	0			
					CD11	0			
					CD10	0			
FFD5H	CD17	CD16	CD15	CD14	CD17	0			MSB Programmable timer 1 compare data (high-order 4 bits) LSB
	R/W				CD16	0			
					CD15	0			
					CD14	0			
FFD8H	0	0	PTSEL1	PTSEL0	0 *3	– *2			Unused Unused Programmable timer 1 PWM output selection Programmable timer 0 PWM output selection
	R		R/W	PTSEL1 PTSEL0	0 *3	– *2			
					0	PWM	Normal		
					0	PWM	Normal		
FFE0H	0	0	ECTC1	ECTC0	0 *3	– *2			Unused Unused Interrupt mask register (Programmable timer 1 compare match) Interrupt mask register (Programmable timer 0 compare match)
	R		R/W	ECTC1 ECTC0	0 *3	– *2			
					0	Enable	Mask		
					0	Enable	Mask		
FFE1H	0	EIPT2	EIPT1	EIPT0	0 *3	– *2			Unused Interrupt mask register (Programmable timer 2 underflow) Interrupt mask register (Programmable timer 1 underflow) Interrupt mask register (Programmable timer 0 underflow)
	R	R/W			EIPT2	0	Enable	Mask	
					EIPT1	0	Enable	Mask	
					EIPT0	0	Enable	Mask	
FFF0H	0	0	ICTC1	ICTC0	0 *3	– *2	(R)	(R)	Unused Unused Interrupt factor flag (Programmable timer 1 compare match) Interrupt factor flag (Programmable timer 0 compare match)
	R		R/W	ICTC1 ICTC0	0 *3	– *2	Yes	No	
					0	(W)	(W)		
					0	Reset	Invalid		
FFF1H	0	IPT2	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused Interrupt factor flag (Programmable timer 2 underflow) Interrupt factor flag (Programmable timer 1 underflow) Interrupt factor flag (Programmable timer 0 underflow)
	R	R/W			IPT2	0	Yes	No	
					IPT1	0	(W)	(W)	
					IPT0	0	Reset	Invalid	

\*1 Initial value at initial reset

\*3 Constantly "0" when being read

\*2 Not set in the circuit



**CKSEL0: Prescaler 0 source clock selection register (FFC2H•D0)****CKSEL1: Prescaler 1 source clock selection register (FFC2H•D1)****CKSEL2: Prescaler 2 source clock selection register (FFC2H•D2)**

Selects the source clock of the prescaler.

When "1" is written: OSC3 clock

When "0" is written: OSC1 clock

Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSELx register, the OSC1 clock is selected as the input clock for the prescaler x (for timer x) and when "1" is written, the OSC3 clock is selected.

When the event counter mode is selected for timer 0, the setting of CKSEL0 becomes invalid.

When timers 0 and 1 are used as a 16-bit timer, the setting of CKSEL1 becomes invalid.

At initial reset, these registers are set to "0".

**PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC3H•D2, D3)****PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC4H•D2, D3)****PTPS20, PTPS21: Timer 2 prescaler division ratio selection register (FFC5H•D2, D3)**

Sets the division ratio of the prescaler as shown in Table 4.10.9.2.

Table 4.10.9.2 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of PTPS00 and PTPS01 becomes invalid.

When timers 0 and 1 are used as a 16-bit timer, the setting of PTPS10 and PTPS11 becomes invalid.

At initial reset, these registers are set to "0".

**MOD16: 16-bit mode selection register (FFC0H•D3)**

Selects whether timers 0 and 1 are used as a 16-bit timer or 2 channels of 8-bit timer.

When "1" is written: 16-bit timer

When "0" is written: 8-bit timer

Reading: Valid

When "1" is written to MOD16, a 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte. Use the timer 0 registers for control. When "0" is written to MOD16, timer 0 and timer 1 are used as independent 8-bit timers.

At initial reset, this register is set to "0".

**EVCNT: Timer 0 counter mode selection register (FFC0H•D2)**

Selects a counter mode for timer 0.

When "1" is written: Event counter mode

When "0" is written: Timer mode

Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.

At initial reset, this register is set to "0".

### FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector

When "0" is written: Without noise rejector

Reading: Valid

When "1" is written to the FCSEL register, the noise rejector is used and counting is done by an external clock (K13) with 0.98 msec\* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz\* signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec\* or less.

(\*: fOSC1 = 32.768 kHz)

When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.

Setting of this register is effective only when timer 0 is used in the event counter mode.

At initial reset, this register is set to "0".

### PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge

When "0" is written: Falling edge

Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K13 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.

Setting of this register is effective only when timer 0 is used in the event counter mode.

At initial reset, this register is set to "0".

### PTSEL0: Timer 0 PWM mode selection register (FFD8H•D0)

### PTSEL1: Timer 1 PWM mode selection register (FFD8H•D1)

Sets timer 0 or 1 for PWM output.

When "1" is written: PWM output

When "0" is written: Normal output

Reading: Valid

When "1" is written to the PTSELx, the compare data register becomes valid and PWM waveform is generated using the underflow and compare match signals. When "0" is written, the timer outputs the normal clock generated from the underflow signal. When timers 0 and 1 are used as a 16-bit timer, the setting of PTSEL1 becomes invalid.

At initial reset, these registers are set to "0".

### RLD00–RLD07: Timer 0 reload data register (FFC6H, FFC7H)

### RLD10–RLD17: Timer 1 reload data register (FFC8H, FFC9H)

### RLD20–RLD27: Timer 2 reload data register (FFCAH, FFCBH)

Sets the initial value for the counter.

The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.

Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRSTx register, or when counter underflow occurs.

At initial reset, these registers are set to "00H".

**PTD00–PTD07: Timer 0 counter data (FFCCH, FFCDH)****PTD10–PTD17: Timer 1 counter data (FFCEH, FFCFH)****PTD20–PTD27: Timer 2 counter data (FFD0H, FFD1H)**

Count data in the programmable timer can be read from these latches.

The low-order 4 bits of the count data in timer x can be read from PTDx0–PTDx3, and the high-order data can be read from PTDx4–PTDx7. Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.

Since these latches are exclusively for reading, the writing operation is invalid.

At initial reset, these counter data are set to "00H".

**CD00–CD07: Timer 0 compare data register (FFD2H, FFD3H)****CD10–CD17: Timer 1 compare data register (FFD4H, FFD5H)**

Set the compare data for PWM output.

When timer 0 or 1 is set in the PWM mode, the compare data set in this register is compared with the counter data and outputs the compare match signal if they are matched. The compare match signal is used for generating an interrupt and controlling the duty ratio of the PWM waveform.

At initial reset, these registers are set to "00H".

**PTRST0: Timer 0 reset (reload) (FFC3H•D1)****PTRST1: Timer 1 reset (reload) (FFC4H•D1)****PTRST2: Timer 2 reset (reload) (FFC5H•D1)**

Resets the timer and presets reload data to the counter.

When "1" is written: Reset

When "0" is written: No operation

Reading: Always "0"

By writing "1" to PTRSTx, the reload data in the reload register RLDx0–RLDx7 is preset to the counter in timer x. When the counter is preset in the RUN status, the counter restarts immediately after presetting.

In the case of STOP status, the reload data is preset to the counter and is maintained.

No operation results when "0" is written.

Since these bits are exclusively for writing, always set to "0" during reading.

**PTRUN0: Timer 0 RUN/STOP control register (FFC3H•D0)****PTRUN1: Timer 1 RUN/STOP control register (FFC4H•D0)****PTRUN2: Timer 2 RUN/STOP control register (FFC5H•D0)**

Controls the RUN/STOP of the counter.

When "1" is written: RUN

When "0" is written: STOP

Reading: Valid

The counter in timer x starts counting down by writing "1" to the PTRUNx register and stops by writing "0". In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.

At initial reset, these registers are set to "0".

**CHSEL0, CHSEL1: TOUT output channel selection register (FFC1H•D1, D2)**

Selects the channel used for TOUT signal output.

*Table 4.10.9.3 Selecting a timer for TOUT output*

CHSEL1	CHSEL0	TOUT output timer
1	1	None (TOUT is fixed at "1")
1	0	Timer 2
0	1	Timer 1
0	0	Timer 0

At initial reset, this register is set to "0".

**PTOUT: TOUT output control register (FFC1H•D0)**

Turns TOUT signal output on and off.

When "1" is written: On  
 When "0" is written: Off  
 Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

At initial reset, this register is set to "0".

**EIPT0, ECTC0: Timer 0 interrupt mask registers (FFE1H•D0, FFE0H•D0)**

**EIPT1, ECTC1: Timer 1 interrupt mask registers (FFE1H•D1, FFE0H•D1)**

**EIPT2: Timer 2 interrupt mask register (FFE1H•D2)**

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled  
 When "0" is written: Masked  
 Reading: Valid

EIPTx and ECTCx are the interrupt mask registers that respectively correspond to the counter underflow and compare match interrupt factors. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.

At initial reset, these registers are set to "0".

**IPT0, ICTC0: Timer 0 interrupt factor flags (FFF1H•D0, FFF0H•D0)**

**IPT1, ICTC1: Timer 1 interrupt factor flags (FFF1H•D1, FFF0H•D1)**

**IPT2: Timer 2 interrupt factor flag (FFF1H•D2)**

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred  
 When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset  
 When "0" is written: Invalid

IPTx and ICTCx are the interrupt factor flags that respectively correspond to the interrupts for counter underflow and compare match, and are set to "1" by generation of each factor.

The underflow interrupt factor is generated at the point where the counter underflows.

The compare match interrupt factor is generated if the counter data and the compare data are matched when timer 0 or timer 1 is set in the PWM mode.

The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by an underflow and compare match of the corresponding counter.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

### 4.10.10 Programming notes

- (1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) are not latched when the low-order 4 bits are read. Therefore, the high-order 4 bits should be read within 0.73 msec (when  $f_{OSC1}$  is 32.768 kHz) from reading the low-order 4 bits. When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data. The counter running with OSC3 counts down for the value listed in Table 4.10.10.1 while the CPU running with OSC1 reads the low-order 4 bits and high-order 4 bits of the counter data by two instructions.

Table 4.10.10.1 Counter change with OSC3 between readings low-order and high-order data with OSC1

Count clock	Counter change between reading
OSC3/1	0200H
OSC3/4	001AH
OSC3/32	0002H

In 16-bit mode, the counter data must be read in the order below.

PTD00–PTD03 → PTD04–PTD07 → PTD10–PTD13 → PTD14–PTD17

- (2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.

Figure 4.10.10.1 shows the timing chart for the RUN/STOP control.

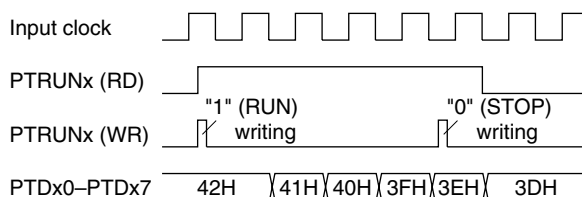


Fig. 4.10.10.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

- (3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
- (4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.
- (5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

- (6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.

The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

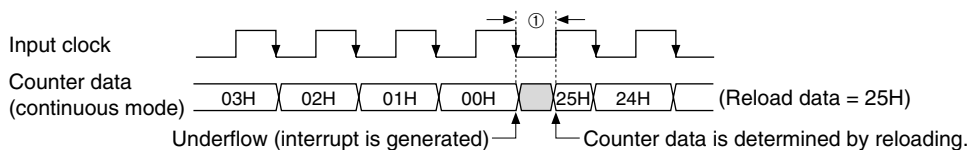


Fig. 4.10.10.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

## 4.11 Sound Generator

### 4.11.1 Configuration of sound generator

The S1C63657 has a built-in sound generator for generating buzzer signals. Hence, generated buzzer signals can be output from the BZ and  $\overline{\text{BZ}}$  (BZ inverted output) terminals. Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.

Figure 4.11.1.1 shows the configuration of the sound generator.

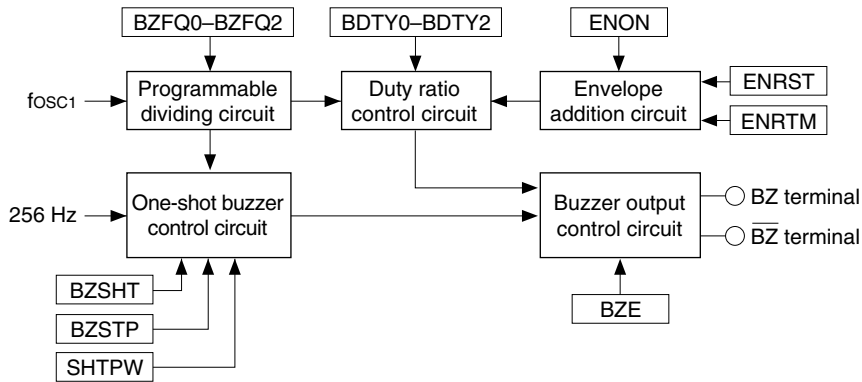


Fig. 4.11.1.1 Configuration of sound generator

**Note:** If the BZ terminal is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to <Output Terminals> in Section 5.3, "Precautions on Mounting", for more information.

### 4.11.2 Control of buzzer output

The BZ and  $\overline{\text{BZ}}$  signals generated by the sound generator are output from the BZ and  $\overline{\text{BZ}}$  terminals by setting "1" for the buzzer output enable register BZE. When "0" is set to BZE register, the BZ terminal goes low (Vss) and the  $\overline{\text{BZ}}$  terminal goes high (VDD).

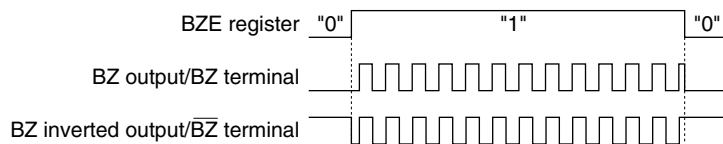


Fig. 4.11.2.1 Buzzer signal output timing chart

**Note:** Since it generates the buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

### 4.11.3 Setting of buzzer frequency and sound level

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency selection registers BZFQ0–BZFQ2 as shown in Table 4.11.3.1.

Table 4.11.3.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.

The duty ratio can be selected from among the 8 types shown in Table 4.11.3.2 according to the setting of the buzzer duty selection registers BDTY0–BDTY2.

Table 4.11.3.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

When the high level output time has been made TH and when the low level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes  $TH/(TH+TL)$  for the BZ output or  $TL/(TH+TL)$  for the  $\overline{BZ}$  output.

When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.

The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.11.3.2.

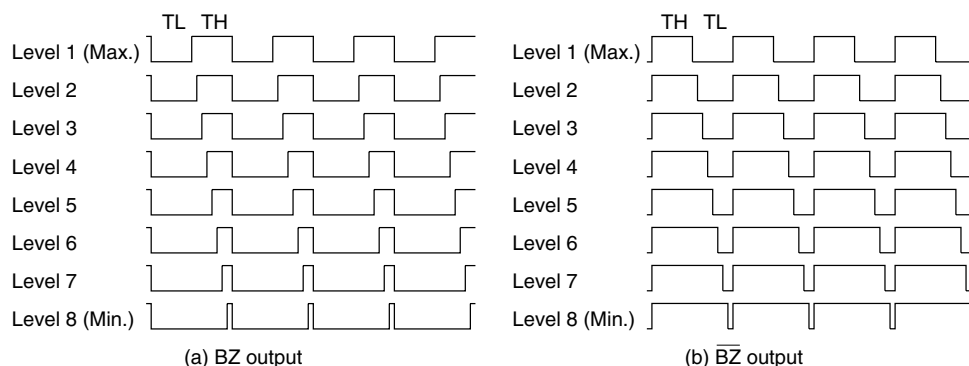


Fig. 4.11.3.1 Duty ratio of the buzzer signal waveform

**Note:** When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.



#### 4.11.4 Digital envelope

A digital envelope for duty control can be added to the buzzer signal.

The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.11.3.2 in the preceding item from level 1 (maximum) to level 8 (minimum).

The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.

When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8.

When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal.

The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.

Figure 4.11.4.1 shows the timing chart of the digital envelope.

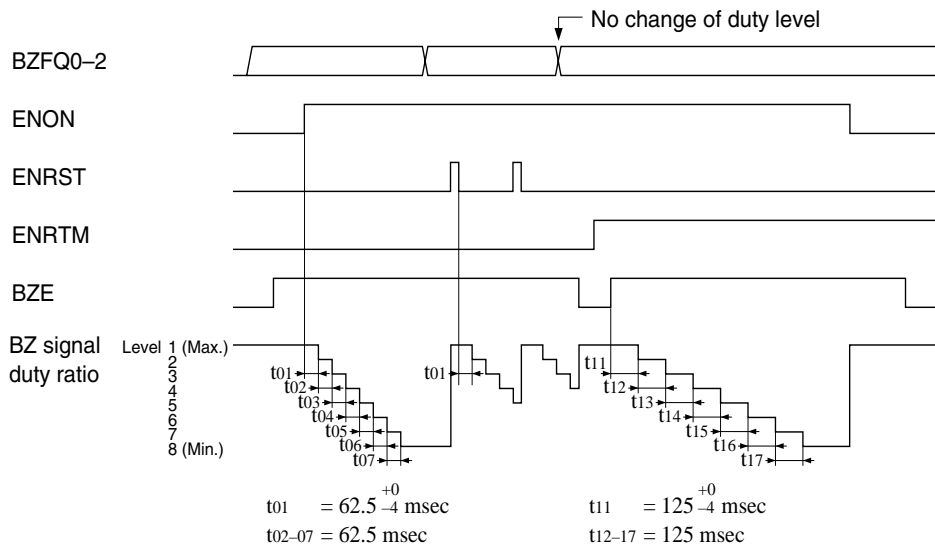


Fig. 4.11.4.1 Timing chart for digital envelope

### 4.11.5 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.

The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the buzzer output terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output. The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes off in synchronization with the 256 Hz signal.

When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.

One-shot output is invalid during normal buzzer output (during BZE = "1").

Figure 4.11.5.1 shows timing chart for one-shot output.

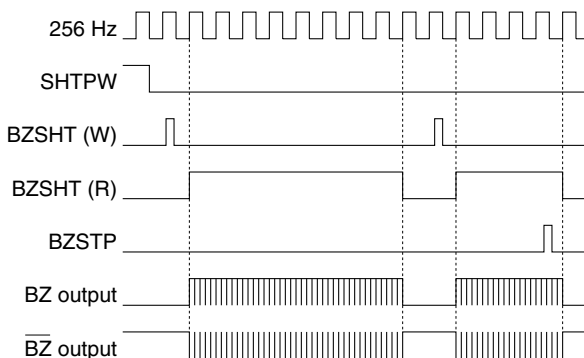


Fig. 4.11.5.1 Timing chart for one-shot output

### 4.11.6 I/O memory of sound generator

Table 4.11.6.1 shows the I/O addresses and the control bits for the sound generator.

Table 4.11.6.1 Control bits of sound generator

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
					ENON	0	On	Off	Envelope On/Off
	R/W	W	R/W		BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W		SHTPW	0	Busy	Ready	1-shot buzzer status (reading)
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
	R	R/W			BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
					BDTY1	0			
	R	R/W			BDTY0	0			

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### BZE: Buzzer output control register (FF6CH•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On

When "0" is written: Buzzer output Off

Reading: Valid

When "1" is written to BZE, the BZ and  $\overline{\text{BZ}}$  signals are output from the BZ and  $\overline{\text{BZ}}$  terminals, respectively.

When "0" is written, the BZ terminal goes to low (VSS) and the  $\overline{\text{BZ}}$  terminal goes high (VDD).

At initial reset, this register is set to "0".

#### BZFQ0–BZFQ2: Buzzer frequency selection register (FF6EH•D0–D2)

Selects the buzzer signal frequency.

Table 4.11.6.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock.

At initial reset, this register is set to "0".

**BDTY0–BDTY2: Duty level selection register (FF6FH•D0–D2)**

Selects the duty ratio of the buzzer signal as shown in Table 4.11.6.3.

Table 4.11.6.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.

However, when the envelope has been set to on (ENON = "1"), this setting becomes invalid.

At initial reset, this register is set to "0".

**ENRST: Envelope reset (FF6CH•D2)**

Resets the envelope.

When "1" is written: Reset

When "0" is written: No operation

Reading: Always "0"

Writing "1" into ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.

This bit is dedicated for writing, and is always "0" for reading.

**ENON: Envelope On/Off control register (FF6CH•D1)**

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: On

When "0" is written: Off

Reading: Valid

Writing "1" into the ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.

At initial reset, this register is set to "0".

**ENRTM: Envelope releasing time selection register (FF6CH•D3)**

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)

When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)

Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.

When "1" has been written in ENRTM, it becomes 125 msec (8 Hz) units and when "0" has been written, it becomes 62.5 msec (16 Hz) units.

At initial reset, this register is set to "0".

**SHTPW: One-shot buzzer pulse width setting register (FF6DH•D0)**

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec

When "0" is written: 31.25 msec

Reading: Valid

Writing "1" into SHTPW causes the one-shot output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.

At initial reset, this register is set to "0".

**BZSHT: One-shot buzzer trigger/status (FF6DH•D1)**

Controls the one-shot buzzer output.

**• When writing**

When "1" is written: Trigger

When "0" is written: No operation

Writing "1" into BZSHT causes the one-shot output circuit to operate and a buzzer signal to be output. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

**• When reading**

When "1" is read: BUSY

When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".

At initial reset, this bit is set to "0".

**BZSTP: One-shot buzzer stop (FF6DH•D2)**

Stops the one-shot buzzer output.

When "1" is written: Stop

When "0" is written: No operation

Reading: Always "0"

Writing "1" into BZSTP permits the one-shot buzzer output to be turned off prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

**4.11.7 Programming notes**

- (1) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.
- (2) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

## 4.12 Integer Multiplier

### 4.12.1 Configuration of integer multiplier

The S1C63657 has a built-in unsigned-integer multiplier. This multiplier performs 8 bits × 8 bits of multiplication or 16 bits ÷ 8 bits of division and returns the results and three flag states.

Figure 4.12.1.1 shows the configuration of the integer multiplier.

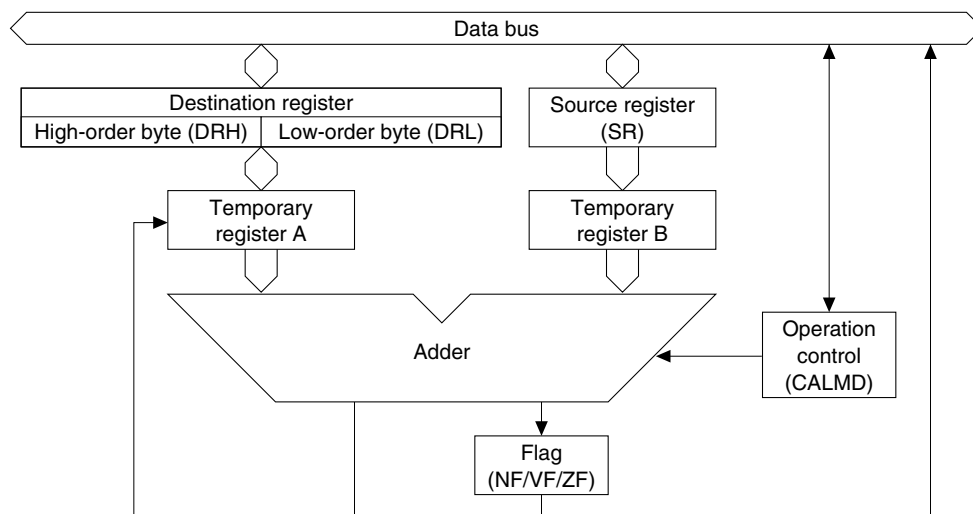


Fig. 4.12.1.1 Configuration of the integer multiplier

### 4.12.2 Multiplication mode

To perform a multiplication, set the multiplier to the source register (SR) and the multiplicand to the low-order 8 bits (DRL) of the destination register, then write "0" to the calculation mode selection register (CALMD). The multiplication takes 10 CPU clock cycles from writing "0" to CALMD until the 16-bit product is loaded into the destination register (DRH and DRL). At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.

The following shows the conditions that change the operation flag states and examples of multiplication.

**N flag:** Set when the MSB of DRH is "1" and reset when it is "0".

**V flag:** Always reset after a multiplication.

**Z flag:** Set when the 16-bit value in DRH/DRL is 0000H and reset when it is not 0000H.

#### <Examples of multiplication>

DRL (multiplicand)	SR (multiplier)	DRH/DRL (product)	NF	VF	ZF
00H	64H	0000H	0	0	1
64H	58H	2260H	0	0	0
C8H	58H	44C0H	0	0	0
C8H	A5H	80E8H	1	0	0

### 4.12.3 Division mode

To perform a division, set the divisor to the source register (SR) and the dividend to the destination register (DRH and DRL), then write "1" to the calculation mode selection register (CALMD). The division takes 10 CPU clock cycles from writing "1" to CALMD until the quotient is loaded into the low-order 8 bits (DRL) of the destination register and the remainder is loaded into the high-order 8 bits (DRH) of the destination register. At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated.

However, when an overflow results (if the quotient exceeds the 8-bit range), the destination register (DRH and DRL) does not change its contents as it maintains the dividend.

The following shows the conditions that change the operation flag states and examples of division.

**N flag:** Set when the MSB of DRL is "1" and reset when it is "0".

**V flag:** Set when the quotient exceeds the 8-bit range and reset when it is within the 8-bit range.

**Z flag:** Set when the 8-bit value in DRL is 00H and reset when it is not 00H.

#### <Examples of division>

<u>DRH/DRL (dividend)</u>	<u>SR (divisor)</u>	<u>DRL (quotient)</u>	<u>DRH (remainder)</u>	<u>NF</u>	<u>VF</u>	<u>ZF</u>
1A16H	64H	42H	4EH	0	0	0
332CH	64H	83H	00H	1	0	0
0000H	58H	00H	00H	0	0	1
2468H	13H	68H	24H	1	1	0

In the example of "2468H" ÷ "13H" shown above, DRH/DRL maintains the dividend because the quotient overflows the 8-bit. To get the correct results when an overflow has occurred, perform the division with two steps as shown below.

1. Divide the high-order 8 bits of the dividend (24H) by the divisor (13H) and then store the quotient (01H) to memory.

<u>DRH/DRL (dividend)</u>	<u>SR (divisor)</u>	<u>DRL (quotient)</u>	<u>DRH (remainder)</u>	<u>NF</u>	<u>VF</u>	<u>ZF</u>
0024H	13H	01H	11H	0	0	0

2. Keep the remainder (11H) in DRH and load the low-order 8 bits of the dividend (68H) to DRL, then perform division again.

<u>DRH/DRL (dividend)</u>	<u>SR (divisor)</u>	<u>DRL (quotient)</u>	<u>DRH (remainder)</u>	<u>NF</u>	<u>VF</u>	<u>ZF</u>
1168H	13H	EAH	0AH	1	0	0

The correct result is obtained as the quotient = 01EAH (the first and second results of DRL are merged) and the remainder = 0AH. However, since the operation flags (NF/VF/ZF) are changed in each step, they cannot indicate the states according to the final operation results.

*Note: Make sure that the division results are correct using software as the hardware does not check.*

#### 4.12.4 Execution cycle

Both the multiplication and division take 10 CPU cycles for an operation. Therefore, before the results can be read from the destination register DRH/DRL, wait at least 5 bus cycles after writing to CALMD. The same applies to reading the operation flags NF/VF/ZF.

The following shows a sample program.

```

    ldb  %ext, src_data@h
    ldb  %xl, src_data@l      ; Set RAM address for operand
    ldb  %ext, au@h
    ldb  %yl, au@l            ; Set multiplier I/O memory address
;
    ldb  %ba, [%x]+
    ldb  [%y]+, %ba            ; Set data to SR
    ldb  %ba, [%x]+
    ldb  [%y]+, %ba            ; Set data to DRL
    ldb  %ba, [%x]+
    ldb  [%y]+, %ba            ; Set data to DRH
;
    ld   [%y], 0b0001          ; Start operation (select calculation mode)
;
    ldb  %ext, rslt_data@h
    ldb  %xl, rslt_data@l      ; Set result store address
    nop
    nop
    nop                        ; Dummy instructions to wait end of operation
;
    bit  [%y], 0b0100
    jrnz overflow              ; Jump to error routine if VF = "1"
;
    add  %y, -4                 ; Set DRL again
;
    ldb  %ba, [%y]+
    ldb  [%x]+, %ba             ; Store result (quotient) into RAM
    ldb  %ba, [%y]+
    ldb  [%x]+, %ba             ; Store result (remainder) into RAM

```



### 4.12.5 I/O memory of integer multiplier

Table 4.12.5.1 shows the I/O addresses and the control bits for the integer multiplier.

Table 4.12.5.1 Control bits of integer multiplier

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF80H	SR3	SR2	SR1	SR0	SR3	– *2			Source register (low-order 4 bits) LSB
					SR2	– *2			
	R/W				SR1	– *2			
					SR0	– *2			
FF81H	SR7	SR6	SR5	SR4	SR7	– *2			Source register (high-order 4 bits) MSB
					SR6	– *2			
	R/W				SR5	– *2			
					SR4	– *2			
FF82H	DRL3	DRL2	DRL1	DRL0	DRL3	– *2			Low-order 8-bit destination register (low-order 4 bits) LSB
					DRL2	– *2			
	R/W				DRL1	– *2			
					DRL0	– *2			
FF83H	DRL7	DRL6	DRL5	DRL4	DRL7	– *2			Low-order 8-bit destination register (high-order 4 bits) MSB
					DRL6	– *2			
	R/W				DRL5	– *2			
					DRL4	– *2			
FF84H	DRH3	DRH2	DRH1	DRH0	DRH3	– *2			High-order 8-bit destination register (low-order 4 bits) LSB
					DRH2	– *2			
	R/W				DRH1	– *2			
					DRH0	– *2			
FF85H	DRH7	DRH6	DRH5	DRH4	DRH7	– *2			High-order 8-bit destination register (high-order 4 bits) MSB
					DRH6	– *2			
	R/W				DRH5	– *2			
					DRH4	– *2			
FF86H	NF	VF	ZF	CALMD	NF	0	Negative	Positive	Negative flag
					VF	0	Overflow	No	Overflow flag
	R			R/W	ZF	0	Zero	No	Zero flag
					CALMD	0	Run	Stop	Operation status (reading)
							Div.	Mult.	Calculation mode selection (writing)

\*1 Initial value at initial reset

\*2 Not set in the circuit

\*3 Constantly "0" when being read

#### SR0–SR7: Source register (FF80H, FF81H)

Used to set multipliers and divisors.

Set the low-order 4 bits of data to SR0–SR3 and the high-order 4 bits to SR4–SR7.

This register maintains the latest set value until the next writing, so it is not necessary to set data for each operation if the same multiplier and divisor is used in a series of operations.

At initial reset, this register is undefined.

#### DRL0–DRL7: Destination register low-order 8 bits (FF82H, FF83H)

Used to set multiplicands and low-order 8 bits of dividends.

Set the low-order 4 bits of data to DRL0–DRL3 and the high-order 4 bits to DRL4–DRL7.

Data written to this register is loaded to the arithmetic circuit when an operation starts (by writing to FF86H•D0), and then a multiplication or a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the low-order 8 bits of the product or the quotient are loaded to this register.

However, if an overflow occurs in a division process, the quotient is not loaded and the low-order 8 bits of the dividend remains.

At initial reset, this register is undefined.

**DRH0–DRH7: Destination register high-order 8 bits (FF84H, FF85H)**

Used to set high-order 8 bits of dividends.

Set the low-order 4 bits of data to DRH0–DRH3 and the high-order 4 bits to DRH4–DRH7.

At the start of a multiplication (by writing "0" to FF86H•D0), the contents in this register are ignored. After 10 CPU cycles (5 bus cycles) of multiplication process has finished, the high-order 8 bits of the product are loaded in this register.

In a division process, data written to this register is loaded to the arithmetic circuit when an operation starts (by writing "1" to FF86H•D0), and then a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the remainder is loaded to this register. However, if an overflow occurs in a division process, the remainder is not loaded and the high-order 8 bits of the dividend remains. At initial reset, this register is undefined.

**NF: Negative flag (FF86H•D3)**

Indicates whether the operation result is a positive value or a negative value.

When "1" is read: Negative value (MSB of the results is "1")

When "0" is read: Positive value (MSB of the results is "0")

Writing: Invalid

NF is a read-only bit, so writing operation is invalid.

At initial reset, this flag is set to "0".

**VF: Overflow flag (FF86H•D2)**

Indicates whether an overflow has occurred or not in a division process.

When "1" is read: Overflow occurred

When "0" is read: Overflow has not occurred

Writing: Invalid

When a multiplication process has finished, this flag is always set to "0".

VF is a read-only bit, so writing operation is invalid.

At initial reset, this flag is set to "0".

**ZF: Zero flag (FF86H•D1)**

Indicates whether the operation result is zero or not.

When "1" is read: Zero

When "0" is read: Not zero

Writing: Invalid

ZF is a read-only bit, so writing operation is invalid.

At initial reset, this flag is set to "0".

**CALMD: Calculation mode selection register/operation status (FF86H•D0)**

Selects multiplication or division mode and starts operation.

When "1" is written: Selects/starts division

When "0" is written: Selects/starts multiplication

When "1" is read: Under operating

When "0" is read: Operation has finished

Writing to this register starts the specified operation. After that, this register is set to "1" and returns to "0" when the multiplication or division process has finished.

At initial reset, this register is reset to "0".

**4.12.6 Programming note**

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode selection register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation is in process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

## 4.13 R/f Converter

### 4.13.1 Configuration of R/f converter

The S1C63657 has a CR oscillation type R/f converter.

Two systems (channel 0 and channel 1) of CR oscillation circuit are built into this R/f converter, so it is possible to compose two types of R/f conversion circuits by connecting different sensors to each CR oscillation circuit.

Channel 0 can be used as an R/f conversion circuit using a resistive sensor such as a thermistor, and channel 1 can be used as an R/f conversion circuit same as channel 0, or an R/f conversion circuit for humidity conversion using a resistive humidity sensor.

The channel to be used and sensor type for channel 1 are selected using software.

Resistance value (relative value to external reference resistance) of the resistive sensor that has been connected to the sensor input terminal is converted into frequency by the CR oscillation circuit and the number of clocks is counted in the built-in measurement counter. By reading the value of the measurement counter, it can obtain the data after digitally-converting the value detected by the sensor.

Various sensor circuits such as temperature/humidity measurement circuits can be easily realized using this R/f converter.

The configuration of the R/f converter is shown in Figure 4.13.1.1.

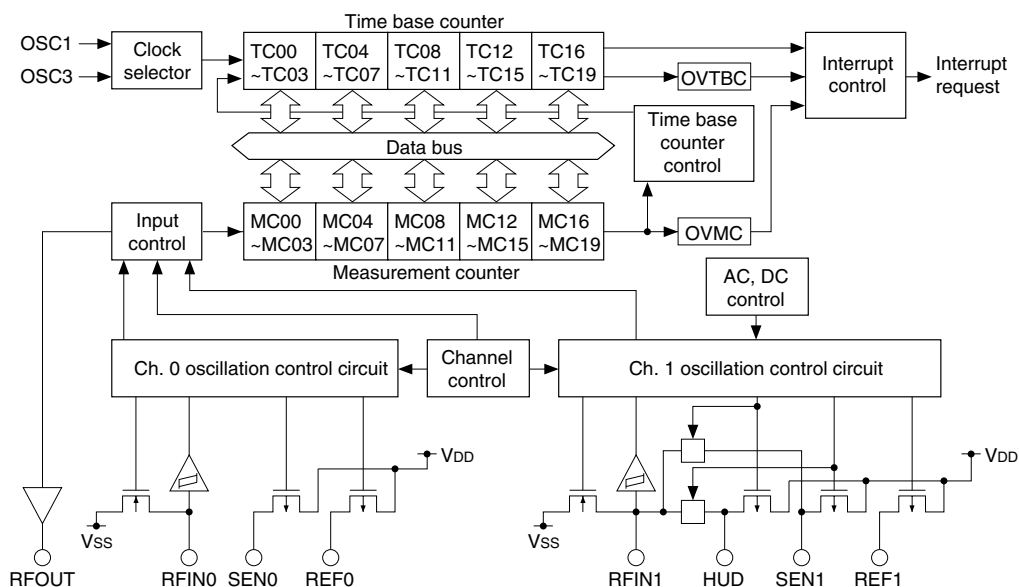


Fig. 4.13.1.1 Configuration of R/f converter

### 4.13.2 Connection terminals and CR oscillation circuit

Two systems of CR oscillation circuit, channel 0 and channel 1, are built into the R/f converter and perform CR oscillation with external resistor and capacitor.

The counter that is used to obtain an R/f converted value is shared with channel 0 and channel 1. Therefore, operation for two systems is realized by switching the CR oscillation circuit that performs R/f conversion. The channel selection is done using the register SENSEL. When SENSEL is set to "0", channel 0 is selected and when "1" is set, channel 1 is selected.

The sensor type to be R/f converted in the channel 1 can also be selected by the software, and it should be previously set using the register RFSEL.

**Channel selection**                      SENSEL = "0": Channel 0  
    SENSEL = "1": Channel 1

**Sensor selection for channel 1**    RFSEL = "0": R/f conversion using a resistive sensor such as thermistor  
    RFSEL = "1": R/f conversion using a resistive humidity sensor \*

\* The operation of the oscillation circuit differs from the normal resistive sensor. (Refer to the following.)

#### (1) R/f conversion using a resistive sensor such as thermistor

Channel 0 is set only for this conversion method, and channel 1 is selected into this method by setting RFSEL to "0". This method should be selected for R/f conversion using a normal resistive sensor (DC bias), such as temperature measurement using thermistor. At initial reset, channel 1 is set into this conversion method.

Figure 4.13.2.1 shows the connection diagram of external elements.

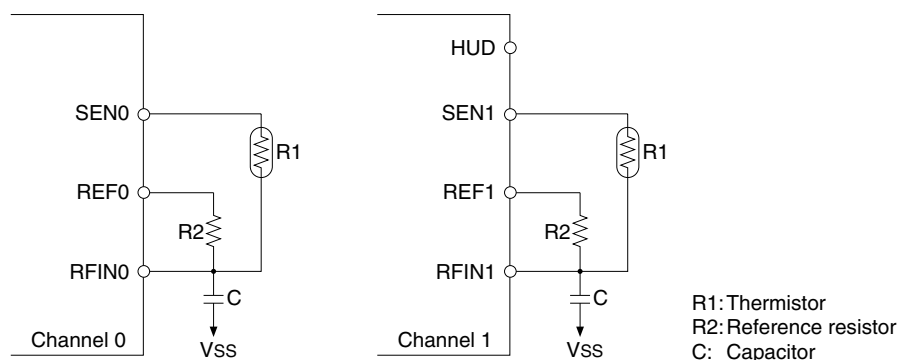


Fig. 4.13.2.1 Connection diagram in case of R/f conversion

Connect a resistive sensor (such as a thermistor) between the SEN0 (SEN1) and RFIN0 (RFIN1) terminals.

Next, set the reference value of the item to be measured (e.g. reference temperature in the case of temperature measurement) and connect the reference resistance equivalent to the sensor resistance value at the above reference value between the REF0 (REF1) and RFIN0 (RFIN1) terminals. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.

Connect an oscillating capacitor that is used for CR oscillation of both the reference resistance and the sensor between the RFIN0 (RFIN1) and Vss terminals.

The HUD terminal should be opened because it is not used in this method.

The R/f converter performs CR oscillation using each of the two resistances (sensor and reference resistance) in the same period, and counts the CR oscillation clock. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program.

The CR oscillation circuit is designed so that either the reference resistance side or the sensor side can be operated independently by the oscillation control circuit.

Each circuit performs the same oscillating operation as follows:

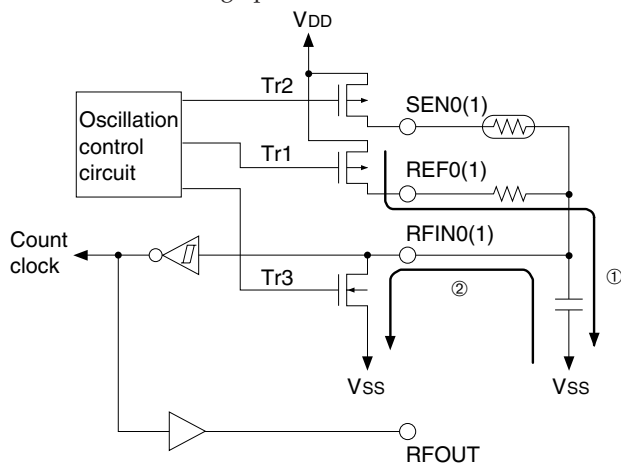


Fig. 4.13.2.2 CR oscillation circuit (DC bias)

The Tr1 (Tr2) turns on first, and the capacitor connected between the REF (SEN) and VSS terminals is charged through the reference resistance (sensor). If the voltage level of the RFIN terminal decreases, the Tr1 (Tr2) turns off and the Tr3 turns on. As a result, the capacitor becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

Oscillation waveforms are shaped by the schmitt trigger and transmitted to the measurement counter. The clock transmitted to the measurement counter is also output from the RFOUT terminal while the sensor is oscillating. As a result, oscillation frequency can be identified by the oscilloscope. Since this monitor has no effect on oscillation frequency, it can be used to adjust R/f conversion accuracy.

Oscillation waveforms and waveforms output from the RFOUT terminal are shown in Figure 4.13.2.3. The "L" pulse width of the RFOUT output must be 10  $\mu\text{sec}$  or more (when  $V_{DD} = 3.0\text{ V}$ ,  $R_{SEN0/1} = 50\text{ k}\Omega$ ,  $C_{RF} = 1000\text{ pF}$ ).

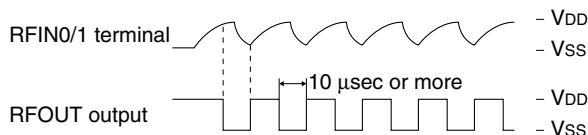


Fig. 4.13.2.3 Oscillation waveform

**(2) R/f conversion using a resistive humidity sensor**

This conversion is possible only in channel 1, and this method is selected by setting the RFSEL register to "1". This is basically the same as the R/f conversion described above (1), but the AC bias circuit works for the humidity sensor.

Figure 4.13.2.4 shows the connection diagram of external devices.

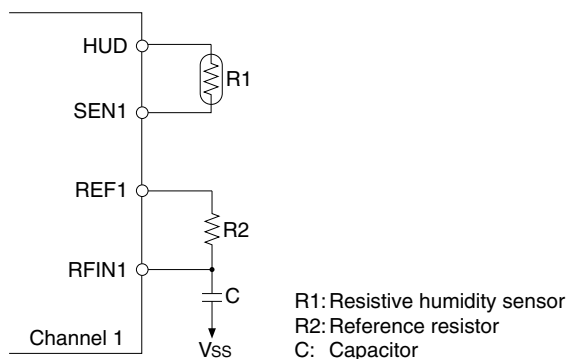


Fig. 4.13.2.4 Connection diagram of resistive humidity sensor

Connect a humidity sensor between the HUD and SEN1 terminals, and connect a reference resistance between the REF1 and RFIN1 terminals.

Connect an oscillating capacitor that is used for CR oscillation of both the reference resistance and the sensor between the RFIN1 and Vss terminals.

The oscillating operation by reference resistance is the same as the R/f conversion described above (1). The humidity sensor cannot be DC biased for a long time, therefore this method powers the HUD and SEN1 terminals alternately.

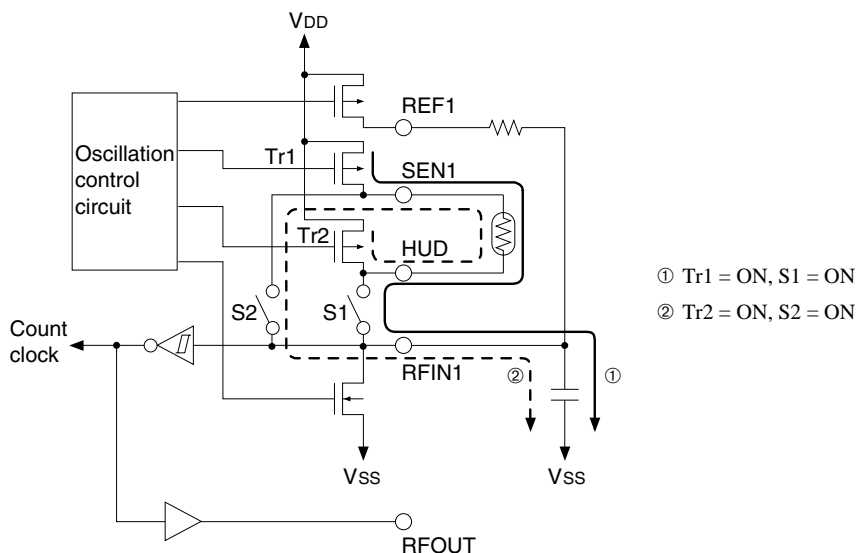


Fig. 4.13.2.5 CR oscillation circuit for resistive humidity sensor

The oscillation waveform is the same as Figure 4.13.2.3.

### 4.13.3 Operation of R/f conversion

#### Counter

The R/f converter incorporates two types of counters: measurement counter MCxx and time base counter TCxx. The measurement counter is a 20-bit up counter that counts the CR oscillation clock with the reference resistance or sensor selected by software. The time base counter is a 20-bit up/down counter to equal both oscillation times for the reference resistance and the sensor. The time base counter uses the count clock selected by the RFCLK register (OSC1 or OSC3). Each counter permits reading and writing on a 4-bit basis.

First start an R/f conversion for the reference resistance. The measurement counter starts counting up and the time base counter starts counting down. The counters stop counting when the measurement counter overflows (counter = 00000H). By resetting the time base counter to 00000H before starting an R/f conversion for the reference resistance, the reference oscillation time will be obtained from the time base counter.

Then start an R/f conversion for the sensor, the measurement counter starts counting up from 00000H and the time base counter starts counting up from the counted value. The counters stop counting when the time base counter overflows (counter = 00000H). The oscillation time in this phase is the same as that of the reference resistance.

Therefore, by converting a proper initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from 00000H) and setting it into the measurement counter before starting to count, the number of counts for the sensor oscillation is obtained by reading the measurement counter after the R/f conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result.

The time base counter allows reading of the counter value and presetting of data. By saving the counter value after the reference oscillation has completed into the RAM, the subsequent reference oscillation phase can be omitted. The sensor oscillation can be started after setting the saved value to the time base counter and 00000H to the measurement counter.

*Note: When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF92H → FF93H → FF94H → FF95H → FF96H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.*

#### R/f conversion sequence

An R/f conversion for the reference resistance starts by writing "1" to the register RFRUNR.

However, an initial value must be set to the measurement counter and the time base counter must be cleared to 00000H before starting the R/f conversion.

When R/f conversion is initiated by the RFRUNR register, oscillation by the reference resistance begins, and the measurement counter starts counting up from the initial value by the oscillation clock. The time base counter also starts counting down by the OSC1 clock.

If the measurement counter becomes 00000H due to overflow, the oscillation is terminated. At the same time an interrupt occurs and the RFRUNR register is set to "0", and the R/f converter circuit stops operation completely.

The time base counter value should be saved into the RAM for R/f conversion of the sensor.

Figure 4.13.3.1 shows a timing chart for the reference oscillation.

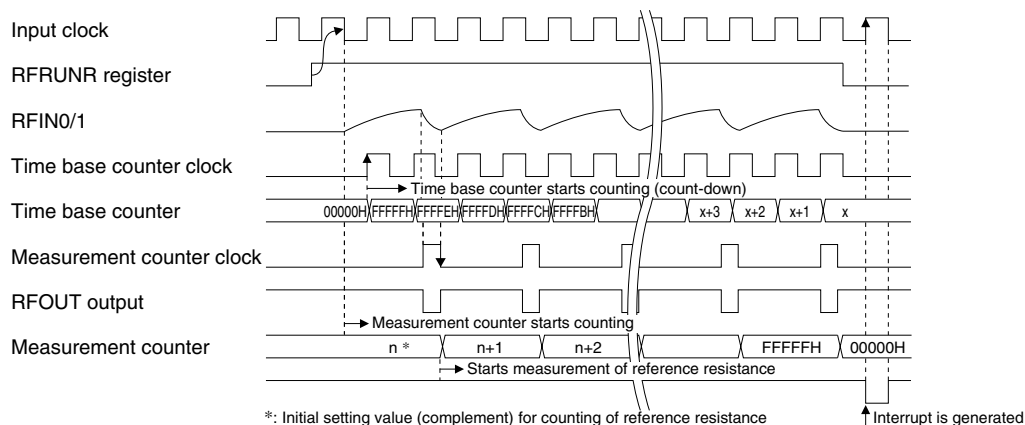


Fig. 4.13.3.1 Reference oscillation timing chart

CR oscillation starts in synchronization with the falling edge of the input clock immediately after writing "1" to the RFRUNR register. The measurement counter starts counting up at the falling edge of the first clock after CR oscillation is initiated. The time base counter is enabled at the falling edge of the first input clock. Then, it counts down by the rising edge of the input clock. The RFRUNR register is set to "0" at the falling edge of the input clock immediately after the measurement counter stops. Interrupt conditions are sampled with the OSC1 clock, so an interrupt occurs in synchronization with the rising edge of the OSC1 clock immediately after the RFRUNR register is set to "0".

An R/f conversion for the sensor starts by writing "1" to the register RFRUNS. When performing this sensor oscillation after an reference oscillation has completed, it is not necessary to set initial values to the counters. If converting the sensor resistance independently, the measurement counter must be set to 00000H and the time base counter must be set to the value measured at the time of a reference oscillation. When R/f conversion is initiated by the RFRUNS register, oscillation by the sensor begins, and the measurement counter starts counting up from 00000H by the oscillation clock. The time base counter also starts counting up by the input clock. If the time base counter becomes 00000H, the oscillation is terminated. At the same time an interrupt occurs and the RFRUNS register is set to "0", and the R/f converter circuit stops operation completely.

Figure 4.13.3.2 shows a timing chart for the sensor oscillation.

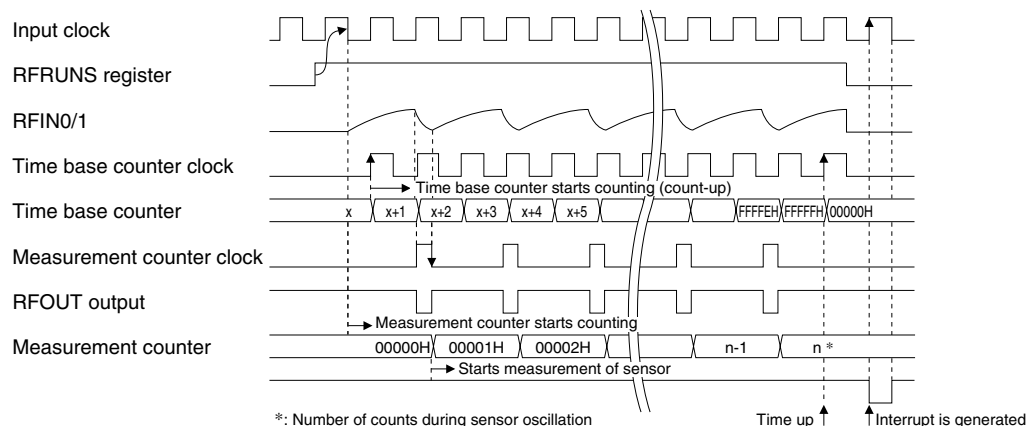


Fig. 4.13.3.2 Sensor oscillation timing chart

The sensor oscillation starts in synchronization with the falling edge of the input clock immediately after writing "1" to the RFRUNS register. The measurement counter starts counting up at the falling edge of the first clock after CR oscillation is initiated.

The time base counter is enabled at the falling edge of the first input clock. Then, it counts up by the rising edge of the input clock. Depending on the timing, the measurement counter may not count the CR oscillation clock at the time RFRUNS is set to "0".



The RFRUNS register is set to "0" at the falling edge of the input clock immediately after the time base counter reaches 00000H. Interrupt conditions are sampled with the OSC1 clock, so an interrupt occurs in synchronization with the rising edge of the OSC1 clock immediately after the RFRUNS register is set to "0".

By the above operation, the sensor is oscillated for the same period of time as the reference resistance is oscillated. Therefore, the difference in oscillation frequency can be measured from the values counted by the measurement counter.

Since the reference resistance is oscillated until the measurement counter overflows, an appropriate initial value needs to be set before R/f conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. However, the time base counter may overflow while counting the oscillation frequency of the reference resistance.

If an overflow occurs, CR oscillation and R/f conversion is terminated immediately. Also in such cases, an interrupt occurs. Moreover, the measurement counter may overflow while counting the sensor oscillation depending on initial value setting. If the measurement counter overflows, CR oscillation and R/f conversion is terminated at that point and an interrupt occurs.

When these overflows occur, the correct value cannot be read. Therefore, the overflow flags are provided to judge whether the read data is correct or an overflow occurs. There are two overflow flags; OVMC that indicates an measurement counter overflow and OVTBC that indicates an time base counter overflow. These flags are set to "1" if respective counter overflows. These flags are reset to "0" when R/f conversion is started or when "1" is written to the flag. When the interrupt occurs, be sure to read the overflow flags and check overflow.

The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.

The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 00000H) before setting it on the measurement counter. Since the data output from the measurement counter after R/f conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 4.13.3.3.

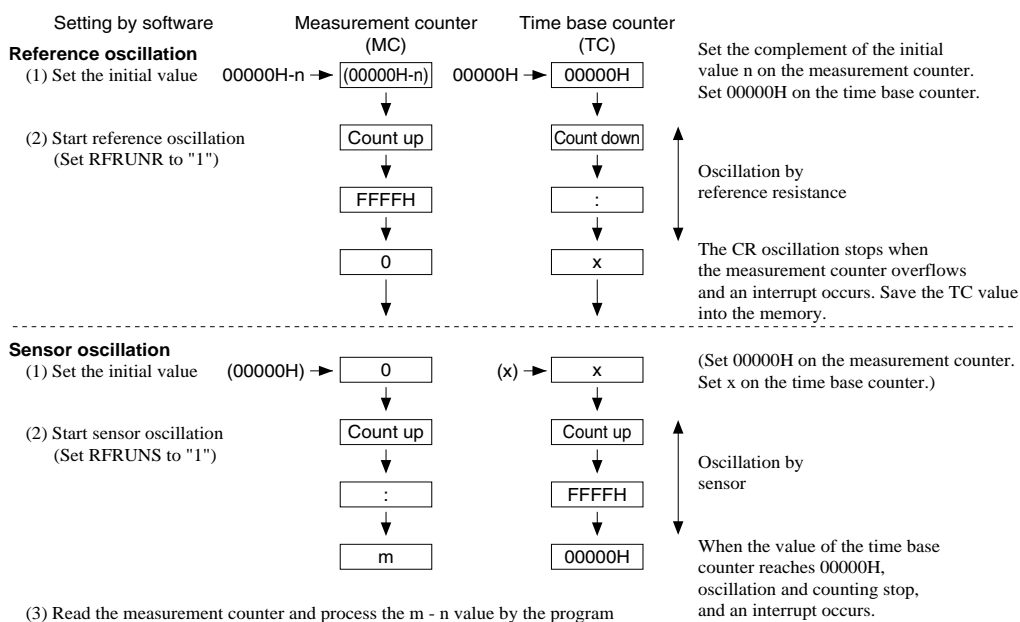


Fig. 4.13.3.3 Sequence of R/f conversion

**Note:** Set the initial value of the measurement counter taking into account the measurable range and the overflow of counters.

4.13.4 Interrupt function

The R/f converter has a function which allows interrupt to occur after R/f conversion. When the measurement counter is counted up to 00000H, both counters stop counting. The interrupt factor flag IRFB is set to "1" at the rising edge of the OSC1 clock immediately after RFRUNR is set to "0" and an interrupt occurs.

When the time base counter is counted down to 00000H, both counters stop counting. The interrupt factor flag IRFM is set to "1" at the rising edge of the OSC1 clock immediately after the RFRUNS register is set to "0" and an interrupt occurs.

If the measurement counter overflows during counting of the sensor oscillation, or the time base counter overflows during counting of the reference resistance oscillation, the interrupt factor flag IRFM or IRFB is also set to "1". These interrupt factors allow masking by the interrupt mask registers EIRFM and EIRFB. When the EIRFM/EIRFB has been set at "1", an interrupt occurs in the CPU. When the EIRFM/EIRFB is set at "0", no interrupt will occur in the CPU even if the interrupt factor flag is set to "1". The interrupt factor flag is reset to "0" by writing "1".

Timing of interrupt by the R/f converter is shown in Figures 4.13.4.1 to 4.13.4.4.

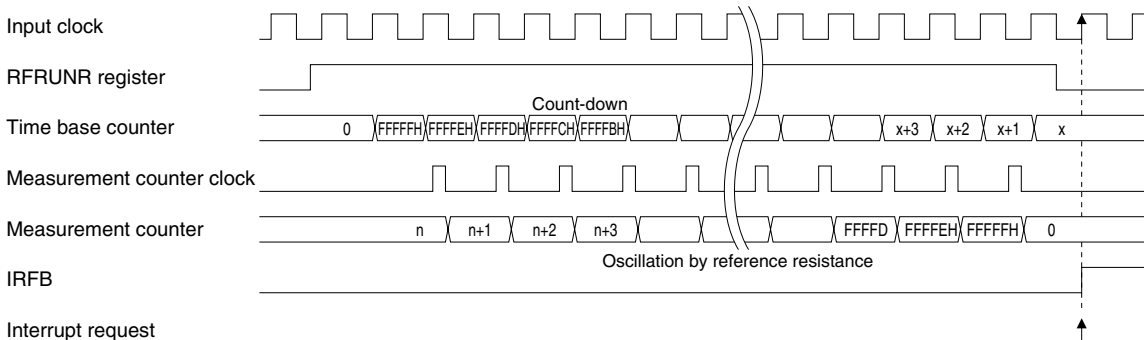


Fig. 4.13.4.1 Reference oscillate completion interrupt

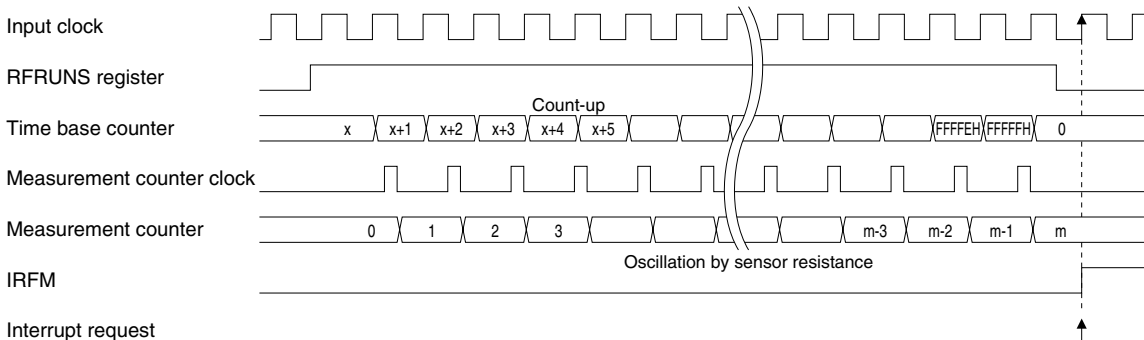


Fig. 4.13.4.2 Sensor oscillate completion interrupt

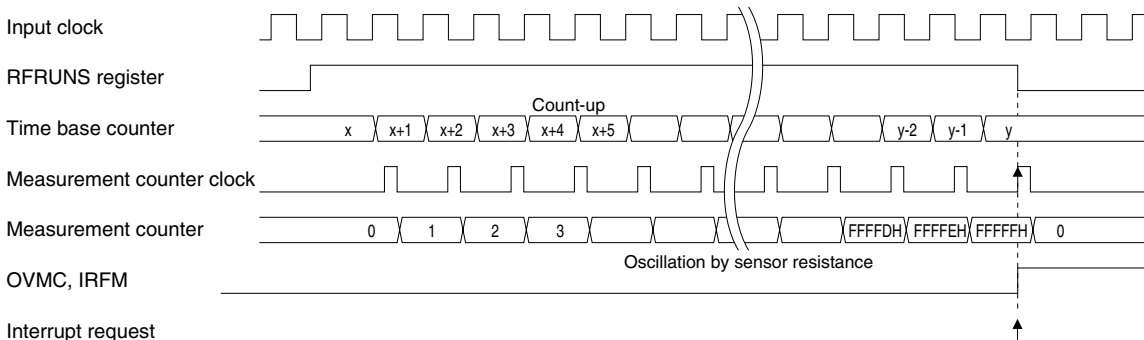


Fig. 4.13.4.3 Measurement counter overflow interrupt

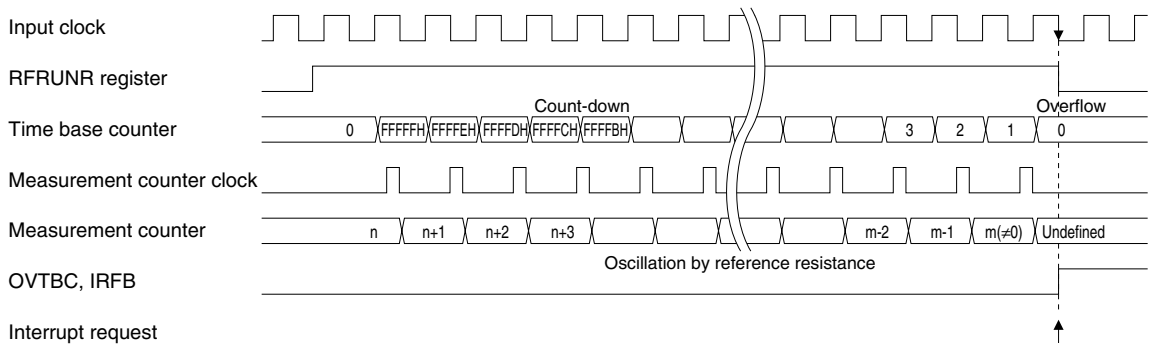


Fig. 4.13.4.4 Time base counter overflow interrupt

- Note:**
- When the R/f converter interrupt is generated, be sure to check whether or not the R/f conversion has completed normally by reading the overflow flags.
  - When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/f converter interrupt occurs.

### 4.13.5 I/O memory of R/f converter

Table 4.13.5.1 shows the I/O addresses and the control bits for the R/f converter.

Table 4.13.5.1 Control bits of R/f converter

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF90H	0	RFCLK	RFSEL	SENSEL	0 *3 RFCLK	– *2 0	OSC3	OSC1	Unused R/f conversion clock selection
	R	R/W			RFSEL	0	AC	DC	Ch. 1 sensor type selection
					SENSEL	0	Ch. 1	Ch. 0	Conversion channel selection
FF91H	OVTBC	OVMC	RFRUNR	RFRUNS	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag
	R/W	R/W			OVMC	0	Overflow	Non-ov	Measurement counter overflow flag
					RFRUNR	0	Run	Stop	Reference oscillation Run control/status (writing "0" is ineffective)
					RFRUNS	0	Run	Stop	Sensor oscillation Run control/status (writing "0" is ineffective)
FF92H	MC3	MC2	MC1	MC0	MC3	– *2			Measurement counter MC0–MC3 LSB
	R/W	R/W			MC2	– *2			
					MC1	– *2			
					MC0	– *2			
FF93H	MC7	MC6	MC5	MC4	MC7	– *2			Measurement counter MC4–MC7
	R/W	R/W			MC6	– *2			
					MC5	– *2			
					MC4	– *2			
FF94H	MC11	MC10	MC9	MC8	MC11	– *2			Measurement counter MC8–MC11
	R/W	R/W			MC10	– *2			
					MC9	– *2			
					MC8	– *2			
FF95H	MC15	MC14	MC13	MC12	MC15	– *2			Measurement counter MC12–MC15
	R/W	R/W			MC14	– *2			
					MC13	– *2			
					MC12	– *2			
FF96H	MC19	MC18	MC17	MC16	MC19	– *2			MSB Measurement counter MC16–MC19
	R/W	R/W			MC18	– *2			
					MC17	– *2			
					MC16	– *2			
FF97H	TC3	TC2	TC1	TC0	TC3	– *2			Time base counter TC0–TC3 LSB
	R/W	R/W			TC2	– *2			
					TC1	– *2			
					TC0	– *2			
FF98H	TC7	TC6	TC5	TC4	TC7	– *2			Time base counter TC4–TC7
	R/W	R/W			TC6	– *2			
					TC5	– *2			
					TC4	– *2			
FF99H	TC11	TC10	TC9	TC8	TC11	– *2			Time base counter TC8–TC11
	R/W	R/W			TC10	– *2			
					TC9	– *2			
					TC8	– *2			
FF9AH	TC15	TC14	TC13	TC12	TC15	– *2			Time base counter TC12–TC15
	R/W	R/W			TC14	– *2			
					TC13	– *2			
					TC12	– *2			
FF9BH	TC19	TC18	TC17	TC16	TC19	– *2			MSB Time base counter TC16–TC19
	R/W	R/W			TC18	– *2			
					TC17	– *2			
					TC16	– *2			
FFE7H	0	0	EIRFB	EIRFM	0 *3 0 *3	– *2 – *2	Enable	Mask	Unused Unused Interrupt mask register (R/f converter reference oscillate completion)
	R	R/W			EIRFB	0			
					EIRFM	0			Interrupt mask register (R/f converter sensor oscillate completion)
FFF7H	0	0	IRFB	IRFM	0 *3 0 *3	– *2 – *2	(R) Yes	(R) No	Unused Unused
	R	R/W			IRFB	0	(W) Reset	(W) Invalid	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFM	0			Interrupt factor flag (R/f converter sensor oscillate completion)

\*1 Initial value at initial reset

\*3 Constantly "0" when being read

\*2 Not set in the circuit

**MC0–MC19: Measurement counter (FF92H–FF96H)**

The measurement counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis.

The complement of the number of clocks to be counted by the oscillation of the reference resistance must be entered in this counter prior to reference oscillation. When the counter reaches 00000H due to overflow, the oscillation of the reference resistance stops. When converting a sensor oscillation, 00000H must be set in this register (it is unnecessary when it is done immediately after a reference oscillation has completed). The sensor oscillation and measurement counter stop when the time base counter overflows. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program. Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to R/f conversion.

At initial reset, this counter is undefined.

**TC0–TC19: Time base counter (FF97H–FF9BH)**

Writing and reading is possible on a 4-bit basis by the time base counter that is used to adjust the CR oscillation time between the reference resistance and the sensor.

The time base counter counts down during oscillation of the reference resistance and counts up to 00000H during oscillation of the sensor.

00000H needs to be entered in the counter prior to a reference oscillation in order to adjust the CR oscillating time (number of clocks) of both counts. The counter value after a reference oscillation has completed should be read from this register and save it in the memory. The saved value should be set in this counter before starting a sensor oscillation.

At initial reset, this counter is undefined.

**RFCLK: Input clock selection (FF90H•D2)**

Selects the clock input to the time base counter.

When "1" is written: OSC3

When "0" is written: OSC1

Reading: Valid

Select the count clock for the time base counter. When "1" is written to RFCLK, the OSC3 clock is selected. When "0" is written, the OSC1 clock (Typ. 32 kHz) is selected. To select the OSC3 clock, the OSC3 oscillation frequency must be 2 MHz or less.

At initial reset, this register is set to "0".

**RFSEL: Sensor selection for channel 1 (FF90H•D1)**

Selects a sensor type to be used for channel 1.

When "1" is written: Resistive humidity sensor

When "0" is written: Resistive sensor

Reading: Valid

When "1" is written to RFSEL, a resistive humidity sensor is selected as the sensor for channel 1. When "0" is written, a normal resistive sensor is selected.

At initial reset, this register is set to "0".

**SENSEL: Channel selection register (FF90H•D0)**

Selects the channel to be converted.

When "1" is written: Channel 1

When "0" is written: Channel 0

Reading: Valid

When "1" is written to SENSEL, channel 1 is selected for R/f conversion and when "0" is written, channel 0 is selected.

At initial reset, this register is set to "0".

**RFRUNR: Reference oscillation RUN control/status (FF91H•D1)**

Starts R/f conversion for the reference resistance and indicates the operating (RUN/STOP) status.

When "1" is written: R/f conversion starts

When "0" is written: No operation

When "1" is read: RUN status

When "0" is read: STOP status

When "1" is written to RFRUNR, R/f conversion for the reference resistance starts. The register remains at "1" during R/f conversion and is set to "0" when R/f conversion is terminated.

Writing "0" to RFRUNR is invalid.

At initial reset, this register is set to "0".

**RFRUNS: Sensor oscillation RUN control/status (FF91H•D0)**

Starts R/f conversion for the sensor and indicates the operating (RUN/STOP) status.

When "1" is written: R/f conversion starts

When "0" is written: No operation

When "1" is read: RUN status

When "0" is read: STOP status

When "1" is written to RFRUNS, R/f conversion for the sensor starts. The register remains at "1" during R/f conversion and is set to "0" when R/f conversion is terminated.

Writing "0" to RFRUNS is invalid.

At initial reset, this register is set to "0".

**OVMC: Measurement counter overflow flag (FF91H•D2)**

Indicates whether the measurement counter has overflowed.

When "1" is read: Overflow has occurred

When "0" is read: Overflow has not occurred

When "1" is written: Flag reset

When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVMC is set to "1" and the interrupt occurs at the same time.

This flag is reset by writing "1" or starting R/f conversion.

At initial reset, this flag is set to "0".

**OVTBC: Time base counter overflow flag (FF91H•D3)**

Indicates whether the time base counter has overflowed.

When "1" is read: Overflow has occurred

When "0" is read: Overflow has not occurred

When "1" is written: Flag reset

When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVTBC is set to "1" and the interrupt occurs at the same time.

This flag is reset by writing "1" or starting R/f conversion.

At initial reset, this flag is set to "0".

**EIRFM, EIRFB: Interrupt mask registers (FFE7H•D0, D1)**

Select whether to mask interrupt with the R/f converter.

When "1" is written: Enable

When "0" is written: Mask

Reading: Valid

EIRFM and EIRFB are the interrupt mask registers for the sensor oscillate completion interrupt and the reference oscillate completion interrupt. The R/f converter interrupt is permitted when "1" is written to EIRFM and EIRFB. When "0" is written, interrupt is masked.

At initial reset, these registers are set to "0".

**IRFM, IRFB: Interrupt factor flags (FFF7H•D0, D1)**

These flags indicate the status of the R/f converter interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

IRFB is set to "1" when an R/f conversion for the reference resistor is terminated or when the time base counter overflows while counting the oscillation of the reference resistance.

IRFM is set to "1" when an R/f conversion for the sensor is terminated or when the measurement counter overflows while counting the oscillation of the sensor.

From the status of these flags, the software can decide whether an R/f converter interrupt has occurred. Further this flag is set in the above timing regardless of the interrupt mask register setting (except for debug mode). These flags are reset to "0" by writing "1". After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state. After an initial reset, these flags are set to "0".

**4.13.6 Programming notes**

- (1) Depending on the initial value of the measurement counter (MC), the measurement counter or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/f conversion is terminated immediately. When the R/f conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC). The upper limit of the CR oscillation frequency is 500 kHz. There is no lower-limit but make sure that the time base counter does not overflow.
- (2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/f converter interrupt occurs.
- (3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (4) When selecting OSC3 for the time base counter clock, the maximum frequency of the OSC3 clock is limited to 2 MHz.
- (5) When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF92H → FF93H → FF94H → FF95H → FF96H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.

## 4.14 Interrupt and HALT

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### <Interrupt types>

The S1C63657 provides the following interrupt functions.

External interrupt:	• Input interrupt	(2 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(5 systems)
	• Clock timer interrupt	(4 systems)
	• R/f converter interrupt	(2 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).

When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.14.1 shows the configuration of the interrupt circuit.

*Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.*

### <HALT>

The S1C63657 has HALT functions that considerably reduce the current consumption when it is not necessary.

The CPU enters HALT status when the HALT instruction is executed.

In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.



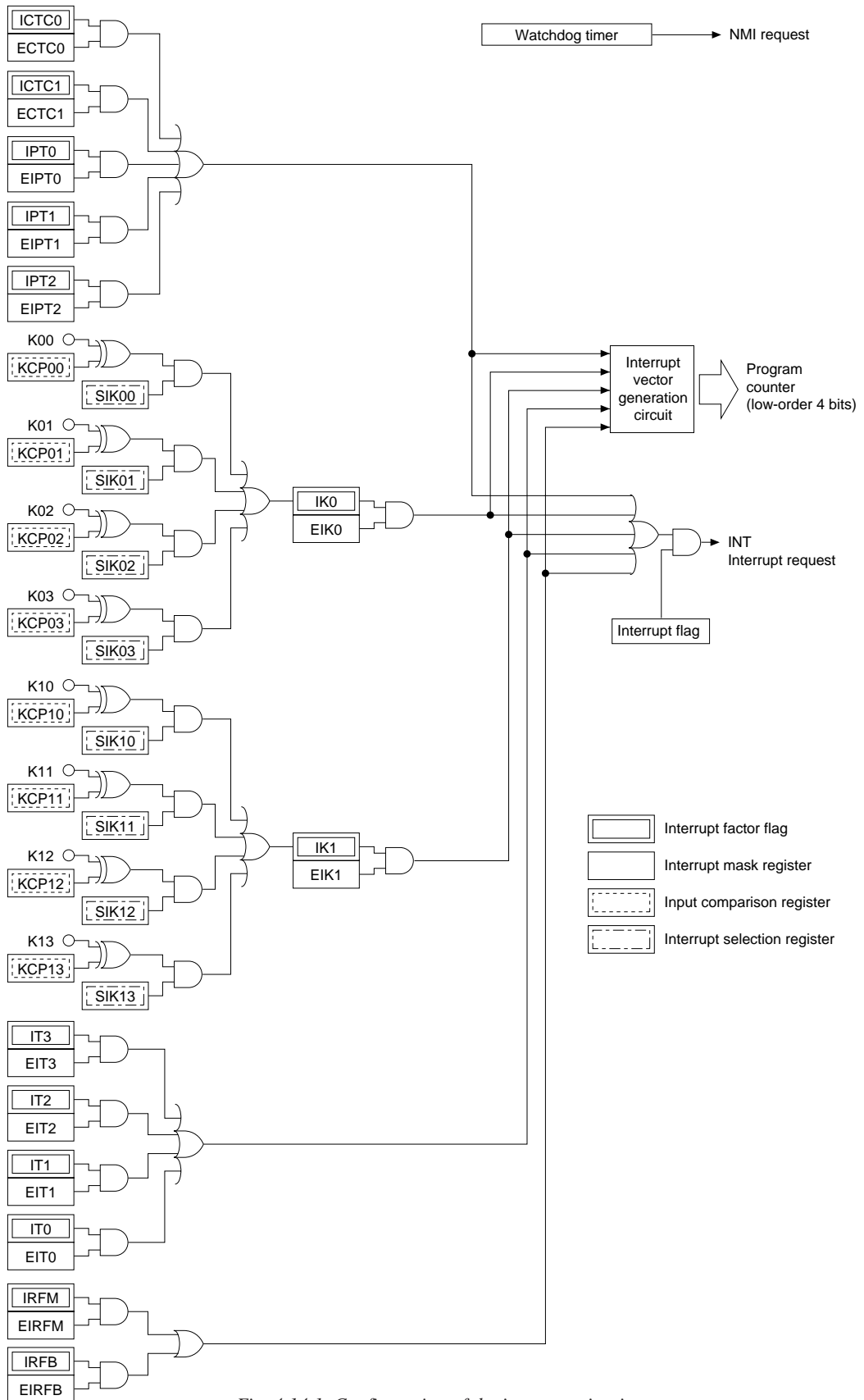


Fig. 4.14.1 Configuration of the interrupt circuit

### 4.14.1 Interrupt factor

Table 4.14.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.

The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.

At initial reset, the interrupt factor flags are reset to "0".

- \* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.14.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Programmable timer 1 (compare match)	ICTC1 (FFF0H•D1)
Programmable timer 0 (compare match)	ICTC0 (FFF0H•D0)
Programmable timer 2 (underflow)	IPT2 (FFF1H•D2)
Programmable timer 1 (underflow)	IPT1 (FFF1H•D1)
Programmable timer 0 (underflow)	IPT0 (FFF1H•D0)
K00–K03 input (falling edge or rising edge)	IK0 (FFF3H•D0)
K10–K13 input (falling edge or rising edge)	IK1 (FFF4H•D0)
Clock timer 1 Hz (falling edge)	IT3 (FFF5H•D3)
Clock timer 2 Hz (falling edge)	IT2 (FFF5H•D2)
Clock timer 8 Hz (falling edge)	IT1 (FFF5H•D1)
Clock timer 32 Hz (falling edge)	IT0 (FFF5H•D0)
R/f converter (end of reference conversion)	IRFB (FFF7H•D1)
R/f converter (end of sensor conversion)	IRFM (FFF7H•D0)

*Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.*

### 4.14.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.

The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.

At initial reset, the interrupt mask register is reset to "0".

Table 4.14.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.14.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
ECTC1	(FFE0H•D1)	ICTC1	(FFF0H•D1)
ECTC0	(FFE0H•D0)	ICTC0	(FFF0H•D0)
EIPT2	(FFE1H•D2)	IPT2	(FFF1H•D2)
EIPT1	(FFE1H•D1)	IPT1	(FFF1H•D1)
EIPT0	(FFE1H•D0)	IPT0	(FFF1H•D0)
EIK0	(FFE3H•D0)	IK0	(FFF3H•D0)
EIK1	(FFE4H•D0)	IK1	(FFF4H•D0)
EIT3	(FFE5H•D3)	IT3	(FFF5H•D3)
EIT2	(FFE5H•D2)	IT2	(FFF5H•D2)
EIT1	(FFE5H•D1)	IT1	(FFF5H•D1)
EIT0	(FFE5H•D0)	IT0	(FFF5H•D0)
EIRFB	(FFE7H•D1)	IRFB	(FFF7H•D1)
EIRFM	(FFE7H•D0)	IRFM	(FFF7H•D0)

### 4.14.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

- 1 The content of the flag register is evacuated, then the I flag is reset.
- 2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
- 3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.
- 4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.14.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.14.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High ↑
0102H	R/f converter	
0104H	Programmable timer	
0106H	–	
0108H	K00–K03 input	↓ Low
010AH	K10–K13 input	
010CH	Clock timer	
010EH	–	

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

#### 4.14.4 I/O memory of interrupt

Tables 4.14.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.14.4.1(a) Control bits of interrupt

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1			K00–K03 input comparison register
					KCP02	1			
					KCP01	1			
					KCP00	1			
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
					SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1			K10–K13 input comparison register
					KCP12	1			
					KCP11	1			
					KCP10	1			
FFE0H	0	0	ECTC1	ECTC0	0 *3	–*2			Unused
					0 *3	–*2			Unused
		R		R/W	ECTC1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 compare match)
					ECTC0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 compare match)
FFE1H	0	EIPT2	EIPT1	EIPT0	0 *3	–*2			Unused
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2 underflow)
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1 underflow)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0 underflow)
FFE3H	0	0	0	EIK0	0 *3	–*2			Unused
					0 *3	–*2			Unused
					0 *3	–*2			Unused
		R		R/W	EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	–*2			Unused
					0 *3	–*2			Unused
					0 *3	–*2			Unused
		R		R/W	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE7H	0	0	EIRFB	EIRFM	0 *3	–*2			Unused
					0 *3	–*2			Unused
		R		R/W	EIRFB	0	Enable	Mask	Interrupt mask register (R/f converter reference oscillate completion)
					EIRFM	0	Enable	Mask	Interrupt mask register (R/f converter sensor oscillate completion)
FFF0H	0	0	ICTC1	ICTC0	0 *3	–*2	(R)	(R)	Unused
					0 *3	–*2	Yes	No	Unused
					ICTC1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1 compare match)
					ICTC0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0 compare match)
FFF1H	0	IPT2	IPT1	IPT0	0 *3	–*2	(R)	(R)	Unused
					IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
					IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	IK0	0 *3	–*2	(R)	(R)	Unused
					0 *3	–*2	Yes	No	Unused
					0 *3	–*2	(W)	(W)	Unused
		R		R/W	IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	–*2	(R)	(R)	Unused
					0 *3	–*2	Yes	No	Unused
					0 *3	–*2	(W)	(W)	Unused
		R		R/W	IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

\*1 Initial value at initial reset

\*3 Constantly "0" when being read

\*2 Not set in the circuit

Table 4.14.4.1(b) Control bits of interrupt

Address	Register								
	D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF7H	0	0	IRFB	IRFM	0 *3	− *2	(R)	(R)	Unused
					0 *3	− *2	Yes	No	Unused
	R		R/W		IRFB	0	(W)	(W)	Interrupt factor flag (R/f converter reference oscillate completion)
					IRFM	0	Reset	Invalid	Interrupt factor flag (R/f converter sensor oscillate completion)

\*1 Initial value at initial reset

\*3 Constantly "0" when being read

\*2 Not set in the circuit

**ECTC1, ECTC0: Interrupt mask registers (FFE0H•D1, D0)****EIPT2, EIPT1, EIPT0: Interrupt mask registers (FFE1H•D2, D1, D0)****ICTC1, ICTC0: Interrupt factor flags (FFF0H•D1, D0)****IPT2, IPT1, IPT0: Interrupt factor flags (FFF1H•D2, D1, D0)**

Refer to Section 4.10, "Programmable Timer".

**KCP03–KCP00, KCP13–KCP10: Input comparison registers (FF22H, FF26H)****SIK03–SIK00, SIK13–SIK10: Interrupt selection registers (FF20H, FF24H)****EIK0, EIK1: Interrupt mask registers (FFE3H•D0, FFE4H•D0)****IK0, IK1: Interrupt factor flags (FFF3H•D0, FFF4H•D0)**

Refer to Section 4.5, "Input Ports".

**EIT3–EIT0: Interrupt mask registers (FFE5H)****IT3–IT0: Interrupt factor flags (FFF5H)**

Refer to Section 4.9, "Clock Timer".

**EIRFB, EIRFM: Interrupt mask registers (FFE7H•D1, D0)****IRFB, IRFM: Interrupt factor flags (FFF7H•D1, D0)**

Refer to Section 4.13, "R/f Converter".

### 4.14.5 Programming notes

- (1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

## CHAPTER 5 SUMMARY OF NOTES

### 5.1 Notes for Low Current Consumption

The S1C63657 contains control registers for each of the circuits so that current consumption can be reduced.

These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.

The following lists the circuits that can control operation and their control registers. Refer to these when programming.

*Table 5.1.1 Circuits and control registers*

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
High-speed operation voltage regulator	VDC0, VDC1
LCD system voltage circuit	LPWR
Voltage halver mode	VDC2, VDC3

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

**CPU:** Operating status

**CPU operating frequency:** Low speed side (CLKCHG = "0")  
OSC3 oscillation circuit is in off status (OSCC = "0")

**Internal logic operating voltage:** VD1L (VDC0 = "0")

**High-speed operation voltage regulator:** Off status (VDC1 = "0")

**LCD system voltage circuit:** Off status (LPWR = "0")

**Voltage halver mode:** Off status (VDC2 = VDC3 = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several  $\mu\text{A}$  on account of the LCD panel characteristics.

## 5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

### Memory and stack

- (1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.
- (2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.
- (3) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).  
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63657 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access. After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

### Power control

- (1) When setting the low-speed operation voltage regulator into the halver mode, switch the CPU clock to OSC1 before writing "1" to VDC2.
- (2) When setting the LCD system voltage circuit into the halver mode, set the VC1 voltage (contrast) to 1.13 V or lower (LC register = 6 or less) before writing "1" to VDC3.

### Watchdog timer

- (1) When the watchdog timer is being used, the software must reset it within 3-second cycles.
- (2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

### Oscillation circuit

- (1) When switching the CPU system clock from OSC1 to OSC3, first set the operating voltage for high-speed operation (VD3). After that maintain 2.5 msec or more, and then turn the OSC3 oscillation on. When switching from OSC3 to OSC1, set the operating voltage for low-speed operation (VD1L) after switching to OSC1 and turning the OSC3 oscillation off.
- (2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.  
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.
- (3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.
- (4) When the low-speed operation voltage regulator is in the halver mode (VDC2 = "1"), the system can be operated only in low-speed using the OSC1 clock. Do not switch the system clock to OSC3.
- (5) Do not switch the operating voltage to VD1L while the CPU is operating with the OSC3 clock. Furthermore, do not stop the high-speed operating voltage regulator.
- (6) When selecting OSC3 for the time base counter clock of the R/f converter, the maximum frequency of the OSC3 clock is limited to 2 MHz.

- (7) If the HALT instruction is executed or HALT mode is canceled while the CPU is running with the high-speed clock generated by the OSC3 oscillation circuit, the internal logic operating voltage  $V_{D1}$  becomes unstable momentarily and it may cause unexpected problem, such as runaway, be occurred. Do not use the HALT instruction while the CPU is running with the OSC3 high-speed clock.

### Input port

When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time. Particular care needs to be taken of the key scan during key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF  
R: pull-down resistance 375 k $\Omega$  (Max.)

### Output port

- (1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).  
Be aware that the output terminal is fixed at a low ( $V_{SS}$ ) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.  
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).
- (2) A hazard may occur when the FOUT signal and the TOUT signal are turned on and off.
- (3) When  $f_{OSC3}$  is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.  
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

### I/O port

When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF  
R: pull-down resistance 375 k $\Omega$  (Max.)

### LCD driver

Because at initial reset, the contents of display memory are undefined and LC3–LC0 (LCD contrast) is set to 0000B, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes off.

### Clock timer

Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

### Programmable timer

- (1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) are not latched when the low-order 4 bits are read. Therefore, the high-order 4 bits should be read within 0.73 msec (when  $f_{OSC1}$  is 32.768 kHz) from reading the low-order 4 bits. When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data. The counter running with OSC3 counts down for the value listed in Table 5.2.1 while the CPU running with OSC1 reads the low-order 4 bits and high-order 4 bits of the counter data by two instructions.



Table 5.2.1 Counter change with OSC3 between readings low-order and high-order data with OSC1

Count clock	Counter change between reading
OSC3/1	0200H
OSC3/4	001AH
OSC3/32	0002H

In 16-bit mode, the counter data must be read in the order below.

PTD00–PTD03 → PTD04–PTD07 → PTD10–PTD13 → PTD14–PTD17

- (2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.

Figure 5.2.1 shows the timing chart for the RUN/STOP control.

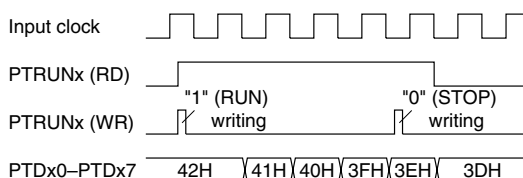


Fig. 5.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

- (3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
- (4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

- (5) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running. The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

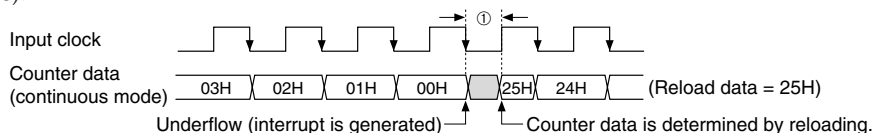


Fig. 5.2.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

## Sound generator

- (1) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.
- (2) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

## Integer multiplier

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode selection register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

## R/f converter

- (1) Depending on the initial value of the measurement counter (MC), the measurement counter or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/f conversion is terminated immediately. When the R/f conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC). The upper limit of the CR oscillation frequency is 500 kHz. There is no lower-limit but make sure that the time base counter does not overflow.
- (2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/f converter interrupt occurs.
- (3) When selecting OSC3 for the time base counter clock, the maximum frequency of the OSC3 clock is limited to 2 MHz.
- (4) When setting the measurement counter, always write 5 words of data continuously in order from the lower address (FF92H → FF93H → FF94H → FF95H → FF96H). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used.

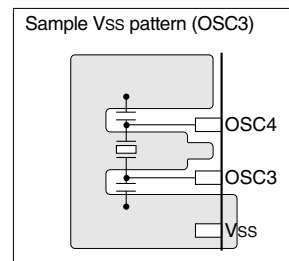
## Interrupt

- (1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

## 5.3 Precautions on Mounting

### <Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:
  - (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.
  - (2) As shown in the right hand figure, make a Vss pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this Vss pattern for any purpose other than the oscillation system.
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

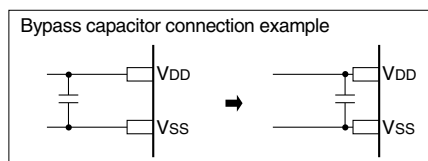


### <Reset Circuit>

- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.). Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When using the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

### <Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:
  - (1) The power supply should be connected to the VDD, VSS, VDDA and VSSA terminals with patterns as short and large as possible. In particular, the power supply for VDDA and VSSA affect R/f conversion accuracy.
  - (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



- (3) Components which are connected to the VD1, VD2, VOSC and VC1–VC3 terminals, such as capacitors, should be connected in the shortest line. In particular, the VC1–VC3 voltages affect the display quality.
- Do not connect anything to the VC1–VC3 terminals when the LCD driver is not used.

**<R/f Converter>**

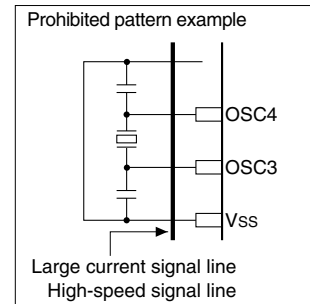
- The power supply terminals for the analog system should be connected as shown below even if the R/f converter is not used.

VDDA → VDD

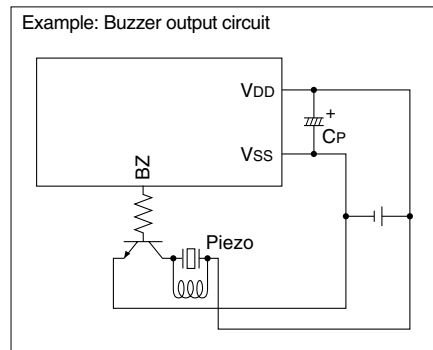
VSSA → VSS

**<Arrangement of Signal Lines>**

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.

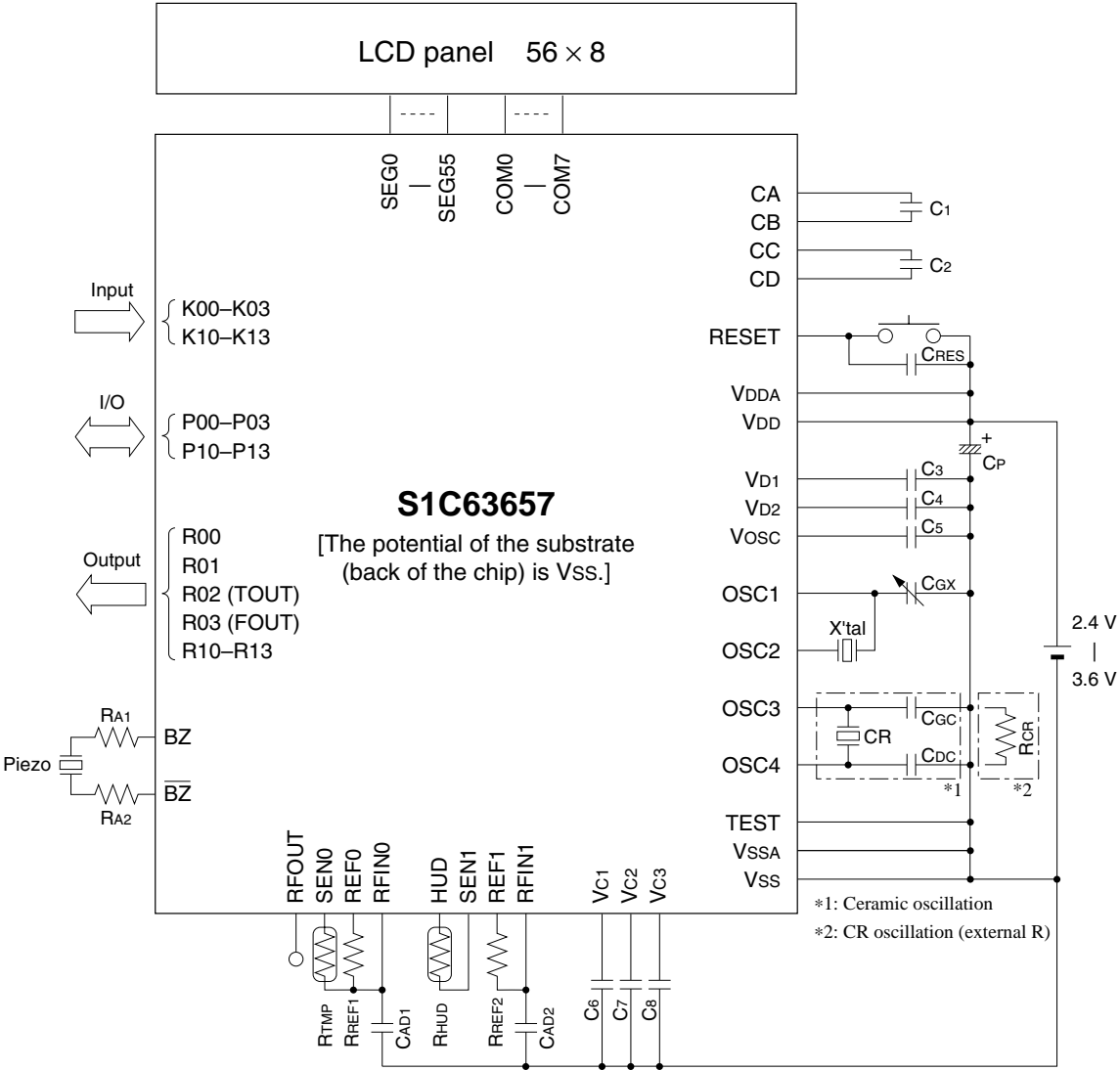
**<Output Terminals>**

- When an output terminal is used to drive an external component that consumes a large amount of current, the operation of the external component affects the built-in power supply circuit of this IC and the output voltage may vary. When driving a bipolar transistor by a periodic signal such as the BZ or timer output in particular, it may cause variations in the voltage output from the LCD system voltage circuit that affects the contrast of the LCD display. To prevent this, separate the traces on the printed circuit board. Put one between the power supply and the IC's VDD and VSS terminals, and another between the power supply and the external component that consumes the large amount of current. Furthermore, use an external component with as low a current consumption as possible.

**<Precautions for Visible Radiation (when bare chip is mounted)>**

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.
  - (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.
  - (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
  - (3) As well as the face of the IC, shield the back and side too.

# CHAPTER 6    BASIC EXTERNAL WIRING DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, C1 (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR	Resistor for OSC3 CR oscillation	30 kΩ (2 MHz)
C1–C8	Capacitor	0.2 μF
CP	Capacitor	3.3 μF
CRES	RESET terminal capacitor	0.1 μF
RA1, RA2	Protective resistor	100 Ω

Note: The above table is simply an example, and is not guaranteed to work.

# CHAPTER 7 ELECTRICAL CHARACTERISTICS

## 7.1 Absolute Maximum Rating

(V <sub>SS</sub> =0V)			
Item	Symbol	Rated value	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 4.5	V
Input voltage (1)	V <sub>I</sub>	-0.5 to V <sub>DD</sub> + 0.3	V
Input voltage (2)	V <sub>I</sub> OSC	-0.5 to V <sub>D1</sub> + 0.3	V
Permissible total output current *1	ΣI <sub>VDD</sub>	10	mA
Operating temperature	T <sub>opr</sub>	-20 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature / time	T <sub>sol</sub>	260°C, 10sec (lead section)	—
Permissible dissipation	P <sub>d</sub>	250	mW

\*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

## 7.2 Recommended Operating Conditions

(Ta=-20 to 70°C)							
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	VDD	VSS=0V	Normal mode, OSC3 OFF	1.8	3.0	3.6	V
			Normal mode, OSC3=4MHz (Max.)	2.4	3.0	3.6	V
			Halver mode, OSC3 OFF	2.4	3.0	3.6	V
Oscillation frequency	fOSC1	Crystal oscillation		—	32.768	—	kHz
	fOSC3	CR oscillation (built-in R), VDD=2.4 to 3.6V		770	1,100	1,430	kHz
		CR oscillation (external R), VDD=2.4 to 3.6V		200		2,000	kHz
		Ceramic oscillation, VDD=2.4 to 3.6V when the R/f converter uses the OSC3 clock				2,000	kHz
		Ceramic oscillation, VDD=2.4 to 3.6V when the R/f converter does not use the OSC3 clock				4,000	kHz

## 7.3 DC Characteristics

Unless otherwise specified:

V<sub>DD</sub>=3.0V, V<sub>SS</sub>=0V, f<sub>OSC1</sub>=32.768kHz, Ta=25°C, V<sub>D1</sub>-V<sub>D2</sub>/V<sub>C1</sub>-V<sub>C3</sub> are internal voltage, C<sub>1</sub>-C<sub>8</sub>=0.2μF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V <sub>IH1</sub>	K00-03, K10-13, P00-03, P10-13	0.8·V <sub>DD</sub>		V <sub>DD</sub>	V
High level input voltage (2)	V <sub>IH2</sub>	RESET, TEST	0.9·V <sub>DD</sub>		V <sub>DD</sub>	V
Low level input voltage (1)	V <sub>IL1</sub>	K00-03, K10-13, P00-03, P10-13	0		0.2·V <sub>DD</sub>	V
Low level input voltage (2)	V <sub>IL2</sub>	RESET, TEST	0		0.1·V <sub>DD</sub>	V
High level input current (1)	I <sub>IH1</sub>	V <sub>IH1</sub> =3.0V No pull down	0		0.5	μA
High level input current (2)	I <sub>IH2</sub>	V <sub>IH2</sub> =3.0V With pull down	8	12	20	μA
Low level input current (1)	I <sub>IL1</sub>	V <sub>IL1</sub> =V <sub>SS</sub> No pull down	-0.5		0	μA
Low level input current (2)	I <sub>IL2</sub>	V <sub>IL2</sub> =V <sub>SS</sub> With pull down	-0.5		0	μA
High level output current (1)	I <sub>OH1</sub>	V <sub>OH1</sub> =0.9·V <sub>DD</sub> R00-03, R10-13, P00-03, P10-13			-0.5	mA
High level output current (2)	I <sub>OH2</sub>	V <sub>OH2</sub> =0.9·V <sub>DD</sub> BZ, BZ			-0.5	mA
Low level output current (1)	I <sub>OL1</sub>	V <sub>OL1</sub> =0.1·V <sub>DD</sub> R00-03, R10-13, P00-03, P10-13	0.5			mA
Low level output current (2)	I <sub>OL2</sub>	V <sub>OL2</sub> =0.1·V <sub>DD</sub> BZ, BZ	0.5			mA
Common output current	I <sub>OH3</sub>	V <sub>OH3</sub> =V <sub>C3</sub> -0.05V	10		-10	μA
	I <sub>OL3</sub>	V <sub>OL3</sub> =V <sub>SS</sub> +0.05V				μA
Segment output current (during LCD output)	I <sub>OH4</sub>	V <sub>OH4</sub> =V <sub>C3</sub> -0.05V			-10	μA
	I <sub>OL4</sub>	V <sub>OL4</sub> =V <sub>SS</sub> +0.05V	10			μA
Segment output current (during DC output)	I <sub>OH5</sub>	V <sub>OH5</sub> =0.9·V <sub>DD</sub>			-300	μA
	I <sub>OL5</sub>	V <sub>OL5</sub> =0.1·V <sub>DD</sub>	300			μA
R/f converter transistor ON resistance	R <sub>RFINT<sub>r</sub></sub>	V <sub>DS</sub> =0.1V, V <sub>DD</sub> =1.8V		20	40	Ω
	R <sub>RFETr</sub>	V <sub>DS</sub> =0.1V, V <sub>DD</sub> =1.8V		50	100	Ω
	R <sub>SENOT<sub>r</sub></sub>	V <sub>DS</sub> =0.1V, V <sub>DD</sub> =1.8V		50	100	Ω
	R <sub>SENIT<sub>r</sub></sub>					

## 7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:

$V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $f_{OSC1}=32.768kHz$ ,  $C_G=25pF$ ,  $T_a=25^{\circ}C$ ,  $V_{D1}-V_{D2}/V_{C1}-V_{C3}$  are internal voltage,  $C_1-C_8=0.2\mu F$

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	VC1	Connect 1 M $\Omega$ load resistor between VSS and VC1 (without panel load)	LC0-3="0"	Typ. -100mV	0.95	Typ. +100mV	V
			LC0-3="1"		0.98		
			LC0-3="2"		1.01		
			LC0-3="3"		1.04		
			LC0-3="4"		1.07		
			LC0-3="5"		1.10		
			LC0-3="6"		1.13		
			LC0-3="7"		1.16		
			LC0-3="8"		1.19		
			LC0-3="9"		1.22		
			LC0-3="10"		1.25		
			LC0-3="11"		1.28		
			LC0-3="12"		1.31		
			LC0-3="13"		1.34		
			LC0-3="14"		1.37		
			LC0-3="15"		1.40		
LCD drive voltage	VC2	Connect 1 M $\Omega$ load resistor between VSS and VC2 (without panel load)		$2 \cdot V_{C1} \times 0.9$		$2 \cdot V_{C1}$	V
	VC3	Connect 1 M $\Omega$ load resistor between VSS and VC3 (without panel load)		$3 \cdot V_{C1} \times 0.9$		$3 \cdot V_{C1}$	V
Current consumption	IOP	During HALT (32kHz crystal)	LCD OFF (normal) *1,*2,*3		0.90	1.80	$\mu A$
			LCD OFF (halver) *1,*2,*4		0.45	0.90	$\mu A$
			LCD ON (normal) *1,*2,*3		1.4	2.8	$\mu A$
			LCD ON (halver) *1,*2,*4		0.65	1.4	$\mu A$
		During execution (32kHz crystal)	LCD ON (normal) *1,*2,*3		4.0	5.0	$\mu A$
			LCD ON (halver) *1,*2,*4		2.5	3.5	$\mu A$
		During execution (2MHz ceramic)	LCD ON (normal) *1,*5		400	800	$\mu A$
			LCD ON (normal) *1,*5		800	1000	$\mu A$
		During execution (4MHz ceramic)	LCD ON (normal) *1,*5		350	600	$\mu A$
			LCD ON (normal) *1,*5		350	600	$\mu A$
Current consumption		R/f converter circuit current Operating frequency=10kHz, $V_{DD}=1.8$ to $3.6V$			100	150	$\mu A$

\*1 No panel load. When R/f converter use in OFF status.

\*2  $V_{DC0}=V_{DC1}="0"$ ,  $OSCC="0"$

\*3  $V_{DC2}=V_{DC3}="0"$

\*4  $V_{DC2}=V_{DC3}="1"$

\*5  $V_{DC0}=V_{DC1}="1"$ ,  $OSCC="1"$ ,  $V_{DC2}=V_{DC3}="0"$

## 7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

### OSC1 crystal oscillation circuit

Unless otherwise specified:

V<sub>DD</sub>=3.0V, V<sub>SS</sub>=0V, f<sub>osc1</sub>=32.768kHz, C<sub>G</sub>=25pF, C<sub>D</sub>=built-in, T<sub>a</sub>=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V <sub>sta</sub>	t <sub>sta</sub> ≤3sec (V <sub>DD</sub> )	1.8			V
Oscillation stop voltage	V <sub>stp</sub>	t <sub>stp</sub> ≤10sec (V <sub>DD</sub> )	1.8			V
Built-in capacitance (drain)	C <sub>D</sub>	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	∂f/∂V	V <sub>DD</sub> =1.8 to 3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C <sub>G</sub>	C <sub>G</sub> =5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	V <sub>hho</sub>	C <sub>G</sub> =5pF (V <sub>DD</sub> )	3.6			V
Permitted leak resistance	R <sub>leak</sub>	Between OSC1 and V <sub>SS</sub>	200			MΩ

### OSC3 ceramic oscillation circuit

Unless otherwise specified:

V<sub>DD</sub>=3.0V, V<sub>SS</sub>=0V, Ceramic oscillator: 4MHz, C<sub>GC</sub>=C<sub>DC</sub>=30pF, T<sub>a</sub>=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V <sub>sta</sub>	(V <sub>DD</sub> )	2.4			V
Oscillation start time	t <sub>sta</sub>	V <sub>DD</sub> =2.4 to 3.6V			5	ms
Oscillation stop voltage	V <sub>stp</sub>	(V <sub>DD</sub> )	2.4			V

### OSC3 CR oscillation circuit (built-in R type)

Unless otherwise specified:

V<sub>DD</sub>=3.0V, V<sub>SS</sub>=0V, R<sub>CR</sub>=Built in, T<sub>a</sub>=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f <sub>osc3</sub>		-30	1,100kHz	30	%
Oscillation start voltage	V <sub>sta</sub>	(V <sub>DD</sub> )	2.4			V
Oscillation start time	t <sub>sta</sub>	V <sub>DD</sub> =2.4 to 3.6V			3	ms
Oscillation stop voltage	V <sub>stp</sub>	(V <sub>DD</sub> )	2.4			V

### OSC3 CR oscillation circuit (external R type)

Unless otherwise specified:

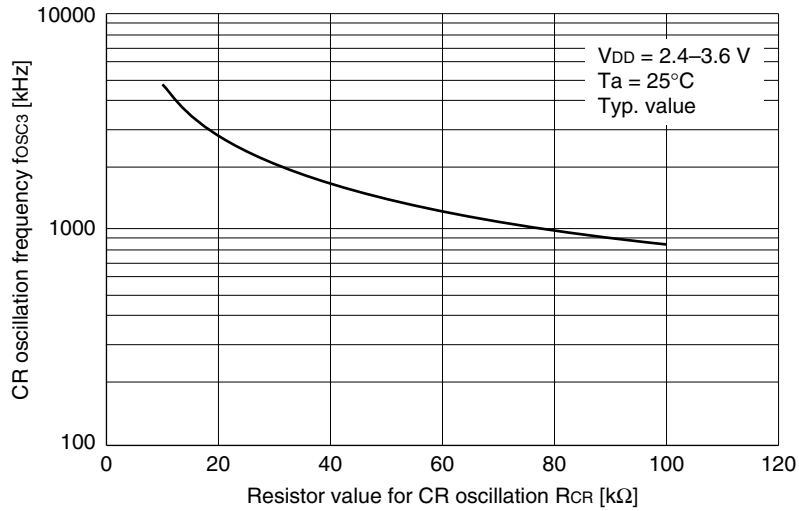
V<sub>DD</sub>=3.0V, V<sub>SS</sub>=0V, R<sub>CR</sub>=30kΩ (2MHz), T<sub>a</sub>=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f <sub>osc3</sub>		-30		30	%
Oscillation start voltage	V <sub>sta</sub>	(V <sub>DD</sub> )	2.4			V
Oscillation start time	t <sub>sta</sub>	V <sub>DD</sub> =2.4 to 3.6V			3	ms
Oscillation stop voltage	V <sub>stp</sub>	(V <sub>DD</sub> )	2.4			V



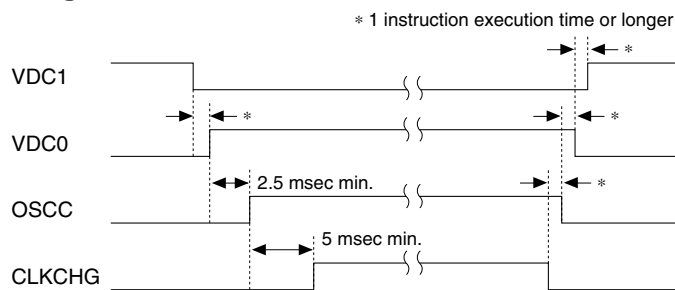
**OSC3 CR oscillation frequency-resistance characteristic (external R type)**

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



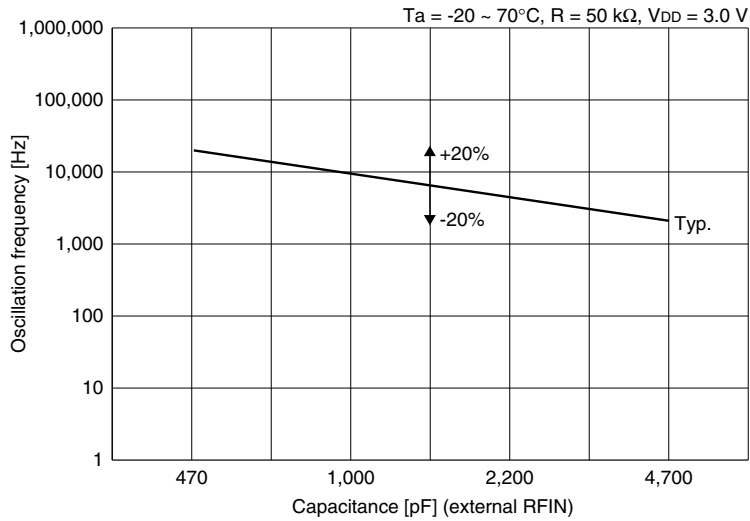
## 7.6 Timing Chart

### System clock switching

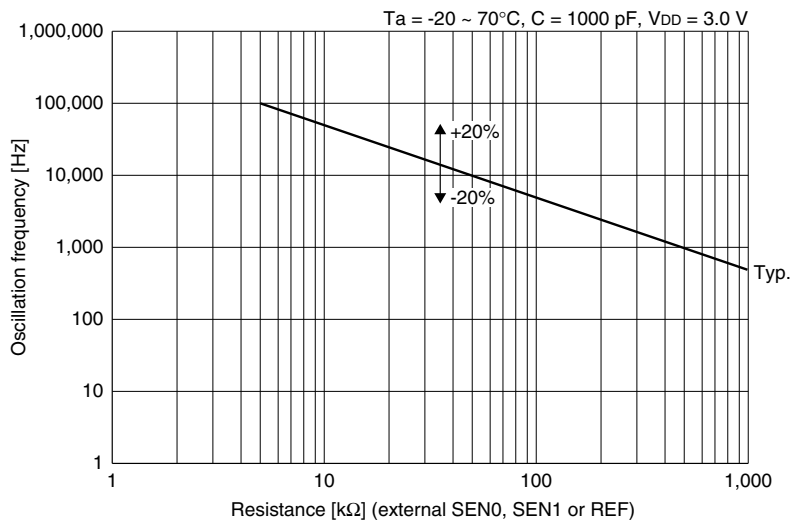


## 7.7 R/f Converter Characteristics

### R/f converter oscillation frequency - capacitance characteristic



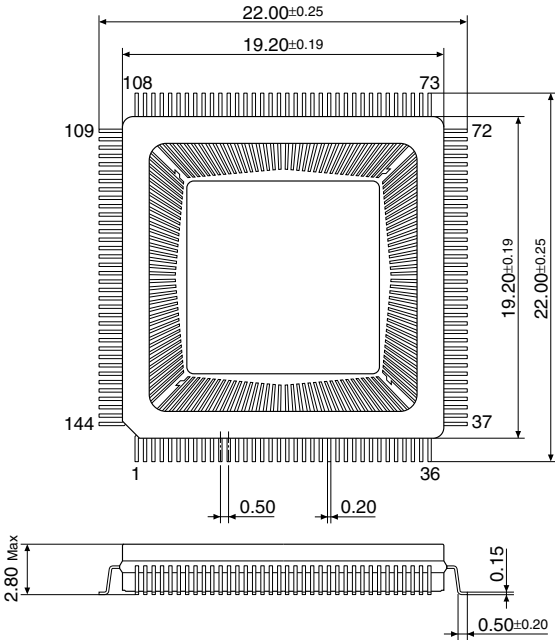
### R/f converter oscillation frequency - resistance characteristic



CHAPTER 8 CERAMIC PACKAGE FOR TEST SAMPLES

QFP17-144pin

(Unit: mm)



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	37	N.C.	73	COM4	109	N.C.
2	COM0	38	SEG28	74	COM5	110	SEG0
3	COM1	39	SEG29	75	COM6	111	SEG1
4	COM2	40	SEG30	76	COM7	112	SEG2
5	COM3	41	SEG31	77	V <sub>DD</sub>	113	SEG3
6	CA	42	N.C.	78	K00	114	N.C.
7	CB	43	SEG32	79	K01	115	SEG4
8	VC1	44	SEG33	80	K02	116	SEG5
9	VC2	45	SEG34	81	K03	117	SEG6
10	VC3	46	SEG35	82	K10	118	SEG7
11	N.C.	47	N.C.	83	K11	119	N.C.
12	N.C.	48	SEG36	84	K12	120	SEG8
13	N.C.	49	SEG37	85	K13	121	SEG9
14	V <sub>SSA</sub>	50	SEG38	86	P00	122	SEG10
15	RFOUT	51	N.C.	87	P01	123	N.C.
16	RFIN0	52	SEG39	88	P02	124	SEG11
17	RFIN1	53	SEG40	89	P03	125	SEG12
18	REF0	54	SEG41	90	P10	126	SEG13
19	SEN0	55	SEG42	91	P11	127	SEG14
20	REF1	56	SEG43	92	P12	128	SEG15
21	SEN1	57	SEG44	93	P13	129	SEG16
22	HUD	58	N.C.	94	R00	130	N.C.
23	V <sub>DDA</sub>	59	SEG45	95	R01	131	SEG17
24	CC	60	SEG46	96	R02	132	SEG18
25	CD	61	SEG47	97	R03	133	SEG19
26	V <sub>D2</sub>	62	N.C.	98	R10	134	N.C.
27	V <sub>DD</sub>	63	SEG48	99	R11	135	SEG20
28	V <sub>OSC</sub>	64	SEG49	100	R12	136	SEG21
29	OSC1	65	SEG50	101	R13	137	SEG22
30	OSC2	66	SEG51	102	BZ	138	SEG23
31	V <sub>D1</sub>	67	N.C.	103	BZ	139	N.C.
32	OSC3	68	SEG52	104	V <sub>SS</sub>	140	SEG24
33	OSC4	69	SEG53	105	N.C.	141	SEG25
34	V <sub>SS</sub>	70	SEG54	106	N.C.	142	SEG26
35	TEST	71	SEG55	107	N.C.	143	SEG27
36	RESET	72	N.C.	108	N.C.	144	N.C.

N.C. : No Connection

## APPENDIX *PERIPHERAL CIRCUIT BOARDS FOR S1C63657*

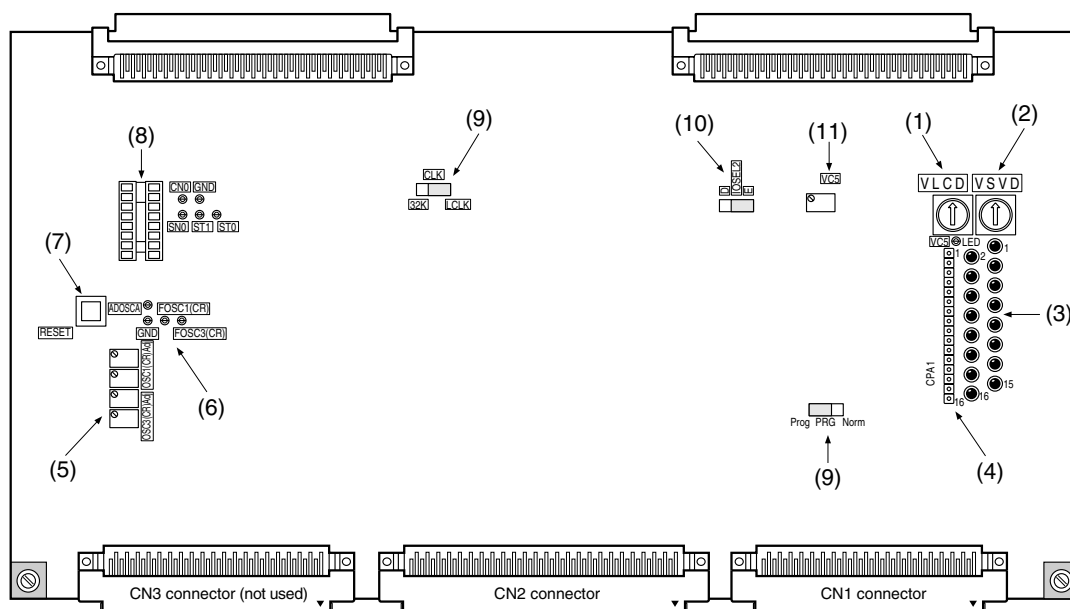
This section describes how to use the Peripheral Circuit Boards for the S1C63657 (S5U1C63000P1/S5U1C63000P6 and S5U1C63658P2), which provide emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H1/S5U1C63000H2/S5U1C63000H6).

This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P1/S5U1C63000P6) provided in this document assumes that circuit data for the S1C63657 has already been downloaded to the board. For information on downloading a circuit data and the board specifications, please see Sections A.3 and A.5, respectively. Please refer to the user's manual provided with your ICE for detailed information on its functions and method of use.

### A.1 Names and Functions of Each Part

#### A.1.1 S5U1C63000P1/S5U1C63000P6

The following explains the names and functions of each part of the S5U1C63000P1 board. The S5U1C63000P6 board has the same functions.



#### (1) VLCD

When external LCD power supply has been selected by mask option, you can turn this control to adjust the LCD drive power supply voltage.

#### (2) VSVD

Unused

#### (3) Register monitor LEDs

These LEDs correspond one-to-one to the registers listed below. The LED lights when the data is logic "1" and goes out when the data is logic "0".

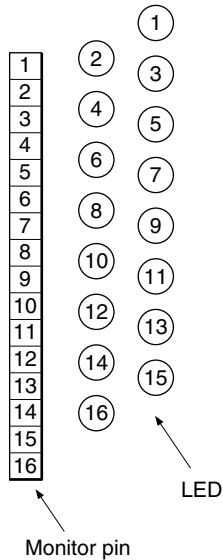
VDC0-VDC3, OSC, CLKCHG, LPWR

(4) Register monitor pins

These pins correspond one-to-one to the registers listed below. The pin outputs a high for logic "1" and a low for logic "0".

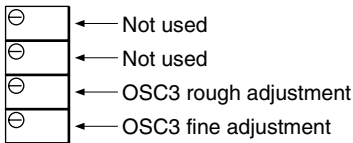
Monitor		LED	
Pin No.	Name	LED No.	Name
1	DONE *	1	DONE *
2	VDC0	2	VDC0
3	VDC1	3	VDC1
4	VDC2	4	VDC2
5	VDC3	5	VDC3
6	OSCC	6	OSCC
7	CLKCHG	7	CLKCHG
8	LPWR	8	LPWR
9	—	9	—
10	—	10	—
11	—	11	—
12	—	12	—
13	—	13	—
14	—	14	—
15	—	15	—
16	—	16	—

\* DONE: The monitor pin outputs a high while the LED lights when initialization of this board completes without problems.



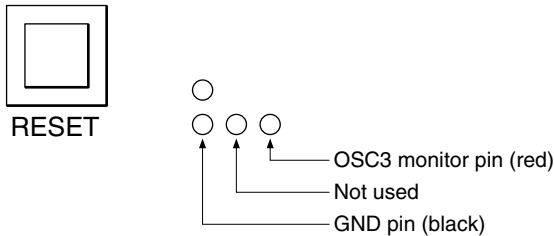
(5) CR oscillation frequency adjusting control

This control allows you to adjust the OSC3 oscillation frequency. This function is effective when ceramic oscillation is selected for the OSC3 oscillation circuit by mask option as well as when CR oscillation is selected. The oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "Electrical Characteristics", to select the appropriate operating frequency.



(6) CR oscillation frequency monitor pins

These pins allow you to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that these pins always output a signal waveform whether or not the oscillation circuit is operating.



**(7) RESET switch**

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

**(8) External part connecting socket**

Unused

**(9) CLK and PRG switch**

If power to the ICE is shut down before circuit data downloading is complete, the circuit configuration in this board will remain incomplete, and the debugger may not be able to start when you power on the ICE once again. In this case, temporarily power off the ICE and set CLK to the 32K position and the PRG switch to the Prog position, then switch on power for the ICE once again. This should allow the debugger to start up, allowing you to download circuit data. After downloading the circuit data, temporarily power off the ICE and reset CLK and PRG to the LCLK and the Norm position, respectively. Then power on the ICE once again.

**(10) IOSEL2**

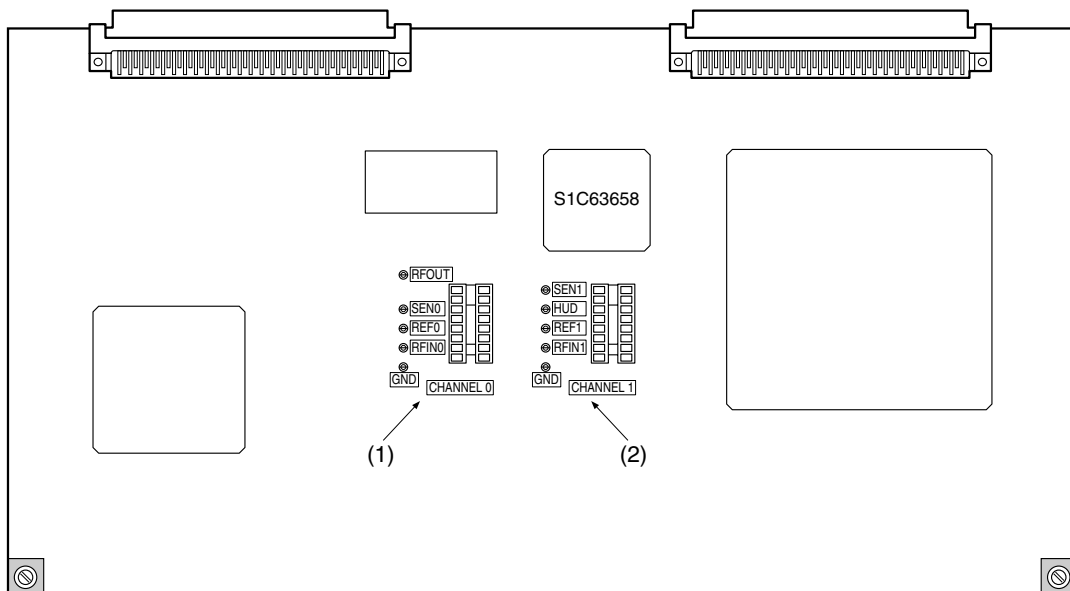
When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

**(11) VC5**

When the internal LCD power supply has been selected by mask option, you can turn this control to fine-adjust the LCD drive power supply voltage. Note, however, that the LCD drive power supply voltage in the actual IC is set according to the contents of the LCD contrast adjustment register.

### A.1.2 S5U1C63658P2

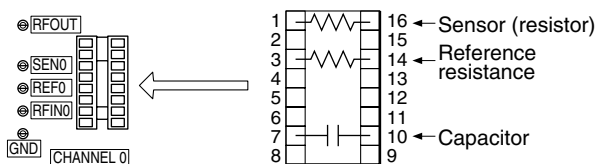
The following explains the names and functions of each part of the S5U1C63658P2 board.



#### (1) R/f converter monitor pins and external part connecting socket (Channel 0)

These monitor pins are used to check the operation of R/f converter channel 0. The socket is used to connect external resistors and a capacitor for R/f conversion.

Mount resistors and a capacitor on the platform attached with the S5U1C63658P2 and then connect it to the onboard socket.

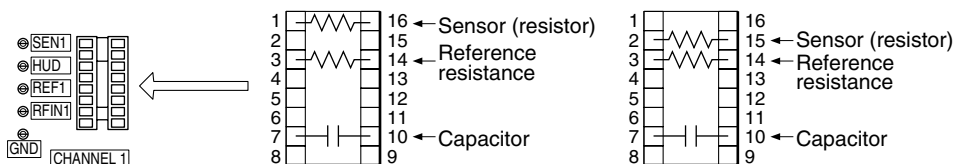


Connecting a DC-bias  
resistive sensor (e.g. thermistor)

#### (2) R/f converter monitor pins and external part connecting socket (Channel 1)

These monitor pins are used to check the operation of R/f converter channel 1. The socket is used to connect external resistors and a capacitor for R/f conversion.

Mount resistors and a capacitor on the platform attached with the S5U1C63658P2 and then connect it to the onboard socket.



Connecting a AC-bias  
resistive humidity sensor

Connecting a DC-bias  
resistive sensor (e.g. thermistor)

The sensor connect position changes according to the sensor type to be used.

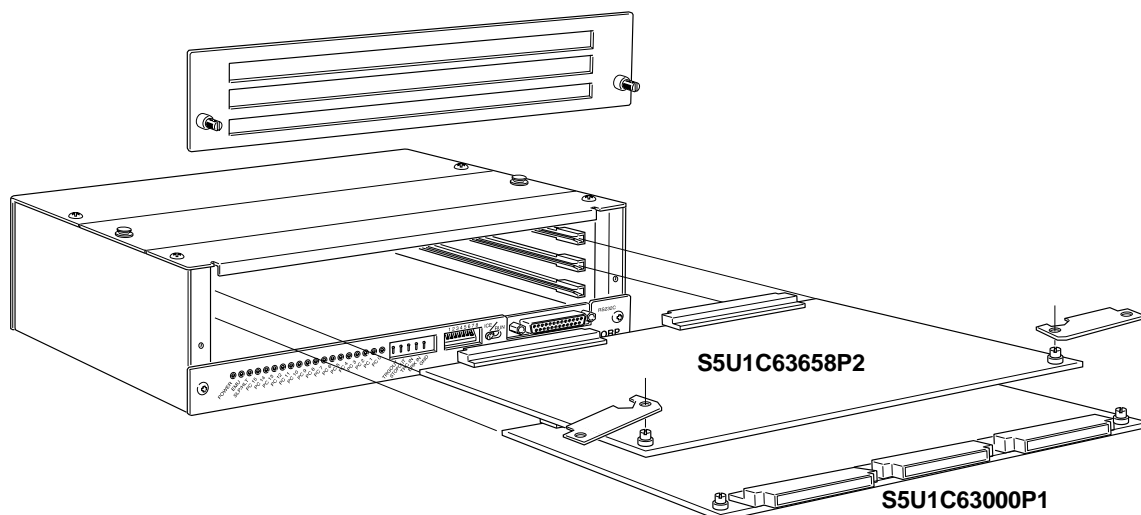
Do not mount an AC bias sensor and a DC bias sensor at the same time as it causes a malfunction.



## A.2 Connecting to the Target System

This section explains how to connect the S5U1C63000P1 to the target system.

First insert the S5U1C63658P2 board into the top slot of the ICE and the S5U1C63000P1 (S5U1C63000P6) board into the second upper slot.



(when the S5U1C63000H1/S5U1C63000H2 and S5U1C63000P1 are used)

Fig. A.2.1 Installing the peripheral circuit boards to the ICE

### • Installing the S5U1C63000P1 (S5U1C63000P6), S5U1C63658P2 board

Set the jig included with the ICE into position as shown in Figure A.2.2. Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the board has been firmly fitted into the internal slot of the ICE, remove the jig.

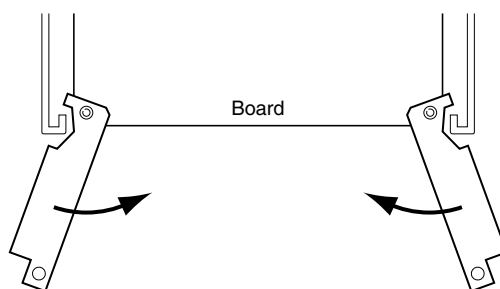


Fig. A.2.2  
Installing the board

### • Dismounting the S5U1C63000P1 (S5U1C63000P6), S5U1C63658P2 board

Set the jig included with the ICE into position as shown in Figure A.2.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides. After confirming that the board has been dismounted from the backboard connector, pull the board out of the ICE.

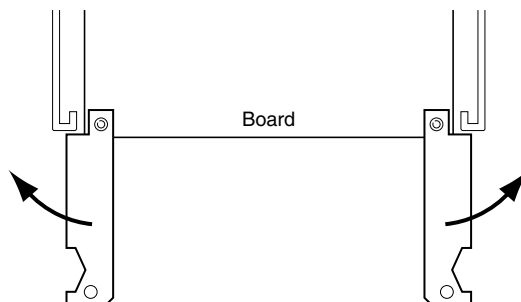


Fig. A.2.3  
Dismounting the board

To connect the S5U1C63000P1 (S5U1C63000P6) board to the target system, use the I/O connecting cables supplied with the board (80-pin/40-pin  $\times$  2, 100-pin/50-pin  $\times$  2, flat type). Take care when handling the connectors, since they conduct electrical power ( $V_{DD} = +3.3$  V).

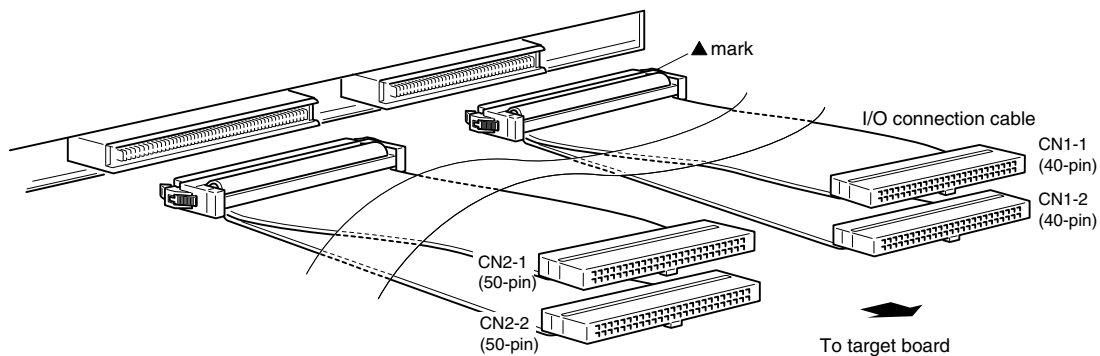


Fig. A.2.4 Connecting to the target system

Table A.2.1 I/O connector pin assignment

40-pin CN1-1 connector		40-pin CN1-2 connector		50-pin CN2-1 connector		50-pin CN2-2 connector	
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VDD (= 3.3 V)	1	VDD (= 3.3 V)	1	VDD (= 3.3 V)	1	VDD (= 3.3 V)
2	VDD (= 3.3 V)	2	VDD (= 3.3 V)	2	VDD (= 3.3 V)	2	VDD (= 3.3 V)
3	K00	3	R00	3	SEG0 (DC)	3	SEG40 (DC)
4	K01	4	R01	4	SEG1 (DC)	4	SEG41 (DC)
5	K02	5	R02	5	SEG2 (DC)	5	SEG42 (DC)
6	K03	6	R03	6	SEG3 (DC)	6	SEG43 (DC)
7	K10	7	R10	7	SEG4 (DC)	7	SEG44 (DC)
8	K11	8	R11	8	SEG5 (DC)	8	SEG45 (DC)
9	K12	9	R12	9	SEG6 (DC)	9	SEG46 (DC)
10	K13	10	R13	10	SEG7 (DC)	10	SEG47 (DC)
11	Vss	11	Vss	11	Vss	11	Vss
12	Vss	12	Vss	12	Vss	12	Vss
13	P00	13	BZ	13	SEG8 (DC)	13	SEG48 (DC)
14	P01	14	$\overline{\text{BZ}}$	14	SEG9 (DC)	14	SEG49 (DC)
15	P02	15	Cannot be connected	15	SEG10 (DC)	15	SEG50 (DC)
16	P03	16	Cannot be connected	16	SEG11 (DC)	16	SEG51 (DC)
17	P10	17	Cannot be connected	17	SEG12 (DC)	17	SEG52 (DC)
18	P11	18	Cannot be connected	18	SEG13 (DC)	18	SEG53 (DC)
19	P12	19	Cannot be connected	19	SEG14 (DC)	19	SEG54 (DC)
20	P13	20	Cannot be connected	20	SEG15 (DC)	20	SEG55 (DC)
21	VDD (= 3.3 V)	21	VDD (= 3.3 V)	21	VDD (= 3.3 V)	21	VDD (= 3.3 V)
22	VDD (= 3.3 V)	22	VDD (= 3.3 V)	22	VDD (= 3.3 V)	22	VDD (= 3.3 V)
23	Cannot be connected	23	Cannot be connected	23	SEG16 (DC)	23	Cannot be connected
24	Cannot be connected	24	Cannot be connected	24	SEG17 (DC)	24	Cannot be connected
25	Cannot be connected	25	Cannot be connected	25	SEG18 (DC)	25	Cannot be connected
26	Cannot be connected	26	Cannot be connected	26	SEG19 (DC)	26	Cannot be connected
27	Cannot be connected	27	Cannot be connected	27	SEG20 (DC)	27	Cannot be connected
28	Cannot be connected	28	Cannot be connected	28	SEG21 (DC)	28	Cannot be connected
29	Cannot be connected	29	Cannot be connected	29	SEG22 (DC)	29	Cannot be connected
30	Cannot be connected	30	Cannot be connected	30	SEG23 (DC)	30	Cannot be connected
31	Vss	31	Vss	31	Vss	31	Vss
32	Vss	32	Vss	32	Vss	32	Vss
33	Cannot be connected	33	Cannot be connected	33	SEG24 (DC)	33	Cannot be connected
34	Cannot be connected	34	Cannot be connected	34	SEG25 (DC)	34	Cannot be connected
35	Cannot be connected	35	Cannot be connected	35	SEG26 (DC)	35	Cannot be connected
36	Cannot be connected	36	Cannot be connected	36	SEG27 (DC)	36	Cannot be connected
37	Cannot be connected	37	Cannot be connected	37	SEG28 (DC)	37	Cannot be connected
38	Cannot be connected	38	RESET	38	SEG29 (DC)	38	Cannot be connected
39	Vss	39	Vss	39	SEG30 (DC)	39	Cannot be connected
40	Vss	40	Vss	40	SEG31 (DC)	40	Cannot be connected
				41	VDD (= 3.3 V)	41	VDD (= 3.3 V)
				42	VDD (= 3.3 V)	42	VDD (= 3.3 V)
				43	SEG32 (DC)	43	Cannot be connected
				44	SEG33 (DC)	44	Cannot be connected
				45	SEG34 (DC)	45	Cannot be connected
				46	SEG35 (DC)	46	Cannot be connected
				47	SEG36 (DC)	47	Cannot be connected
				48	SEG37 (DC)	48	Cannot be connected
				49	SEG38 (DC)	49	Cannot be connected
				50	SEG39 (DC)	50	Cannot be connected

\* Connectors CN2-1 and CN2-2 are used when the SEG pins are set for DC output by mask option.

### A.3 Downloading to S5U1C63000P1/S5U1C63000P6

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#### A.3.1 Downloading circuit data – when ICE (S5U1C63000H2/S5U1C63000H6) is used

The S5U1C63000P1/S5U1C63000P6 board comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

- 1) Remove the ICE top cover and then set the DIP switch "IOSEL2" on the S5U1C63000P1/S5U1C63000P6 board to the "E" position.
- 2) Connect the ICE to the host PC. Then turn the host PC and ICE on.
- 3) Invoke the debugger included in the assembler package (ver. 5 or later). For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
- 4) Download the circuit data file (.mot) corresponding to the model by entering the following commands in the command window.

```
>XFER                (erase all)
>XFWR <file name>    (download the specified file)*
>XFCP <file name>    (compare the specified file and downloaded data)
```

\* The downloading takes about 15 minutes.

- 5) Terminate the debugger and then turn the ICE off.
- 6) Set the DIP switch "IOSEL2" on the S5U1C63000P1/S5U1C63000P6 board to the "D" position.
- 7) Turn the ICE on and invoke the debugger again. Debugging can be started here.

## A.4 Usage Precautions

To ensure correct use of the peripheral circuit board, please observe the following precautions.

### A.4.1 Operational precautions

- (1) Before inserting or removing cables, turn off power to all pieces of connected equipment.
- (2) Do not turn on power or load mask option data if all of the input ports (K00–K03) are held low. Doing so may activate the multiple key entry reset function.
- (3) Before debugging, always be sure to load mask option data.

### A.4.2 Differences with the actual IC

#### (1) Differences in I/O

##### *<Interface power supply>*

S5U1C63000P1/S5U1C63000P6 and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter circuit, etc. on the target system side to accommodate the required interface voltage.

##### *<Each output port's drive capability>*

The drive capability of each output port on S5U1C63000P1/S5U1C63000P6 is higher than that of the actual IC. When designing application system and software, refer to Chapter 7, "Electrical Characteristics", to confirm each output port's drive capability.

##### *<Each port's protective diode>*

All I/O ports incorporate a protective diode for VDD and VSS, and the interface signals between S5U1C63000P1/S5U1C63000P6 and the target system are set to +3.3 V. Therefore, S5U1C63000P1/S5U1C63000P6 and the target system cannot be interfaced with voltages exceeding VDD by setting the output ports for open-drain mode.

##### *<Pull-down resistance value>*

The pull-down resistance values on S5U1C63000P1/S5U1C63000P6 are set to 220 k $\Omega$  which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "Electrical Characteristics".

Note that when using pull-down resistors to pull the input pins low, the input pins may require a certain period to reach a valid low level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since fall delay times on these input ports differ from those of the actual IC.

#### (2) Differences in current consumption

The amount of current consumed by the peripheral circuit boards differ significantly from that of the actual IC. Inspecting the LEDs on S5U1C63000P1/S5U1C63000P6 may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

##### *<Those which can be verified by LEDs and monitor pins>*

- a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
- b) Logic system power select circuit (VDC0)
- c) High-speed operation voltage regulator circuit (VDC1)
- d) Low-speed operation voltage regulator power select circuit (VDC2)
- e) LCD system voltage regulator power select circuit (VDC3)
- f) OSC3 oscillation on/off circuit (OSCC)
- g) CPU clock select circuit (CLKCHG)
- h) LCD power supply on/off circuit (LPWR)
- i) R/f converter oscillation on/off circuit (RFOUT)

##### *<Those that can only be counteracted by system or software>*

- j) Current consumed by the internal pull-down resistors
- k) Input ports in a floating state

**(3) Functional precautions****<LCD power supply circuit>**

There is a finite delay time from the point at which the LCD power supply circuit (LPWR) turns on until an LCD drive waveform is output. On S5U1C63000P1/S5U1C63000P6, this delay is set to approx. 100 msec, which differs from that of the actual IC.

**<Differences in LCD drive waveform>**

This board is capable of static waveform output even if the internal LCD power supply is used. However, select 1/2-bias external power supply by mask option when driving the LCD with the static waveform.

**<Oscillation circuit>**

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. On S5U1C63000P1/S5U1C63000P6, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with S5U1C63000P1/S5U1C63000P6, may not function properly well with the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on S5U1C63000P1/S5U1C63000P6 differs from that of the actual IC.
- S5U1C63000P1/S5U1C63000P6 contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, its emulator can operate with the OSC3 circuit.
- Do not turn on the OSC3 oscillation circuit when the voltage-regulating circuit for high-speed operation remains idle.
- S5U1C63000P1/S5U1C63000P6 generates the OSC3 clock using the onboard CR oscillation circuit even if ceramic oscillation is selected for the OSC3 oscillation circuit by mask option.

**<Access to undefined address space>**

If any undefined space in the S1C63657's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between S5U1C63000P1/S5U1C63000P6 and the actual IC. Note that the ICE (S5U1C63000H1/S5U1C63000H2/S5U1C63000H6) incorporates the program break function caused by accessing to an undefined address space.

**<Reset circuit>**

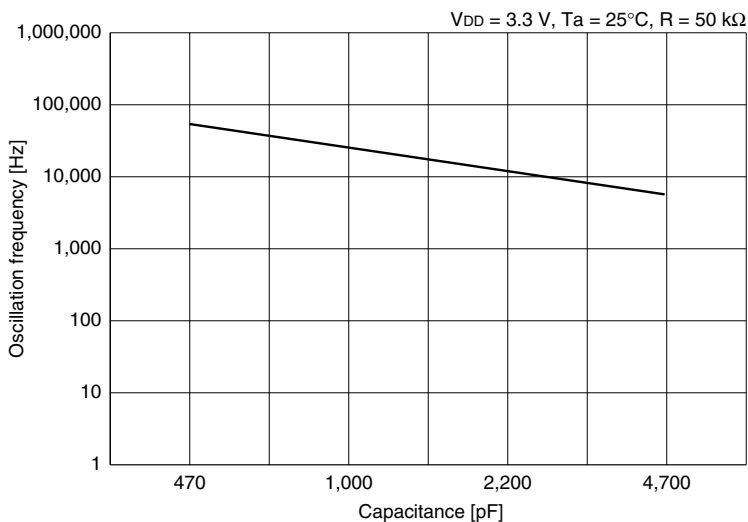
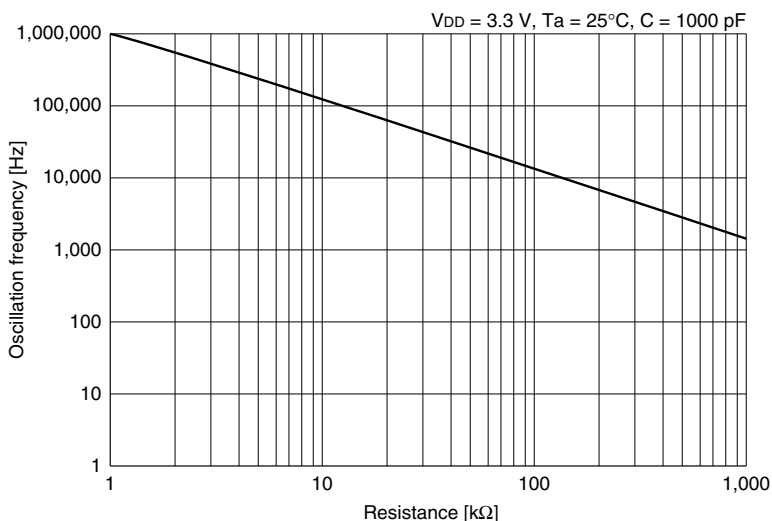
Keep in mind that the operation sequence from when the ICE and the peripheral circuit boards are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because S5U1C63000P1/S5U1C63000P6 becomes capable of operating as a debugging system after the user program and optional data are downloaded. When operating the ICE after placing it in free-running mode, always apply a system reset. A system reset can be performed by pressing the reset switch on S5U1C63000P1/S5U1C63000P6, by a reset pin input, or by holding the input ports high simultaneously.

**<Internal power supply circuit>**

- Although S5U1C63000P1/S5U1C63000P6 contains VDC0–VDC3 registers, it does not actually exercise power supply control by these registers. Refer to Section 4.4, "Oscillation Circuit", when setting the correct voltage. Also, when switching the control voltages, consult the technical manual to determine the appropriate wait time to be inserted.
- The LCD drive voltage on this board is different from that on the actual IC.
- Since the usable operating frequency range depends on the device's internal operating voltage, refer to Section 2.1, "Power Supply", to ensure that the device will not be operated with an inappropriate combination of the operating frequency and the internal power supply.

**<R/f converter>**

- If the debugger breaks executing of the target program while the R/f converter is counting the oscillation, the R/f converter stops counting. Note that the R/f converter will not be able to load a proper result if the count operation is resumed from that point.
- The signal polarity of the R/f converter oscillation frequency output (RFOUT) is inverted. RFOUT of the S5U1C63658P2 is active High and that of the actual IC is active Low. Pay attention when using the output signal for a purpose other than measurement of the oscillation frequency.
- The following shows the oscillation characteristics (reference value) of the R/f converter on the S5U1C63658P2:

**R/f converter oscillation frequency - capacitance characteristic****R/f converter oscillation frequency - resistance characteristic**

## A.5 Product Specifications

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### A.5.1 Specifications of S5U1C63000P1

#### S5U1C63000P1

Dimension:	254 mm (wide) × 144.8 mm (depth) × 13 mm (height) (including screws)
Weight:	Approx. 300 g
Power supply:	DC 5 V ± 5%, less than 1 A (supplied from ICE main unit)

#### I/O connection cable (80-pin)

S5U1C63000P1 connector:	KEL 8830E-080-170L	
Cable connector (80-pin):	KEL 8822E-080-171	
Cable connector (40-pin):	3M 7940-6500SC	1 pair
Cable:	40-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

#### I/O connection cable (100-pin)

S5U1C63000P1 connector:	KEL 8830E-100-170L	
Cable connector (100-pin):	KEL 8822E-100-171	
Cable connector (50-pin):	3M 7950-6500SC	1 pair
Cable:	50-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

#### Accessories

40-pin connector for connecting to target system:	3M 3432-6002LCSC × 2
50-pin connector for connecting to target system:	3M 3433-6002LCSC × 2

### A.5.2 Specifications of S5U1C63000P6

#### S5U1C63000P6

Dimension:	254 mm (wide) × 144.8 mm (depth) × 16 mm (height) (including screws)
Weight:	Approx. 250 g
Power supply:	DC 5 V ± 5%, less than 1 A (except inrush current at power-on)

#### I/O connection cable (80-pin)

S5U1C63000P6 connector:	KEL 8830E-080-170L-F	
Cable connector (80-pin):	KEL 8822E-080-171-F	
Cable connector (40-pin):	3M 7940-6500SC	1 pair
Cable:	40-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

#### I/O connection cable (100-pin)

S5U1C63000P6 connector:	KEL 8830E-100-170L-F	
Cable connector (100-pin):	KEL 8822E-100-171-F	
Cable connector (50-pin):	3M 7950-6500SC	1 pair
Cable:	50-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

#### Accessories

40-pin connector for connecting to target system:	3M 3432-6002LCPL × 2
50-pin connector for connecting to target system:	3M 3433-6002LCPL × 2



### *A.5.3 Specifications of S5U1C63658P2*

#### **S5U1C63658P2**

Dimension:	254 mm (width) × 144.8 mm (depth) × 13 mm (height) (including screws)
Weight:	Approx. 130 g
Power supply:	DC 5 V ± 5%, less than 10 mA (supplied from ICE main unit and converted into 3.3 V by the onboard regulator)

#### **Accessory**

Discreet platform (for mounting external resistors and capacitors of the R/f converter):
DIS12-016-403 (KEL) × 2

# EPSON

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