Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK™" FAMILY

32K x 16/32K x 16 CMOS SRAM/EEPROM MODULE

PRELIMINARY
IDT7M7005

FEATURES:

- High-density CMOS module with SRAM and EEPROM memory on-board
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules, with equivalent pin-outs, supporting a wide range of applications.
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
  - — 25ns (max.) commercial SRAM
  - — 30ns (max.) military SRAM
  - — 75ns (max.) commercial EEPROM
  - — 95ns (max.) military EEPROM
- Low power CMOS operation
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Offered in a 66-pin HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Please consult the factory regarding the number of Erase/ Write Cycles per Byte Minimum available on the module

DESCRIPTION:

The IDT7M7005 is a high-speed, high-density CMOS module with both SRAM & EEPROM memory on-board. It is constructed on a multi-layer, co-fired ceramic substrate using 32K x 8 SRAM or EEPROM components in leadlesss chip carriers.

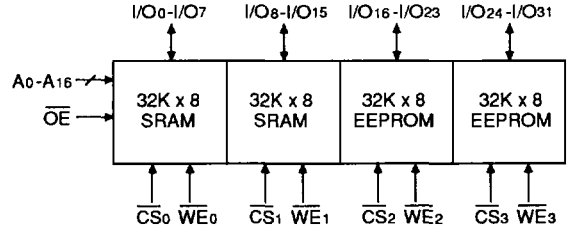
These modules are part of the IDT Subsystems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmmable memory or those applications needing a combination of both. All of these module configurations have equivalent pin-outs, making them "plug-in compatible" with each other, suitable for a wide range of applications.

The IDT7M7005 is available with SRAM access times as fast as 25ns over the commercial temperature range and 30ns over the military temperature range and EEPROM access times as fast as 75ns over the commercial temperature range and 95ns over the military temperature range.

These modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and fits the SRAM/EEPROM memory into 1 sq. inch of board space.

All military IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

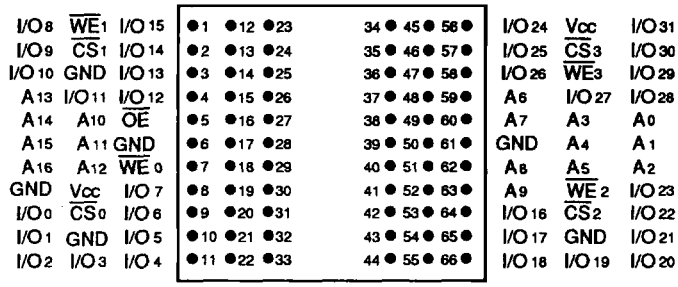
FUNCTIONAL BLOCK DIAGRAM



2826 drw 01

Flexi-Pak is a Trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS [1, 2]



2826 drw 02

HIP
TOP VIEW

NOTES:
1. For module dimensions, please refer to the module drawings in the packaging section.
2. For the IDT7M7005 (32K x 16/32K x 16) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
$\overline{WE}$ 0-1	RAM Write Enables
$\overline{WE}$ 2-3	EEPROM Write Enables
$\overline{CS}$ 0-1	RAM Chip Selects
$\overline{CS}$ 2-3	EEPROM Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2826 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2826 tbl 06

B

TRUTH TABLE [1]

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	note 1	L	DIN	Active
Read	L	H	H	High Z	Active

2826 tbl 02

NOTE:
1. For the SRAM array $\overline{OE}$ = X (don't care); however, for the EEPROM array $\overline{OE}$ = H (high).

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN (1)	Input Capacitance (Data, $\overline{CS}$, $\overline{WE}$)	VIN = 0V	12	pF
CIN (2)	Input Capacitance (Address, $\overline{OE}$)	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	15	pF

2826 tbl 03

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2826 tbl 05

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2826 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (EEPROM)

(V_{CC} = 5V ± 10%, T_A =-55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Dynamic Operating Current	f = 5 MHz, I_{OUT} = 0 mA V_{CC} = Max.	—	160	mA
I_{SB}	Standby Supply Current (TTL)	$\overline{CS}$ ≥ 2V to V_{CC} + 1V	—	6	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 6mA	—	0.45	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2826 tbl 07

DC ELECTRICAL CHARACTERISTICS (SRAM)

Symbol	Parameter	Test Conditions	Min.	Max.[1]	Max.[2]	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	10	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	10	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL} f = f_{MAX}, Output Open	—	400	440	mA
I_{SB}	Standby Supply Curent	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} f = f_{MAX}, Output Open	—	40	140	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or < 0.2V	—	40	40	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	—	V

NOTES:
1. For T_A = 0°C to +70°C versions only.
2. For T_A = -55°C to +125°C versions only.

2826 tbl 06

AC TEST CONDITIONS (EEPROM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2826 tbl 08

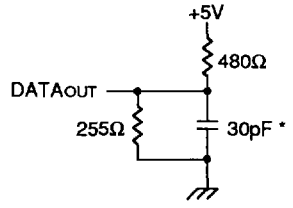
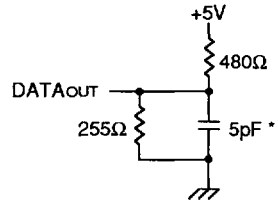


Figure 1. Output Load



2826 drw 03

Figure 2. Output Load (for tCHZ)

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS (EEPROM)

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameters	7M7005Sxx/xxCH 7M7005Sxx/xxCHB -75 Min.	-75 Max.	-95 Min.	-95 Max.	-125 Min.	-125 Max.	-150 Min.	-150 Max.	-200 Min.	-200 Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	75	—	95	—	125	—	150	—	200	—	ns
tAA	Address Access Time	—	75	—	95	—	125	—	150	—	200	ns
tACS	Chip Select Access Time	—	75	—	95	—	125	—	150	—	200	ns
tOE	Output Enable to Output Valid	—	40	—	50	—	55	—	70	—	80	ns
tCHZ (1)	Chip Select to Output in High Z	0	40	0	50	0	55	0	55	0	60	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
tAH	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
tWP	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
tCS	$\overline{CS}$ Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tCH	$\overline{CS}$ Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tDS	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
PAGE MODE WRITE CYCLE												
tWC	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
tAH	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
tAS	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
tDS	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
tBLC	Byte Load Cycle Time	0.2	200	0.2	200	0.2	200	0.2	200	0.2	200	µs
tWPH	Write Pulse Width High	55	—	55	—	55	—	55	—	55	—	ns
DATA POLLING CYCLE												
tDH (1)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ms
tOEH (1)	Output Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOE (1)	Output Enable to Output Delay	—	100	—	100	—	100	—	100	—	100	ns
tWR (1)	Write Recovery Time	2	—	2	—	2	—	2	—	2	—	ns

2826 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

B

AC TEST CONDITIONS (SRAM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2826 tbl 08

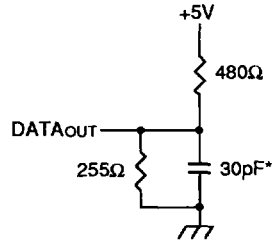


Figure 1. Output Load

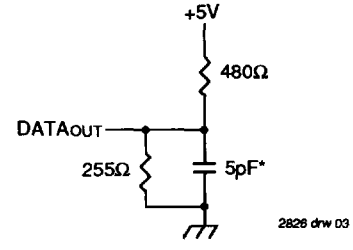


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS (SRAM)

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	7M7005Sxx/xxCH 7M7005Sxx/xxCHB										Unit
		-25		-30		-35		-40		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	13	—	15	—	20	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	12	—	15	—	17	—	20	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	12	—	13	—	15	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	20	—	23	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	12	—	13	—	17	—	20	—	20	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	16	—	16	—	20	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2826 tbl 08

AC ELECTRICAL CHARACTERISTICS (SRAM CONTINUED)

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	7M7005Sxx/xxCH 7M7005Sxx/xxCHB										Unit
		-50		-60		-70		-85		-100		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	30	—	35	—	40	—	45	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	45	—	55	—	65	—	80	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	2	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

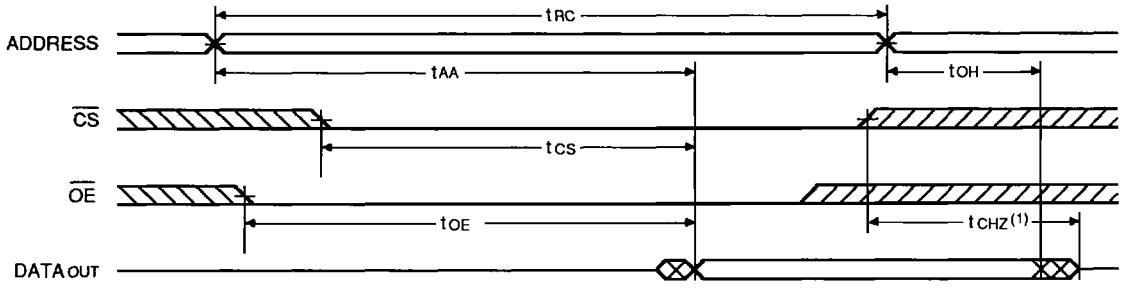
NOTE:
1. This parameter is guaranteed by design, but not tested.

2826 tbl 09

B

EEPROM TIMING WAVEFORMS

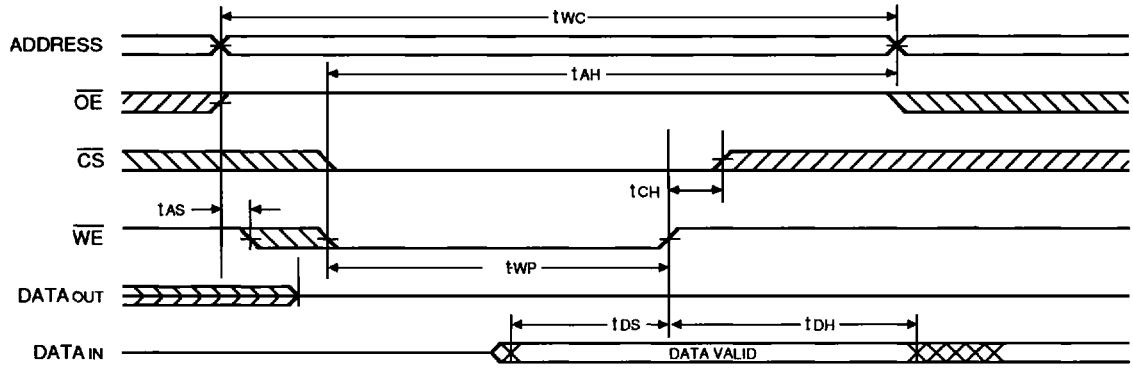
TIMING WAVEFORM OF READ CYCLE[1]



2826 drw 04

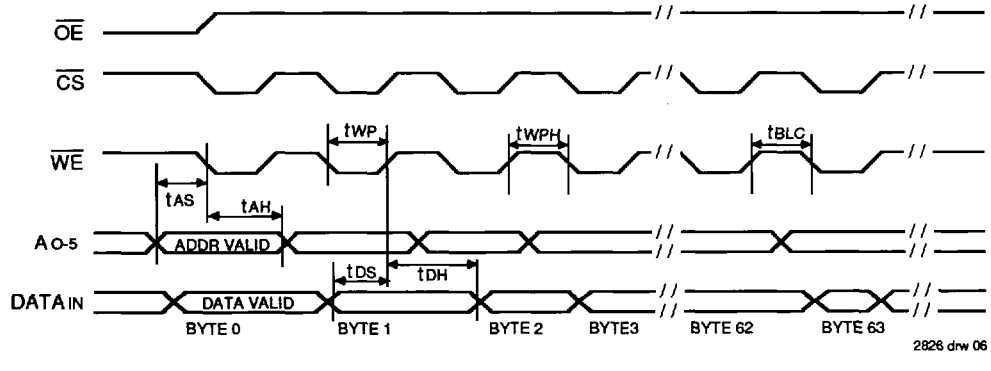
NOTES:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



2826 drw 05

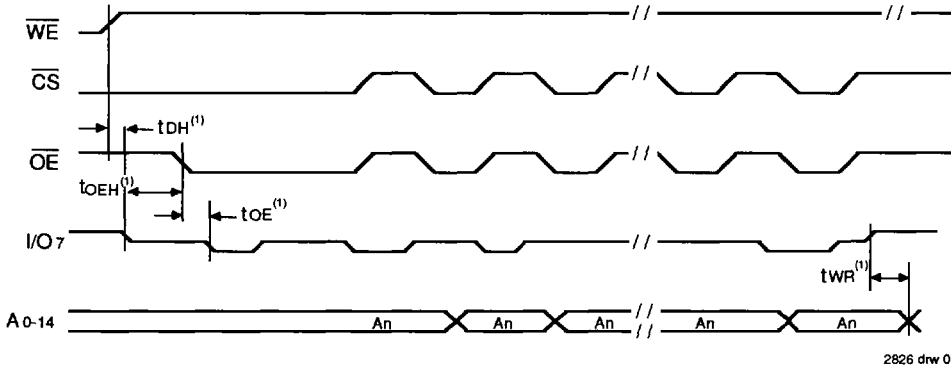
TIMING WAVEFORM OF PAGE MODE WRITE CYCLE (1)



2826 drw 06

NOTES:
1. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

TIMING WAVEFORM OF $\overline{\text{DATA}}$ POLLING CYCLE

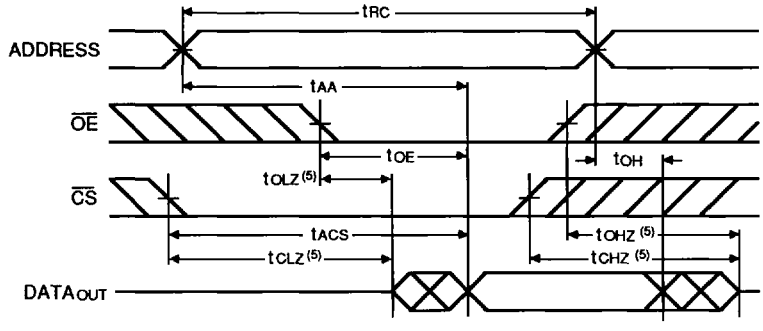


NOTES:
1. This parameter is guaranteed by design but not tested.
2. A6 through A14 must specify the page address during each High to Low transitions of $\overline{\text{WE}}$ (or $\overline{\text{CS}}$). $\overline{\text{OE}}$ must be High only when $\overline{\text{WE}}$ and $\overline{\text{CS}}$ are both Low.

B

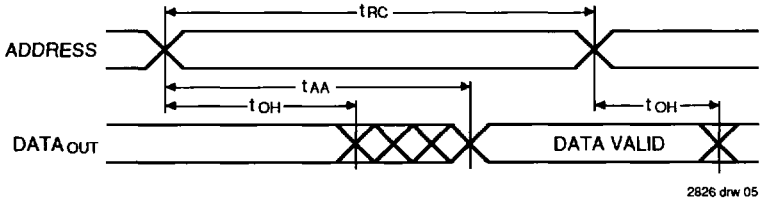
SRAM TIMING WAVEFORMS

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



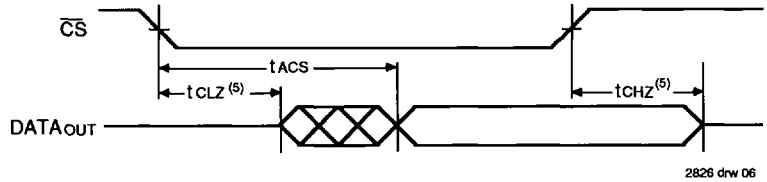
2826 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2826 drw 05

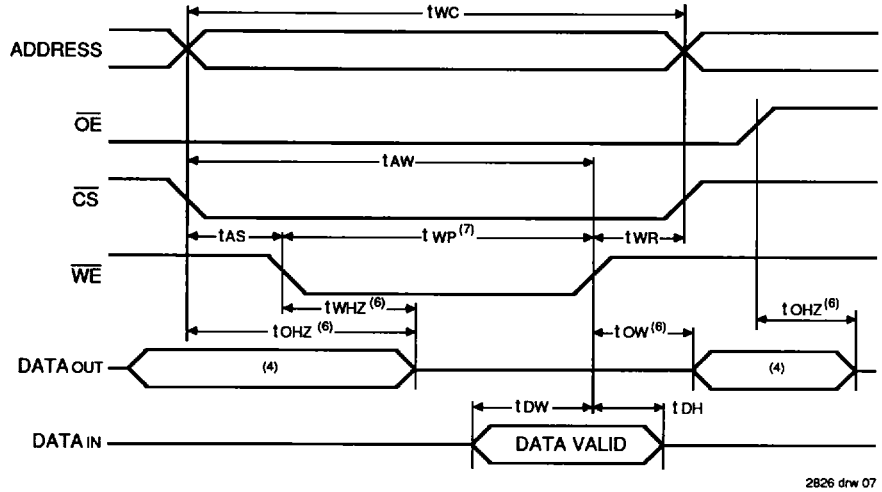
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2826 drw 06

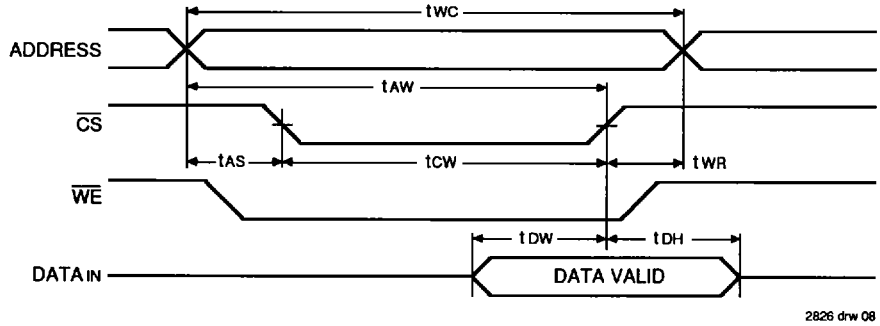
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)



2826 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)

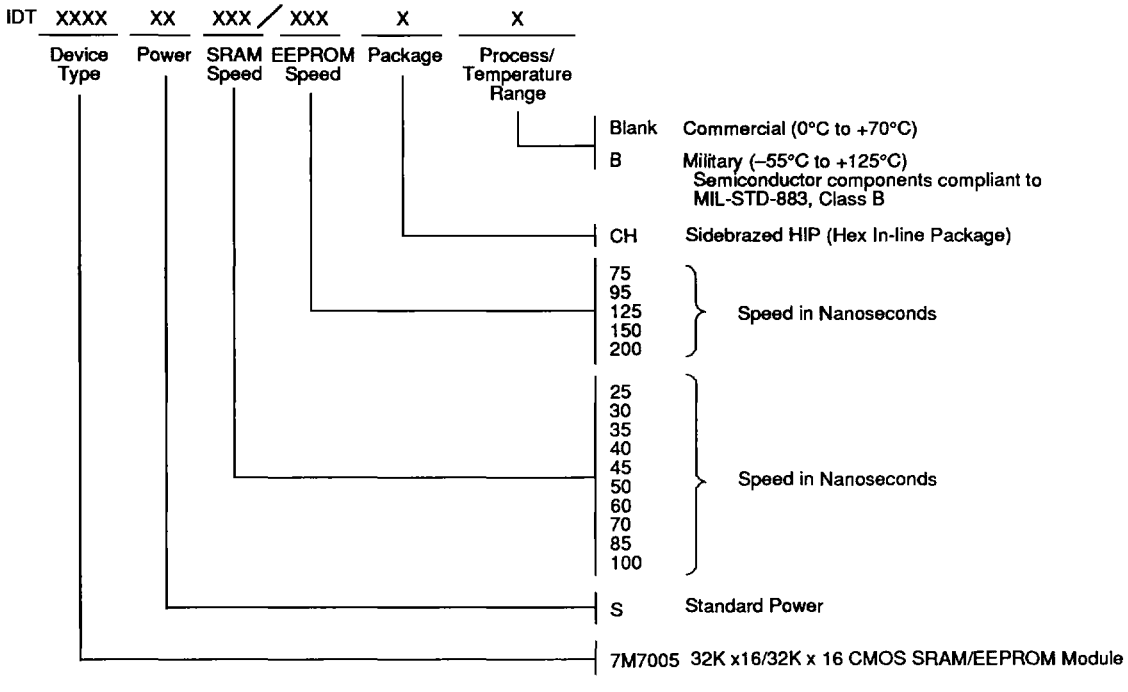


2826 drw 08

B

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

ORDERING INFORMATION



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