Structure Silicon monolithic integrated circuit

Product Name For Home Electoronics and Security Devices IC

Type **BU6566GVW**

Feature Built-in JPEG Codec, VGA Camera Module Interface, and QCIF+ LCD controller interface

• Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage 1 (IO1)	VDDIO1	-0.3～+4.2	V
Supply voltage 2 (IO2)	VDDIO2	-0.3～+4.2	V
Supply voltage 3 (CORE)	VDD	-0.3～+2.1	V
Power dissipation	PD	410*1, 950*2	mW
Other terminals	VIN	-0.3～VDDIO+0.3	V
Storage temperature range	Tstg	-40～+150	°C

*1 IC only. If exceeding 25°C, 4.1mW should be reduced at the rating 1°C.

*2 When packaging a glass epoxy board of 70x70x1.6mm. If exceeding 25°C, 9.5 mW should be reduced at the rating 1°C.

* Anti radiation design is not provided.

* Operation is not guaranteed.

• Operating conditions (Ta=-30°C～+85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage 1 (IO1)	VDDIO1	1.70	1.80	3.15	V
Supply voltage 2 (IO2)	VDDIO2	2.70	2.85	3.15	V
Supply voltage 3 (CORE)	VDD	1.45	1.50	1.55	V
Input "H" voltage 1	VIH1	VDDIOx0.8	-	VDDIO+0.3	V
Input "L" voltage 1	VIL1	-0.3	-	VDDIOx0.2	V
Input "H" voltage 2	VIH2	VDDIOx0.85	-	VDDIO+0.3	V
Input "L" voltage 2	VIL2	-0.3	-	VDDIOx0.15	V
Input voltage range	VIN-VDDIO1,2	-0.3	-	VDDIO+0.3	V

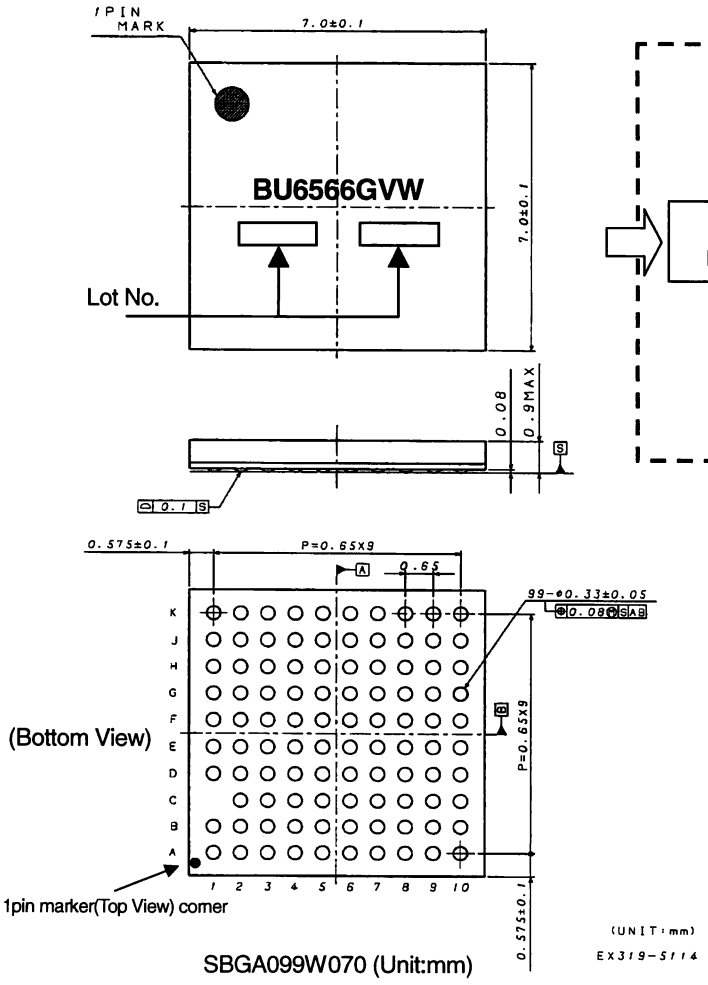
* Supply power in the order of VDD→VDDIO1→VDDIO2.

Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

• Electric Characteristics (Unless otherwise specified, VDD=1.50V, VDDIO=2.85V, GND=0.0V, Ta=25°C, F_{IN} = F_{SYS} =30.0MHz.)

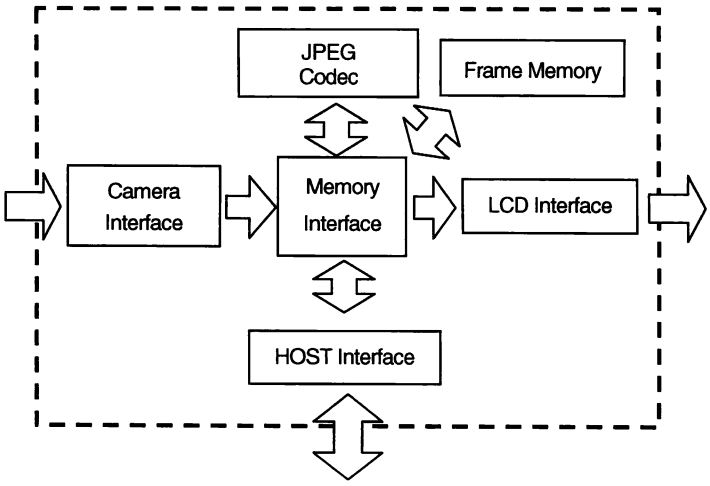
Parameter	Symbol	Specification			Unit	Conditions
		MIN	TYP	MAX		
Input frequency	F_{IN}	-	-	30.0	MHz	XIN(Duty45%~55%)
Internal action frequency 1	F_{SYS}	-	-	30.0	MHz	Internal SCLK frequency
SIF_SCK frequency	F_{SCK}	-	-	26.0	MHz	Serial I/F clock frequency
Action consumption current 1	IDD	-	6.4	-	mA	At camera ON, LCD display ON In viewer operation
Static consumption current	IDDst	-	-	50	uA	When suspend mode is set
Input "H" current 1	IIH1	-10	-	10	uA	VIH=VDDIO
Input "H" current 2	IIH2	25	50	100	uA	Pull-down pin, VIH=VDDIO
Input "H" current 3	IIH3	-10	-	10	uA	Pull-up pin, VIH=VDDIO
Input "L" current 1	IIL1	-10	-	10	uA	VIL=GND
Input "L" current 2	IIL2	-10	-	10	uA	Pull-down pin, VIL=GND
Input "L" current 3	IIL3	-160	-80	-25	uA	Pull-up pin, VIL=GND
Input "H" voltage 1	VIH1	VDDIO x0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O pin)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO x0.2	V	Normal input (including input mode of I/O pin)
Input "H" voltage 2	VIH2	VDDIO x0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Input "L" voltage 2	VIL2	-0.3	-	VDDIO x0.15	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Output "H" voltage 1	VOH1	VDDIO -0.4	-	VDDIO	V	IOH1=-1.0mA(DC) (Including output mode of I/O pin)
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC) (Including output mode of I/O pin))
Output "H" voltage 2	VOH2	VDDIO -0.4	-	VDDIO	V	IOH2=-1.0mA(DC)、XOUT pin
Output "L" voltage 2	VOL2	0.0	-	0.4	V	IOL2=1.0mA(DC)、XOUT pin

• External Dimensional Drawing and Mark Drawing



SBGA099W070 (Unit:mm)

• Block Diagram



Land No.	Pin Name
K2	A1
J1	A2
K8	CAMCKI
K9	CAMCKO
H5	CAMD0
G5	CAMD1
F6	CAMD2
G6	CAMD3
J6	CAMD4
K6	CAMD5
K7	CAMD6
J7	CAMD7
J5	CAMHS
K5	CAMVS
J3	CSB
H1	D0
G3	D1
G2	D2
G1	D3
F1	D4
F2	D5
F3	D6
F4	D7
E3	D8
E2	D9
E1	D10
D1	D11
D2	D12
D3	D13
C2	D14
B1	D15
H6	GIO2/KEY2
K4	INT
F7	KEY0
D5	KEY1
E8	LCDA0
F9	LCDCS1B
F8	LCDCS2B
E10	LCDD0
D10	LCDD1

Land No.	Pin Name
D9	LCDD2
C10	LCDD3
C9	LCDD4
A9	LCDD5
B8	LCDD6/SCL
A8	LCDD7/SI
A7	LCDD8
A6	LCDD9
B6	LCDD10
C6	LCDD11
D6	LCDD12
C5	LCDD13
B5	LCDD14
A5	LCDD15
E7	LCDRDB
E6	LCDWRB
H10	LEDCNT/GIO1
B4	PWM0/GIO0
G8	PWM1/GIO3
G9	PWM2/GIO4
G10	PWM3/GIO5
H4	RDB
A4	RESETB
J10	SDA
H9	SDC
C7	TEST
F10	VD/GIO6
K3	WRB
A2	XIN
B3	XOUT
B7	X16_8

Land No.	Pin Name
F5	VDD
J9	
B9	
B2	VDDIO1
J2	
C4	
H7	VDDIO2
E9	
E4	GND
G4	
G7	
D7	
D4	
A1	N.C.
C1	
H2	
H3	
K1	
J4	
J8	
H8	
K10	
D8	
B10	
C8	
A10	
E5	
A3	
C3	

• Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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