National Semiconductor

54F/74F548
Octal Decoder/Demultiplexer with Acknowledge

General Description

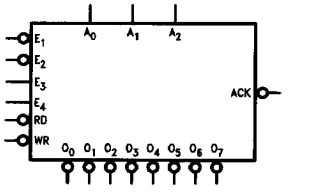
The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are Active LOW and two are Active HIGH for maximum addressing versatility. Also provided is an Active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

Features

- 3-to-8 line address decoder
- Multiple enables for address extension
- Open collector acknowledge output
- Active LOW decoder outputs

Ordering Code: See Section 5

Logic Symbols



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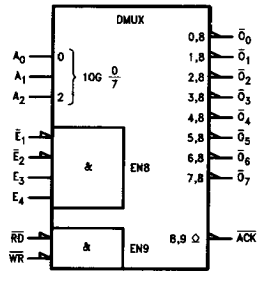
IEEE/IEC



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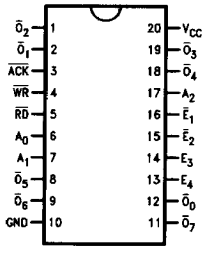
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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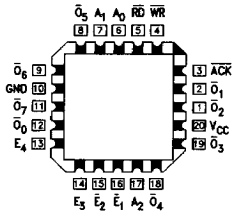
Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_2	Output Select Address Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{E}_1$, $\overline{E}_2$	Chip Enable Inputs (Active LOW)	1.0/1.0	20 μA/−0.6 mA
E_3, E_4	Chip Enable Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{RD}$	Read Acknowledge Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{WR}$	Write Acknowledge Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{ACK}$	Open Collector Acknowledge Output (Active LOW)	OC*/33.3	*/20 mA
$\overline{O}_0$–$\overline{O}_7$	Decoded Outputs (Active LOW)	50/33.3	−1 mA/20 mA

*OC = Open Collector

Functional Description

When enabled, the 'F548 accepts the A_0–A_2 Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. When one or more Enables is inactive, all decoder outputs are HIGH. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The open collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e., OFF) and goes LOW when the Enables are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

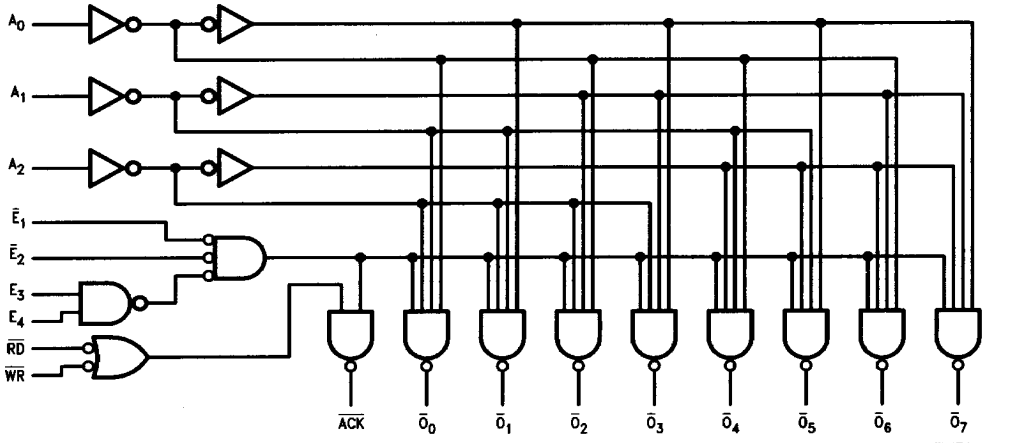
Inputs						Output
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Decoder Truth Table

Inputs							Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA ($\overline{O}_0$–$\overline{O}_7$)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA ($\overline{O}_0$–$\overline{O}_7$)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA ($\overline{O}_0$–$\overline{O}_7$)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V ($\overline{O}_0$–$\overline{O}_7$)
I_{OHC}	Open Collector, Output OFF Leakage Test				250	μA	Min	V_{OUT} = V_{CC} ($\overline{ACK}$)
I_{CCH}	Power Supply Current			14	21	mA	Max	V_O = HIGH

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	2.0 4.0	5.5 8.0	8.0 9.5	3.0 4.0	10.0 12.0	1.5 4.0	9.0 10.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	2.5 3.5	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	2.0 3.0	9.5 9.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to $\overline{O}_n$	4.0 4.0	8.5 8.5	9.5 9.5	5.0 4.0	13.0 12.5	3.0 3.5	10.5 10.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{ACK}$	6.5 3.0	11.0 7.5	12.5 9.5	6.5 3.0	16.5 11.0	6.5 3.0	13.0 10.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to $\overline{ACK}$	8.0 4.0	13.0 8.5	14.0 10.0	8.0 4.0	19.5 13.0	8.0 4.0	15.0 11.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	5.5 2.5	10.0 5.0	12.0 8.0	5.5 2.5	16.5 8.5	5.5 2.5	12.5 8.5	ns	2–3