FS6128-04 / FS6128-05 / FS6128-06

PLL Clock Generator IC with VCXO

1.0 Features

- Phase-locked loop (PLL) device synthesizes output clock frequency from crystal oscillator or external reference clock
- On-chip tunable voltage-controlled crystal oscillator (VCXO) allows precise system frequency tuning
- Typically used for generation of MPEG-2 decoder clock
- 3.3V supply voltage
- Very low phase noise PLL
- Use with “pullable” 14pF crystals – no external padding capacitors required
- Small circuit board footprint (8-pin 0.150″ SOIC)
- Custom frequency selections available - contact your local AMI Sales Representative for more information

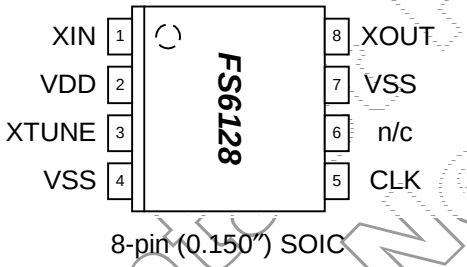
2.0 Description

The FS6128 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

At the core of the FS6128 is circuitry that implements a voltage-controlled crystal oscillator (VCXO) when an external resonator (nominally 13.5MHz) is attached. The VCXO allows device frequencies to be precisely adjusted for use in systems that have frequency matching requirements, such as digital satellite receivers.

A high-resolution phase-locked loop generates an output clock (CLK) through a post-divider. The CLK frequency is ratiometrically derived from the VCXO frequency. The locking of the CLK frequency to other system reference frequencies can eliminate unpredictable artifacts in video systems and reduce electromagnetic interference (EMI) due to frequency harmonic stacking.

Figure 1: Pin Configuration



8-pin (0.150″) SOIC

Table 1: Crystal / Output Frequencies

DEVICE	f_{XIN} (MHz)	CLK (MHz)
FS6128-04	13.500	27.000
FS6128-05	13.500	13.500
FS6128-06	13.500	54.000

NOTE: Contact AMI for custom PLL frequencies

Figure 2: Block Diagram

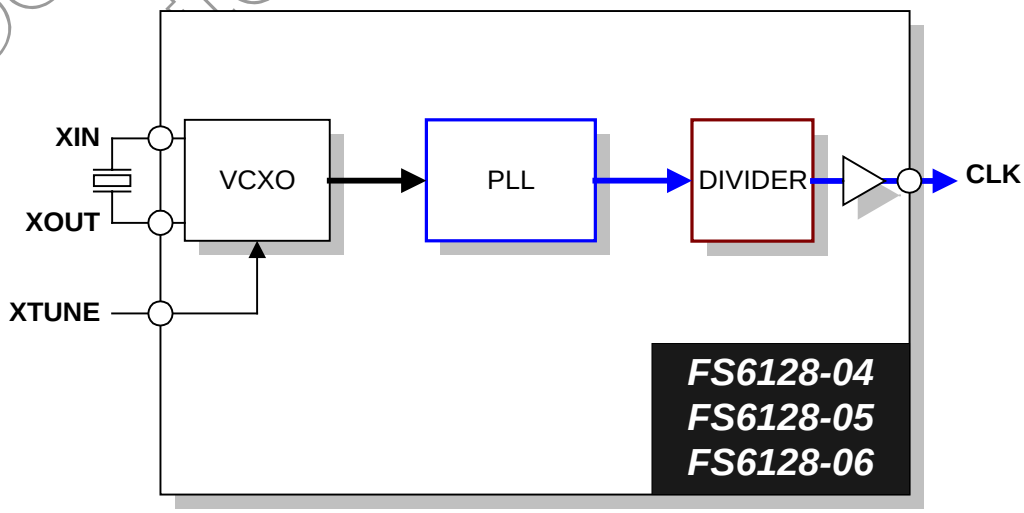


Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	AI	XIN	VCXO Feedback
2	P	VDD	Power Supply (+3.3V)
3	AI	XTUNE	VCXO Tune
4	P	VSS	Ground
5	DO	CLK	Clock Output
6	-	n/c	No Connection
7	DO	VSS	Ground
8	AO	XOUT	VCXO Drive

3.0 Functional Block Description

3.1 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6128 system components. Loading capacitance for the crystal is internal to the FS6128. No external components (other than the resonator itself) are required for operation of the VCXO.

Continuous fine-tuning of the VCXO frequency is accomplished by varying the voltage on the XTUNE pin. The value of this voltage controls the effective capacitance presented to the crystal. The actual amount that this load capacitance change will alter the oscillator frequency depends on the characteristics of the crystal as well as the oscillator circuit itself.

It is important that the crystal load capacitance is specified correctly to "center" the tuning range. See Table 5.

A simple formula to obtain the "pulling" capability of a crystal oscillator is:

$$\Delta f\ (ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where:

C_0 = the shunt (or holder) capacitance of the crystal

C_1 = the motional capacitance of the crystal

C_{L1} and C_{L2} = the two extremes (minimum and maximum) of the applied load capacitance presented by the FS6128.

EXAMPLE: A crystal with the following parameters is used: C_1 = 0.025pF and C_0 = 6pF. Using the minimum and maximum C_{L1} = 10pF, and C_{L2} = 20pF, the tuning range (peak-to-peak) is:

$$\Delta f = \frac{0.025 \times (20 - 10) \times 10^6}{2 \times (6 + 20) \times (6 + 10)} = 300\,ppm.$$

3.2 Phase-Locked Loop (PLL)

The on-chip PLL is a standard frequency- and phase-locked loop architecture. The PLL multiplies the reference oscillator frequency to the desired output frequency by a ratio of integers. The frequency multiplication is exact with a zero synthesis error (unless otherwise specified).

4.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	3.3V ± 10%	3.0	3.3	3.6	V
Ambient Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XTAL}	Fundamental Mode	12	13.5	18	MHz

Table 5: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{XTAL} = 13.5MHz; C_L = 10pF, V_{DD} = 3.6V		30		mA
Supply Current, Static	I_{DD}	XIN = 0V, V_{DD} = 3.6V		3		mA
Voltage Controlled Crystal Oscillator (contact factory for approved crystal sources or other application assistance)						
Crystal Loading Capacitance at Center Tuning Voltage	$C_{L(xtal)}$	Order crystal for this capacitance (parallel load) at desired center frequency		14		pF
Crystal Resonator Motional Capacitance	C_1	Specified motional capacitance of the crystal will affect pullability (see text)		25		fF
XTUNE Effective Range			0		3	V
Synthesized Load Capacitance Min.	C_{L1}	@V(XTUNE)=minimum value		10		pF
Synthesized Load Capacitance Max.	C_{L2}	@V(XTUNE)=maximum value		20		pF
VCXO Tuning Range		f_{XTAL} = 13.5MHz; $C_{L(xtal)}$ = 14pF; $C_{1(xtal)}$ = 25fF (peak-to-peak)		300		ppm
VCXO Tuning Characteristic		Note: positive change of XTUNE = positive change of VCXO frequency		150		ppm/V
Crystal Drive Level		R_{XTAL}=20Ω; C_L = 20pF		200		uW
Clock Output (CLK)						
High-Level Output Source Current *	I_{OH}	V_O = 2.0V		-40		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		17		mA
Output Impedance *	z_{OH}	V_O = 0.1V_{DD}; output driving high		25		Ω
	z_{OL}	V_O = 0.1V_{DD}; output driving low		25		Ω
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-55		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		55		mA

Table 6: AC Timing Specifications

Unless otherwise stated, V_{DD} = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
VCXO Stabilization Time *	$t_{VCXOSTB}$	From power valid		10		ms
PLL Stabilization Time *	t_{PLLSTB}	From VCXO stable		100		us
Synthesis Error		(unless otherwise noted in Frequency Table)			0	ppm
Clock Output (CLK)						
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$) to one clock period	45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$, C_L = 10pF		200		ps
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	From 0-500µs at $V_{DD}/2$, C_L = 10pF compared to ideal clock source		100		ps
Rise Time *	t_r	V_{DD} = 3.3V; V_O = 0.3V to 3.0V; C_L = 10pF		1.7		ns
Fall Time *	t_f	V_{DD} = 3.3V; V_O = 3.0V to 0.3V; C_L = 10pF		1.7		ns

5.0 Package Information

Table 7: 8-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.189	0.196	4.80	4.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

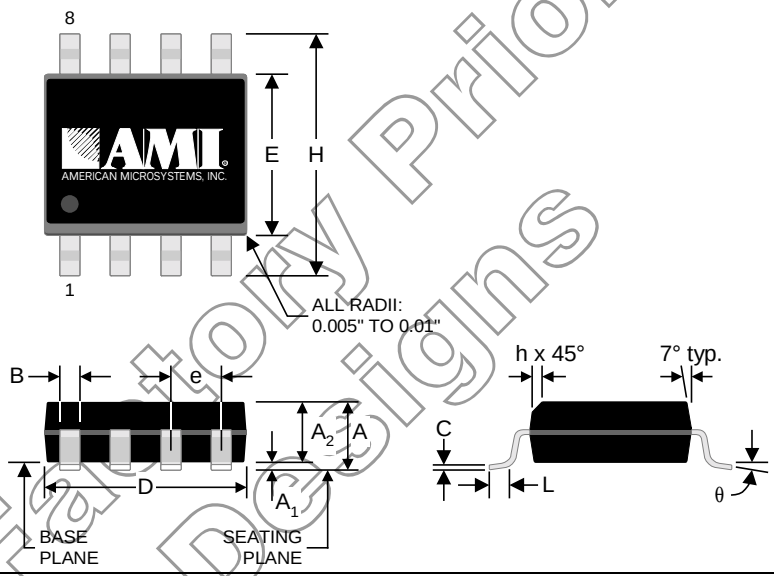


Table 8: 8-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 8-pin 0.150" SOIC	Θ_{JA}	Air flow = 0 m/s	110	°C/W
Lead Inductance, Self	L_{11}	Corner lead	2.0	nH
		Center lead	1.6	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.27	pF

6.0 Ordering Information

Table 9: Device Ordering Codes

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11640-825	FS6128-04	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
11640-835	FS6128-04	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes
11640-102	FS6128-05	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
11640-112	FS6128-05	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes
11640-103	FS6128-06	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
11640-113	FS6128-06	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes

7.0 Revision Information

DATE	PAGE	DESCRIPTION
1/21/00	1	Fixed typographical error
4/24/00	5	Fixed formatting error

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