NEC Electronics Inc.

μPD78224 Family (μPD78220/224/P224) 8-Bit, K-Series Microcontrollers With Analog Comparators, Real-Time Output Ports

August 1993

Description

The μPD78220, μPD78224, and μPD78P224 are members of the K-Series® of microcontrollers. These 8-bit, single-chip microcontrollers contain extended addressing capabilities for up to 1M byte of external memory. The devices also integrate sophisticated analog and digital peripherals as well as two low-power standby modes that make them ideal for low-power/battery backup applications.

The μPD78224 family focuses on embedded control with features such as hardware multiply and divide, two levels of interrupt response, four banks of main registers for multitasking, and macro service for processor-independent peripheral and memory DMA. Augmenting this high-performance core are advanced components; for example, eight analog voltage comparators, two independent serial interfaces, several counter/timers for PWM outputs, and a real-time output port. On board memory includes 640 bytes of RAM and 16K bytes of mask ROM or OTP ROM.

The macro service routine allows data to be transferred between any combination of memory and peripherals independent of the current program execution. The four banks of processor registers allow simplified context switching to be performed. Both features, combined with powerful on-chip peripherals, make the μPD78224 family ideal for a wide variety of embedded control applications.

Features

- Complete single-chip microcontroller
  - 8-bit ALU
  - 16K ROM
  - 640 bytes RAM
  - Both 1-bit and 8-bit logic
- Instruction prefetch queue
- Hardware multiply and divide
- Memory expansion
  - 8085 bus-compatible
  - 64K program address space
  - 1M data address space
- Large I/O capacity: up to 71 I/O port lines
- Extensive timer/counter functions
  - One 16-bit timer/counter/event counter
  - Two 8-bit timer/counter/event counters
- Four timer-controlled PWM channels
- Two 4-bit real-time output ports
- Extensive interrupt handler
  - Vectored interrupt handling
  - Programmable priority
  - Macro service mode
- Two independent serial ports
- Refresh output for pseudostatic RAM
- On-chip clock generator
  - 12-MHz maximum CPU clock frequency
  - 0.33-μs instruction cycle
- CMOS silicon gate technology
- 5-volt power supply

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Ordering Information

Part Number	ROM	Package (Dwg)
μPD78220L	ROMless	84-pin PLCC (P84L-50A3-1)
μPD78224L-xxx	16K mask ROM	
μPD78P224L	16K OTP ROM	
μPD78220GJ-5BG	ROMless	94-pin plastic QFP (S94GJ-80-5BG-1)
μPD78224GJ-xxx-5BG	16K mask ROM	
μPD78P224GJ-5BG	16K OTP ROM	

Pin Identification

Symbol	Function
$P0_0$ - $P0_7$	Output port 0
$P1_0$ - $P1_7$	I/O port 1
$P2_0$/NMI	Input port 2/Nonmaskable interrupt input
$P2_1$ - $P2_2$/INTP0 - INTP1	Input port 2/Ext interrupt input/timer trigger
$P2_3$/INTP2/CI	Input port 2/Ext interrupt input/Clock input
$P2_4$/INTP3	Input port 2/Ext interrupt input/timer trigger
$P2_5$/INTP4	Input port 2/Ext interrupt input
$P2_6$/INTP5	Input port 2/Ext interrupt input
$P2_7$/INTP6/SI	Input port 2/Ext interrupt input/Serial input
$P3_0$/RxD	I/O port 3/Serial receive input
$P3_1$/ TxD	I/O port 3/Serial transmit output
$P3_2$/$\overline{SCK}$	I/O port 3/Serial clock input/output
$P3_3$/SO/SB0	I/O port 3/Serial output/Serial bus I/O
$P3_4$ - $P3_7$/TO0 - TO3	I/O port 3/Timer output
$P4_0$ - $P4_7$/AD_0 - AD_7	I/O port 4/Lower address byte/data bus
$P5_0$ - $P5_7$/A_8 - A_{15}	I/O port 5/Upper address byte

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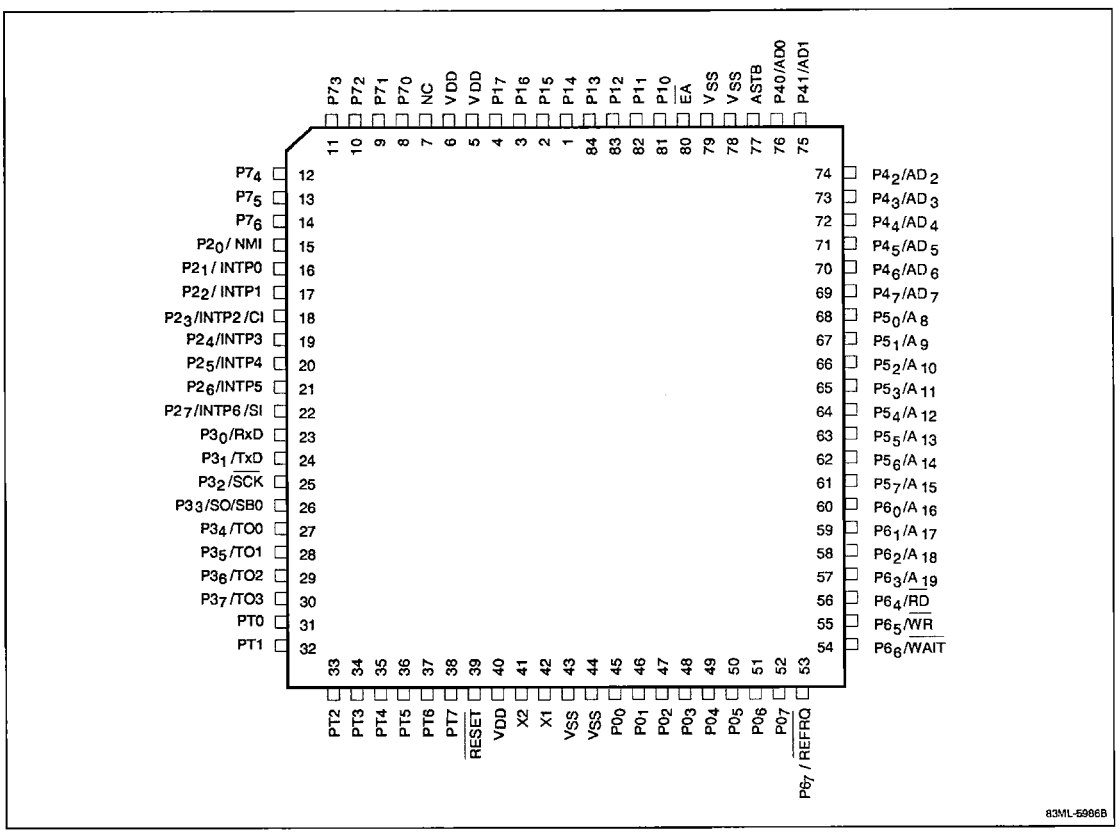
Pin Identification

Symbol	Function
$P6_0$ - $P6_3/A_{16}$ - A_{19}	Output port 6/Extended address nibble
$P6_4/\overline{RD}$	I/O port 6/Read strobe output
$P6_5/\overline{WR}$	I/O port 6/Write strobe output
$P6_6/\overline{WAIT}$	I/O port 6/Wait input
$P6_7/\overline{REFREQ}$	I/O port 6/Rerresh output
$P7_0$ - $P7_6$	I/O port 7
PT0 - PT7	Port T analog inputs to voltage comparators

Symbol	Function
ASTB	Address strobe output
$\overline{RESET}$	External reset input
$\overline{EA}$	External memory access control input
X1, X2	External crystal or external clock input
V_{DD}	Positive power supply input
V_{SS}	Power return; normallly ground
NC	No connection
IC	Internal connection; connect to V_{SS}

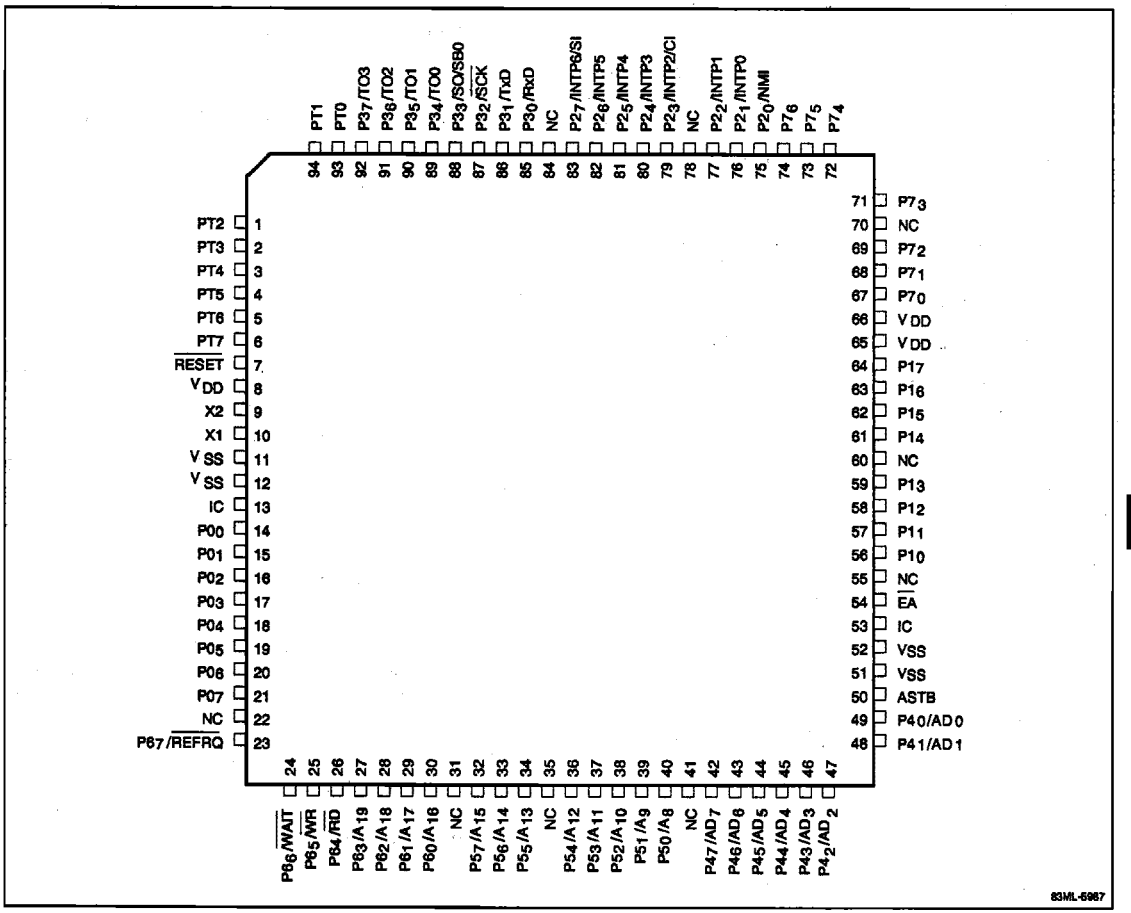
Pin Configurations

84-Pin PLCC



Pin Configurations (cont)

94-Pin Plastic QFP



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Pin Functions

$P0_0$ - $P0_7$. Port 0 is an 8-bit, tristate output port. Port 0 can also be configured as two 4-bit, real-time (timer-controlled) output ports.

$P1_0$ - $P1_7$. Port 1 is an 8-bit bidirectional tristate port. Bits are individually programmable as input/output. Each pin is capable of driving an LED directly (8 mA).

$P2_0$ - $P2_7$. Port 2 is an 8-bit input port.

NMI. Nonmaskable interrupt input.

INTP0 - INTP6. External interrupt inputs. INTP0, INTP1, and INTP3 are timer capture trigger inputs.

CI. External clock input to the timer.

SI. Serial data input for three-line serial I/O mode.

$P3_0$ - $P3_7$. Port 3 is an 8-bit tristate I/O port, each bit programmable as input/output.

RxD. Receive serial data input.

TxD. Transmit serial data output.

$\overline{SCK}$. Serial shift clock output/input.

SO. Serial data output for three-line serial I/O mode.

SB0. I/O bus for the clocked serial interface.

TO0 - TO3. Timer flip-flop outputs

$P4_0$ - $P4_7$. Port 4 is an 8-bit, bidirectional tristate port.

AD_0 - AD_7. Multiplexed address/data bus used with external memory or expanded I/O.

$P5_0$ - $P5_7$. Port 5 is an 8-bit, tristate output port.

A_8 - A_{15}. Upper-order address bus used with external memory or expanded I/O.

$P6_0$ - $P6_3$. Pins $P6_0$ - $P6_3$ of port 6 are outputs.

A_{16} - A_{19}. Extended-order address bus used with external memory.

$P6_4$ - $P6_7$. Pins $P6_4$ - $P6_7$ of port 6 are individually programmable tristate input/output pins.

$\overline{RD}$. Read strobe output used by external memory (or data registers) to place data on the I/O bus during a read operation.

$\overline{WR}$. Write strobe output used by external memory (or data registers) to latch data from the I/O bus during a write operation.

$\overline{WAIT}$. Wait signal input.

$\overline{REFRQ}$. Refresh pulse output used by external pseudostatic memory.

$P7_0$ - $P7_6$. Port 7 has seven individually programmable tristate I/O pins.

PT0 - PT7. Port T is an eight-line input port. The analog voltage on each line is compared continuously with a programmable threshold voltage.

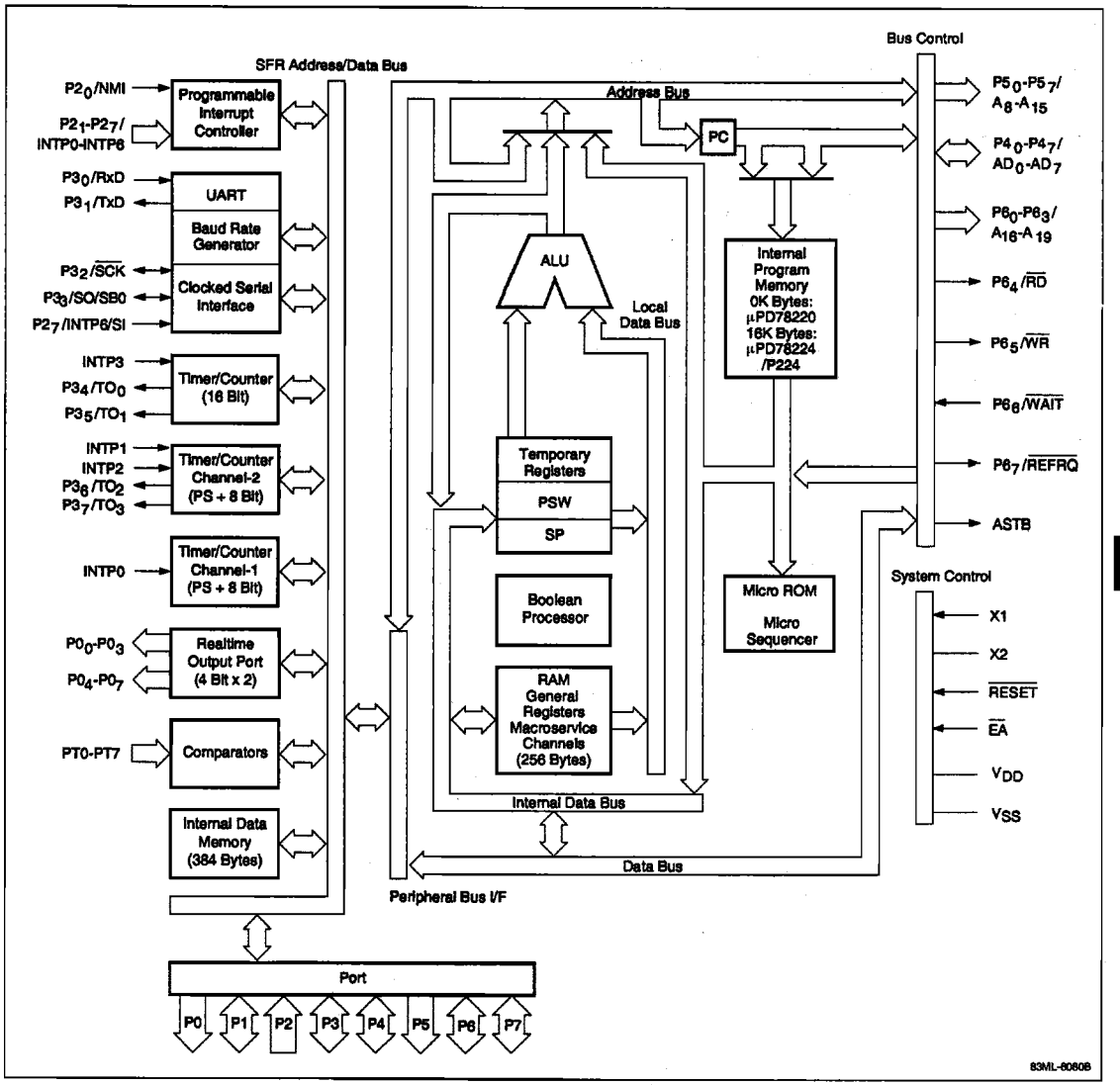
ASTB. Address strobe output used by external circuitry to latch the low-order 8 address bits during the first part of a read or write cycle.

$\overline{RESET}$. A low level on this external reset input sets all registers to their specified reset values. This pin, together with $P2_0$/NMI, sets the μPD78P224 in the PROM programming mode.

$\overline{EA}$. Control signal input that selects external memory or internal ROM as the program memory. When $\overline{EA}$ is low, ROMless mode is initiated and external memory is accessed.

X1, X2. For frequency control of the internal clock oscillator, a crystal is connected to X1 and X2. If the clock is supplied by an external source, the clock signal is connected to X1 and the inverted clock signal is connected to X2.

Block Diagram



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FUNCTIONAL DESCRIPTION

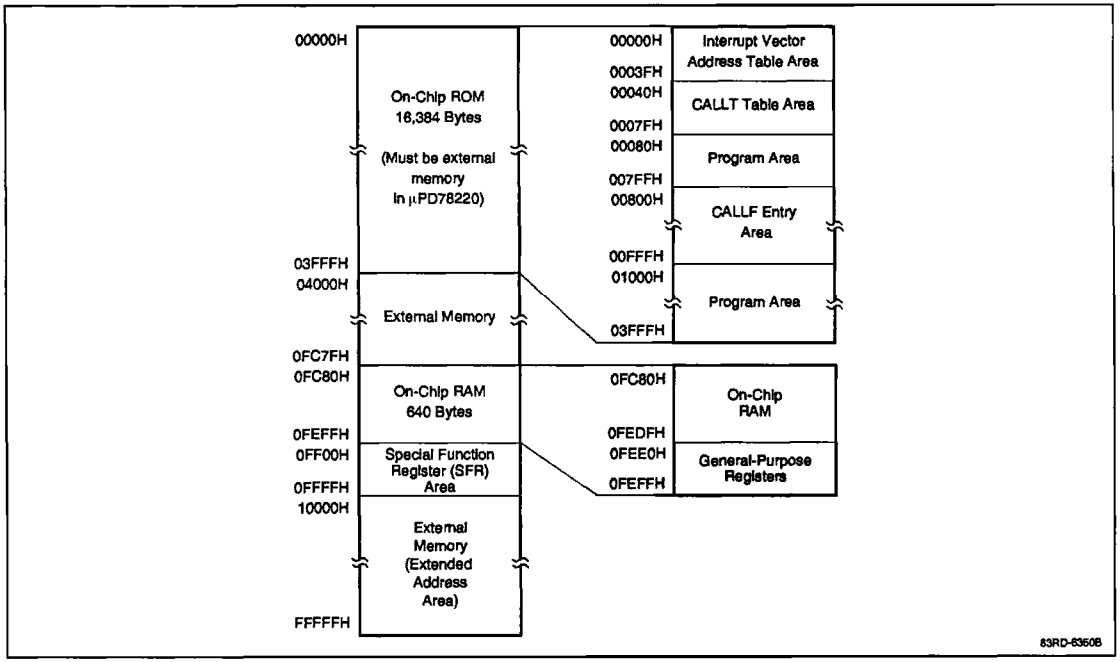
Timing

The maximum clock frequency is 12 MHz. The clock is derived from an external crystal or an external oscillator. The internal processor clock is two-phase and the machine states are executed at a rate of 6 MHz. The shortest instructions require two states (333 ns). The CPU contains a one-byte instruction prefetch. This allows a subsequent instruction to be fetched during the execution of an instruction that does not reference memory.

Memory Map

The μPD78224 family has 1M bytes of address space. This address space is partitioned into 64K bytes of program memory starting at address 00000H. (See figure 1). The remainder of the 1M bytes can be accessed as data memory space.

Figure 1. Memory Map



External memory is supported by I/O port 4, an 8-bit multiplexed address/data bus. The memory mapping register controls the size of external memory as well as the number of added wait states. The upper address byte is derived from port 5, and the extended address nibble is derived from port 6.

The μPD78224 has on-chip mask ROM occupying the space from 00000H to 03FFFH. When the ROM is used and no other program or data space is required, ports 4, 5, and 6 are available as additional I/O ports.

General-Purpose Registers

The general-purpose registers are mapped into specific addresses in data memory. They are made up of four banks, each bank consisting of eight 8-bit or four 16-bit registers. The register bank used is specified by a CPU instruction. This can be checked by reading RBS0 and RBS1 in the program status word (PSW). The general-purpose register configuration is shown in figure 2.

Special Registers

There are three different special registers. The first is a 16-bit binary counter that holds the next program address to be executed and is named the program counter. The stack pointer is the second special 16-bit register. The stack pointer holds the address of the stack area (a last in, first out system). The third special register is an 8-bit program status word. This register contains various flags that are set or preset depending on the results of instruction execution. The program status word format is as follows:

7							0
IE	Z	RBS1	AC	RBS0	0	ISP	CY

CY	Carry flag
ISP	Interrupt priority status flag
RBS0, RBS1	Register bank selection flags
AC	Auxiliary carry flag
Z	Zero flag
IE	Interrupt request enable flag

Special Function Registers

These registers are assigned to special functions such as the mode and control registers for on-chip peripheral hardware. They are mapped into the 256-byte memory space from 0FF00H to 0FFFFH. Table 1 is a list of special function registers.

Figure 2. Register Mapping

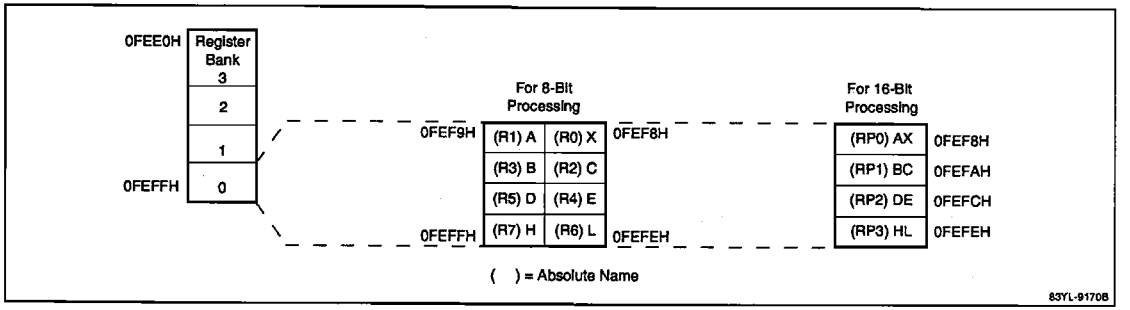


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Table 1. Special Function Registers

Address	Register (SFR)	Symbol	R/W	Access Units (Bits) 1	8	16	State After Reset
0FF00H	Port 0	P0	R/W	x	x	—	Undefined
0FF01H	Port 1	P1	R/W	x	x	—	Undefined
0FF02H	Port 2	P2	R	x	x	—	Undefined
0FF03H	Port 3	P3	R/W	x	x	—	Undefined
0FF04H	Port 4	P4	R/W	x	x	—	Undefined
0FF05H	Port 5	P5	R/W	x	x	—	Undefined
0FF06H	Port 6	P6	R/W	x	x	—	x0H
0FF07H	Port 7	P7	R/W	x	x	—	Undefined
0FF0AH	Port 0 buffer register (low)	P0L	R/W	x	x	—	Undefined
0FF0BH	Port 0 buffer register (high)	P0H	R/W	x	x	—	Undefined
0FF0CH	Real-time output port control register	RTPC	R/W	x	x	—	00H
0FF10H-FF11H	16-bit compare register 0 (16-bit timer/counter)	CR00	R/W	—	—	x	Undefined
0FF12H-FF13H	16-bit compare register 1 (16-bit timer/counter)	CR01	R/W	—	—	x	Undefined
0FF14H	8-bit compare register (8-bit timer/counter 1)	CR10	R/W	—	x	—	Undefined
0FF15H	8-bit compare register (8-bit timer/counter 2)	CR20	R/W	—	x	—	Undefined
0FF16H	8-bit compare register (8-bit timer/counter 2)	CR21	R/W	—	x	—	Undefined
0FF17H	BRG 8-bit compare register	CR30	R/W	—	x	—	Undefined
0FF18H-FF19H	16-bit capture register (16-bit timer/counter)	CR02	R	—	—	x	Undefined
0FF1AH	8-bit capture register (8-bit timer/counter 2)	CR22	R	—	x	—	Undefined
0FF1CH	8-bit capture/compare register (8-bit timer/counter 1)	CR11	R/W	—	x	—	Undefined
0FF20H	Port 0 mode register	PM0	W	—	x	—	FFH
0FF21H	Port 1 mode register	PM1	W	—	x	—	FFH
0FF23H	Port 3 mode register	PM3	W	—	x	—	FFH
0FF25H	Port 5 mode register	PM5	W	—	x	—	FFH
0FF26H	Port 6 mode register	PM6	R/W	—	x	—	FFH
0FF27H	Port 7 mode register	PM7	W	—	x	—	7FH
0FF30H	Capture/compare control register 0	CRC0	W	—	x	—	10H
0FF31H	Timer output control register	TOC	W	—	x	—	00H
0FF32H	Capture/compare control register 1	CRC1	W	—	x	—	00H
0FF34H	Capture/compare control register 2	CRC2	W	—	x	—	00H
0FF43H	Port 3 mode control register	PMC3	R/W	x	x	—	00H
0FF50H-FF51H	16-bit timer register 0	TM0	R	—	—	x	0000H
0FF52H	8-bit timer register 1: CH -1	TM1	R	—	x	—	00H
0FF54H	8-bit timer register 2: CH-2	TM2	R	—	x	—	00H
0FF56H	BRG 8-bit timer register	TM3	R	—	x	—	00H
0FF5CH	Prescaler mode register 0	PRM0	W	—	x	—	00H
0FF5DH	Timer control register 0	TMC0	R/W	—	x	—	00H

Table 1. Special Function Registers (cont)

Address	Register (SFR)	Symbol		R/W	Access Units (Bits) 1	8	16	State After Reset
0FF5EH	Prescaler mode register 1	PRM1		W	—	x	—	00H
0FF5FH	Timer control register 1	TMC1		R/W	—	x	—	00H
0FF6EH	Port T mode register	PMT		R/W	x	x	—	00H
0FF6FH	Port T	PT		R	x	x	—	Undefined
0FF80H	Clocked serial interface mode register	CSIM		R/W	x	x	—	00H
0FF82H	Serial bus interface control register	SBIC		R/W	x	x	—	00H
0FF86H	Serial shift register	SIO		R/W	—	x	—	Undefined
0FF88H	Asynchronous serial interface mode register	ASIM		R/W	x	x	—	80H
0FF8AH	Asynchronous serial interface status register	ASIS		R	x	x	—	00H
0FF8CH	Serial receive buffer: UART	RxB		R	—	x	—	Undefined
0FF8EH	Serial transmit shift register: UART	TxS		W	—	x	—	Undefined
0FFC0H	Standby control register	STBC		R/W	—	x	—	0000x000B
0FFC4H	Memory expansion mode register	MM		R/W	x	x	—	20H
0FFC5H	Programmable wait control register	PW		R/W	x	x	—	80H
0FFC6H	Refresh mode register	RFM		R/W	x	x	—	00H
0FFE0H	Interrupt request flag register L	IF0L	IF0	R/W	x	x	x	Undefined
0FFE1H	Interrupt request flag register H	IF0H		R/W	x	x	—	Undefined
0FFE4H	Interrupt mask flag register L	MK0L	MK0	R/W	x	x	x	FFFFH
0FFE5H	Interrupt mask flag register H	MK0H		R/W	x	x	—	FFFFH
0FFE8H	Priority specification flag register L	PR0L	PR0	R/W	x	x	x	FFFFH
0FFE9H	Priority specification flag register H	PR0H		R/W	x	x	—	FFFFH
0FFECH	Interrupt service mode speification flag register L	ISM0L	ISM0	R/W	x	x	x	0000H
0FFEDH	Interrupt service mode specification flag register H	ISM0H		R/W	x	x	—	0000H
0FFF4H	External interrupt mode register 0	INTM0		R/W	x	x	—	00H
0FFF5H	External interrupt mode register 1	INTM1		R/W	x	x	—	00H
0FFF8H	Interrupt status register	IST		R/W	x	x	—	00H

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Input/Output Ports

Functions of ports P0 - P7 and port PT are explained below. All ports are 8 bits wide except P7, which is 7 bits wide.

Port	Function
P0	8-bit output port or two 4-bit real time output ports
P1	Bit programmable for input or output; large current capacity
P2	Input
P3	Bit programmable for input or output
P4	Input or output
P5	Output
$P6_0$ - $P6_3$	Output
$P6_4$ - $P6_7$	Bit programmable for input or output
P7	Bit programmable for input or output
PT	Inputs to eight voltage comparators

Real-time Output Port

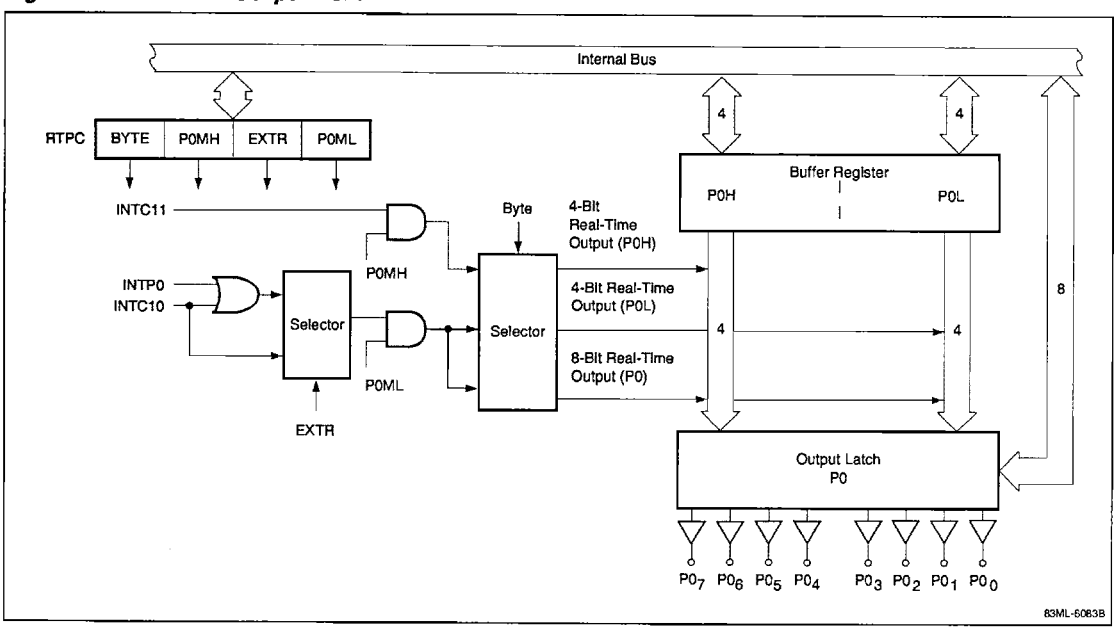
The real-time output port (figure 3) shares pins with port 0. The high and low nibbles may be treated separately or together. In the real-time output function, data stored beforehand in the buffer register is transferred to the output latch simultaneously with the generation of either a timer interrupt or external interrupt. Using the real-time output function in conjunction with the macro service function enables port 0 to output preprogrammed patterns at preprogrammed variable time intervals.

Port T

As shown in figure 4, the analog input voltage on each line of port T is compared with a programmable threshold voltage. The comparator output is 1 if the input voltage is higher than the threshold, or 0 if it is lower.

Four bits from the PTM regster are decoded to set the threshold voltage at one of 15 steps: V_{DD} x 1/16 through V_{DD} x 15/16. Each comparator operates continously as follows.

Figure 3. Real-Time Output Port



(1) Threshold voltage is set by writing the PTM register.

(2) As each comparison is completed, the result is latched in port T and the next comparison begins.

(3) Unless the PTM regiser is written, the threshold voltage is not changed.

Two bits from the PTM register specify the connection of pullup resistors in 4-bit units. When PTM is set to 00H, the resistor ladder is released and threshold voltage is not supplied to the comparators. This can be done in the standby mode to eliminate unnecessary current drain.

Serial Interface

The μPD78224 family has two independent serial interfaces.

- Asynchronous serial interface (UART) (figure 5)
- Clock-synchronized serial interface (figure 6)

A universal asynchronous receiver transmitter (UART) is used as an asynchronous serial interface. This interface transfers one byte of data following a start bit. The μPD78224 contains a baud rate generator. This allows data to be transferred over a wide range of transfer rates.

The clock-synchronized serial interface has two different modes of operation:

- Three-line serial I/O mode.
  In this mode, data 8 bits long is transferred along three lines: a serial clock (SCK) line and two serial bus lines lines (SO and SI). This mode is convenient when a μPD78224 device is connected to peripheral I/Os and display controllers that have the conventional clock-synchronized serial interface.
- Serial bus interface mode (SBI)
  In this mode, the μPD78224 family can communicate data with several devices using the serial clock (SCK) and the serial data bus (SBO) lines. This mode conforms to NEC's serial bus format. In SBI mode, addresses that select a device to communicate with, commands that direct the device, and actual data are output to the serial data bus. A handshake line, which was required for connecting several devices in the conventional clock-synchronized serial interface, is not needed.

Figure 4. Comparator Port T

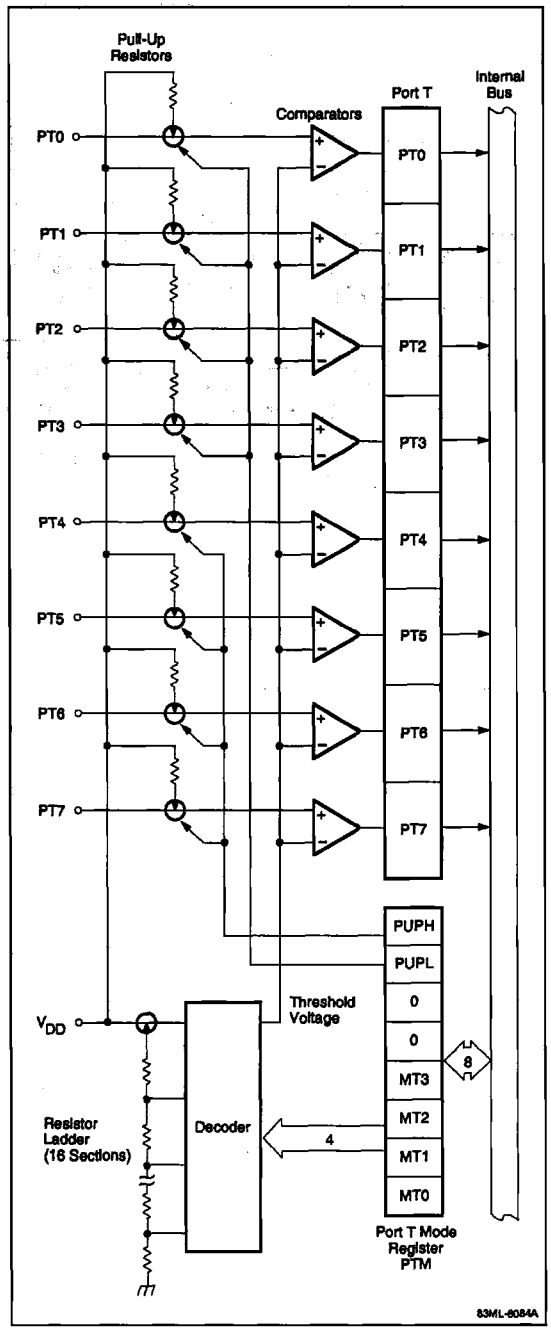


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Figure 5. Asynchronous Serial Interface

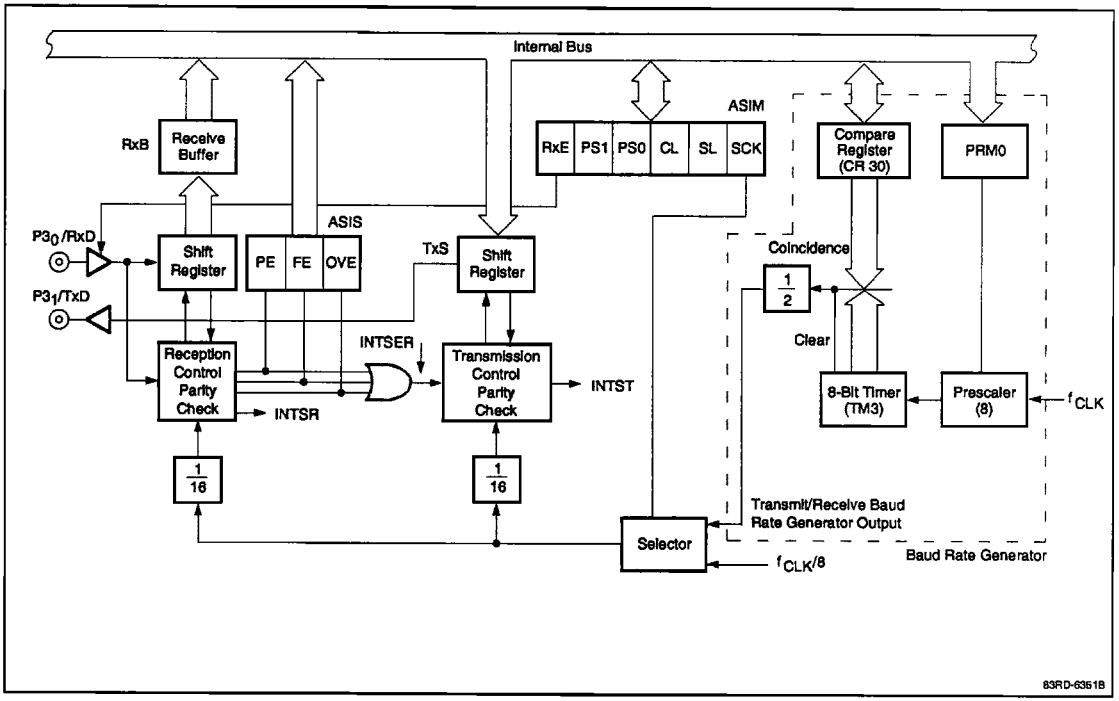
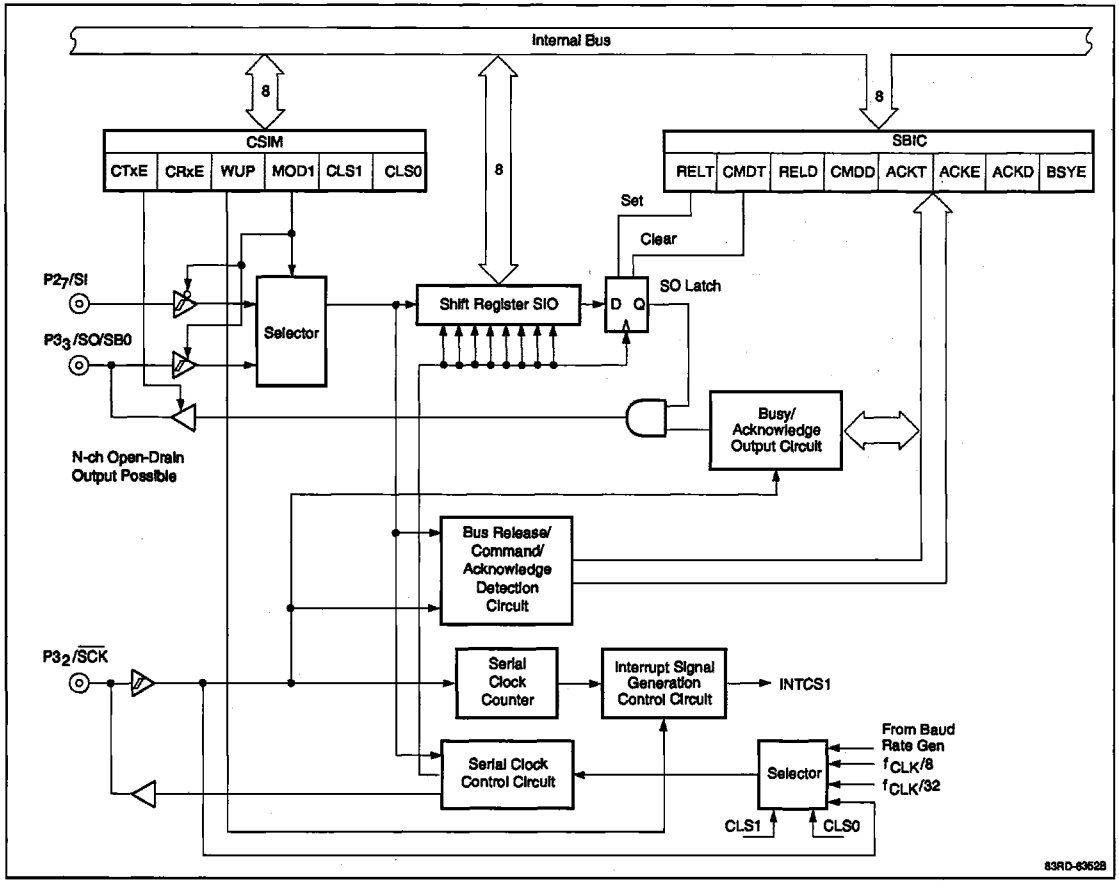


Figure 6. Clock-Synchronized Serial Interface



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Timer/Counters

The μPD78224 family has three timer/counters: one 16-bit and two 8-bit. The 16-bit timer/counter (figure 7) has the basic functionality of an interval timer, a programmable square wave output, and a pulse-width measurer. These functions can provide a digital delayed one-shot output, a pulse-width modulated output, and a cycle measurer.

The two 8-bit timer/counters can provide the basic functions of an interval timer and a pulse-width measurer. Timer/counter 1 can also be used as a timer for output trigger generation for the real-time output port. Timer/counter 2 can also provide an external event counter, a one-shot timer, a programmable square-wave output, a pulse-width modulated output, and a cycle measurer. See figures 8 and 9.

Figure 7. 16-Bit Timer/Counter

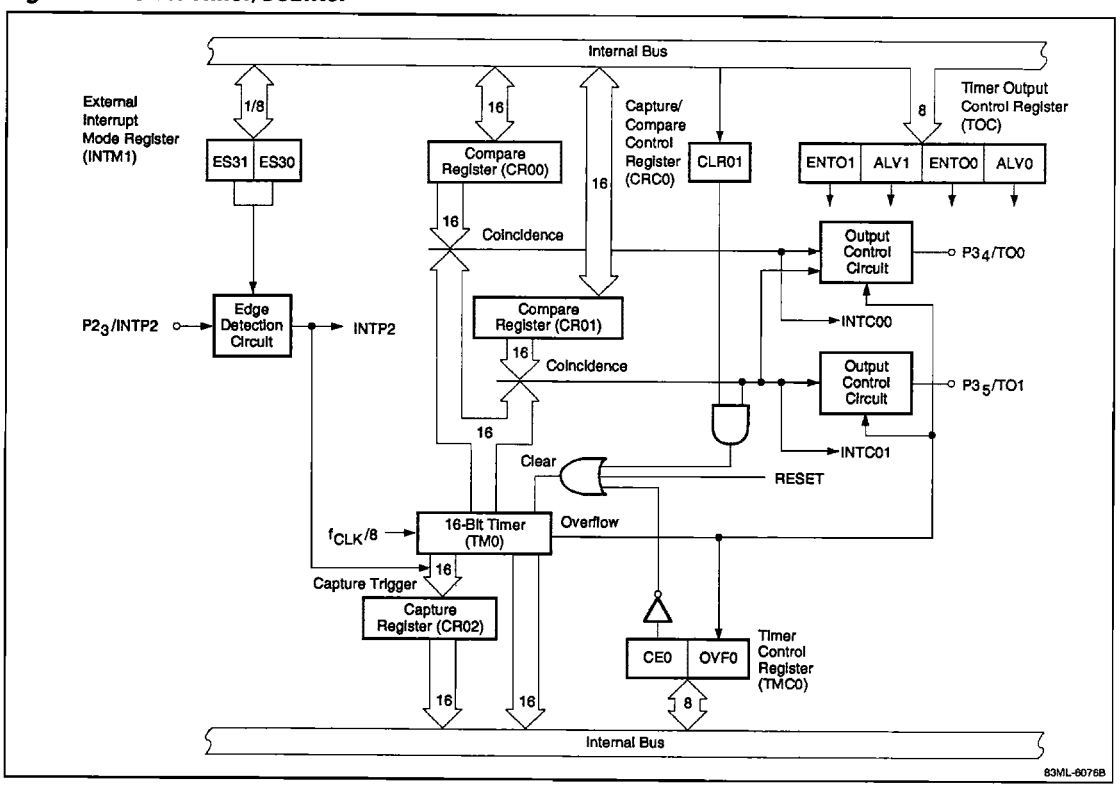


Figure 8. 8-Bit Timer/Counter 1

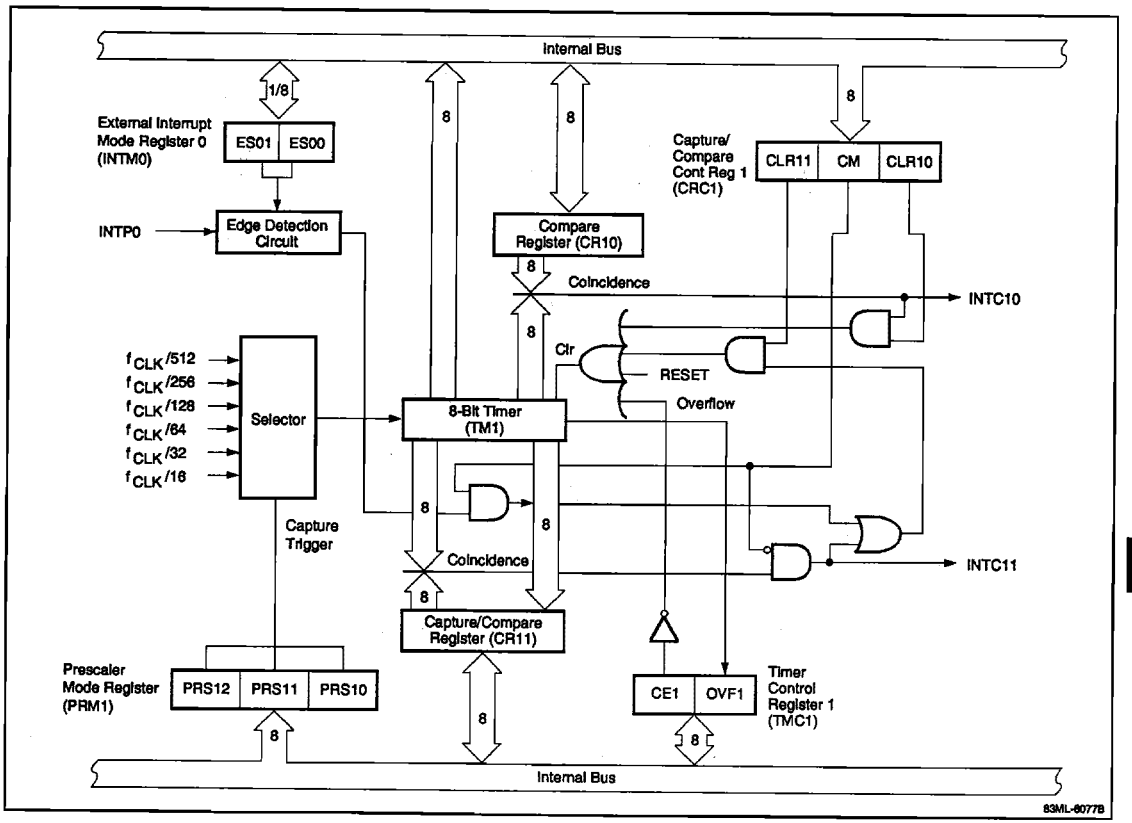
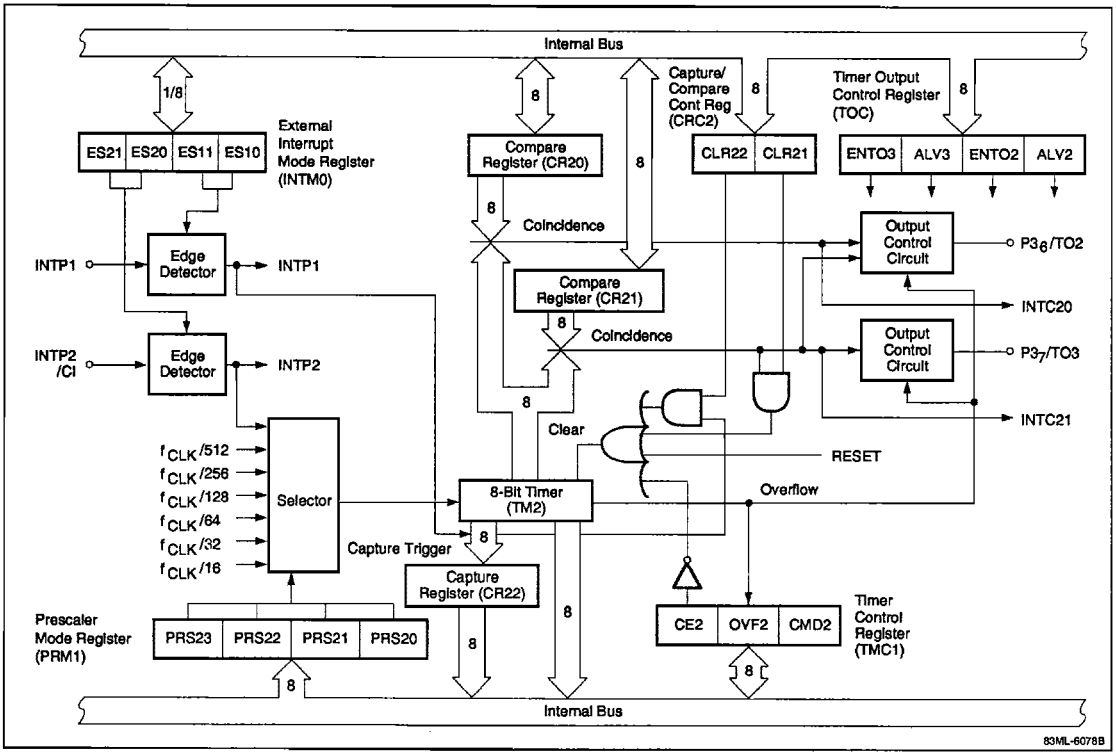


Figure 9. 8-Bit Timer/Counter 2



Interrupts

There are 18 interrupt request sources; each source is allocated a location in the vector table. (See table 2). There is one software interrupt request and one of the remaining 17 interrupts is nonmaskable. The software interrupt and the nonmaskable interrupt are unconditionally received even in the DI state. These two interrupts possess the maximum priority. The maskable interrupt requests are subject to mask control by the setting of the interrupt mask flag.

There are default priorities associated with each maskable interrupt and these can be assigned to either of two programmable priority levels. Interrupts may be serviced by the vectored interrupt method where a branch to a desired service program is executed. Interrupts may also be handled by the macro service function where a preassigned process is performed without program intervention.

Table 2. Interrupt Sources and Vector Addresses

Interrupt Request Type	Default Priority	Interrupt Request Source	Macro Service Handling	Vector Table Address
Software	None	BRK instruction execution	—	003EH
Nonmaskable	None	NMI (pin input edge detection)	—	0002H
Maskable	0	INTP0 (pin input edge detection)	—	0006H
	1	INTP1 (pin input edge detection)	—	0008H
	2	INTP2 (pin input edge detection)	—	000AH
	3	INTP3 (pin input edge detection)	—	000CH
	4	INTC00 (TM0-CR00 coincidence signal generation)	—	0014H
	5	INTC01 (TM0-CR01 coincidence signal generation)	—	0016H
	6	INTC10 (TM1-CR10 coincidence signal generation)	Yes	0018H
	7	INTC11 (TM1-CR11 coincidence signal generation)	Yes	001AH
	8	INTC21 (TM2-CR21 coincidence signal generation)	—	001CH
	9	INTP4 (pin input edge detection)	Yes	000EH
	10	INTP5 (pin input edge detection)	—	0010H
	11	INTP6 (pin input edge detection)	—	0012H
	12	INTSER (generation of asynchronous serial interface receive error)	—	0020H
	13	INTSR (end of asynchronous serial interface reception)	Yes	0022H
	14	INTST (end of asynchronous serial interface transmission)	Yes	0024H
	15	INTCSI (end of clocked serial interface transfer)	Yes	0026H

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Macro Service

When macro service function can be programmed to transfer data from a special function register to memory or from memory to a special function register. Transfer events are triggered by interrupt requests and take place without software intervention. There are six interrupt requests where macro servicing can be executed. The macro service function is controlled by the macro service mode register and the macro service channel pointer. The macro service mode register assigns the macro servicing mode and the macro service channel pointer indicates the address of the memory location pointers. The location of each register and its corresponding interrupt is shown in figure 10.

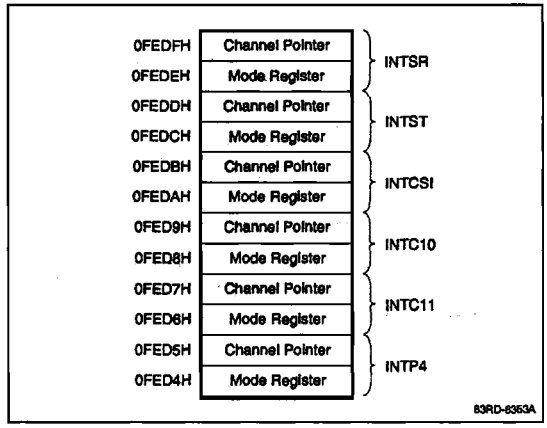
Refresh

The refresh signal is used with a pseudostatic RAM. The refresh cycle can be set to one of four intervals ranging from 2.6 to 21.3 μs. The refresh is timed to follow a read or write operation to avoid interference.

Standby Modes

HALT and STOP functions reduce system power consumption. In HALT mode, the CPU stops and the system clock continues to run. A release of the HALT mode is initiated by an unmasked interrupt request, an NMI, or a $\overline{\text{RESET}}$ input. In the STOP mode, the CPU and system clock are both stopped, reducing the power consumption even further. The STOP mode is released by an NMI input or a $\overline{\text{RESET}}$ input.

Figure 10. Macro Service Control Word Map



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Operating voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.5 V
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Low-level output current, I_{OL}	
per pin	30 mA (peak), 15 mA (mean)
total, all output pins	150 mA (peak), 100 mA (mean)
High-level output current, I_{OH}	
per pin	−2 mA
total, all output pins	−50 mA
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Operating Conditions

Oscillation Frequency	T_A	V_{DD}
f_{XX} = 4 to 12 MHz	−40 to +85°C	+5 V ±5%
	−10 to +70°C	+5 V ±10%

Capacitance

T_A = +25°C; V_{DD} = V_{SS} = 0 V

Item	Symbol	Max	Unit	Conditions
Input capacitance	C_I	20	pF	f = 1 MHz; pins not used for measurement are at 0 V
Output capacitance	C_O	20	pF	
Input/output capacitance	C_{IO}	20	pF	

DC Characteristics

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V

Item	Symbol	Min	Typ	Max	Unit	Conditions
Low-level input voltage	V_{IL}	0		0.8	V	Except PT pins
High-level input voltage	V_{IH1}	2.2		V_{DD}	V	Except PT pins and pins in Note 1
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Pins in Note 1
Low-level output voltage	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
	V_{OL2}			1.0	V	I_{OL} = 8.0 mA (Port PI pins)
High-level output voltage	V_{OH1}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{DD} − 0.5			V	I_{OH} = −100 μA
Input leakage current	I_{LI}			±10	μA	V_I = 0 to V_{DD}
Output leakage current	I_{LO}			±10	μA	V_O = 0 to V_{DD}
Pullup current	I_{IPT}		−150	−400	μA	V_I = 0 V; PT pins
V_{DD} power supply current	I_{DD1}		16	40	mA	Operating mode, f_{XX} = 12 MHz
	I_{DD2}		7	20	mA	HALT mode, f_{XX} = 12 MHz
Data retention voltage	V_{DDDR}	2.5		5.5	V	STOP mode
Data retention current	I_{DDDR}		2	20	μA	STOP mode; V_{DDDR} = 2.5 V
			5	50	μA	STOP mode; V_{DDDR} = 5 V ±10%

Notes:

(1) X1, X2, $\overline{\text{RESET}}$, $P2_0$/NMI, $P2_1$/INTP0, $P2_2$/INTP1, $P2_3$/$\overline{\text{INTP2}}$/CI, $P2_4$/INTP3, $P2_5$/$\overline{\text{INTP4}}$, $P2_6$/INTP5, $P2_7$/INTP6/SI, $P3_2$/SCK, $P3_3$/SO/SB0, and EA pins.

Read/Write Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V; f_{XX} = 12 MHz; C_L = 100 pF

Item	Symbol	Min	Max	Unit	Conditions
X1 input clock cycle time	t_{CYX}	82	250	ns	
Address setup time to ASTB ↓	t_{SAST}	52		ns	
Address hold time from ASTB ↓ (Note 2)	t_{HSTA}	25		ns	R_L = 5 kΩ, C_L = 50 pF
Address to $\overline{RD}$ ↓ delay time	t_{DAR}	129		ns	
Address float time from $\overline{RD}$ ↓	t_{FAR}	11		ns	
Address to data input time	t_{DAID}		228	ns	
ASTB ↓ to data input time	t_{DSTID}		181	ns	
$\overline{RD}$ ↓ to data input time	t_{DRID}		99	ns	
ASTB ↓ to $\overline{RD}$ ↓ delay time	t_{DSTR}	52		ns	
Data hold time from $\overline{RD}$ ↑	t_{HRID}	0		ns	
$\overline{RD}$ ↑ to address active time	t_{DRA}	124		ns	
$\overline{RD}$ ↑ to ASTB ↑ delay time	t_{DRST}	124		ns	
$\overline{RD}$ low-level width	t_{WRL}	124		ns	No wait states
ASTB high-level width	t_{WSTH}	52		ns	
Address to $\overline{WR}$ ↓ delay time	t_{DAW}	129		ns	
$\overline{ASTB}$ ↓ to data output time	t_{DSTOD}		142	ns	
$\overline{WR}$ ↓ to data output time	t_{DWOD}		60	ns	
ASTB ↓ to $\overline{WR}$ ↓ delay time	t_{DSTW1}	52		ns	
	t_{DSTW2}	129		ns	Refresh mode
Data setup time to $\overline{WR}$ ↑	t_{SODWR}	146		ns	
Data setup time to $\overline{WR}$ ↓ (Note 1)	t_{SODWF}	22		ns	Refresh mode
Data hold time from $\overline{WR}$ ↑ (Note 2)	t_{HWOD}	20		ns	
$\overline{WR}$ ↑ to ASTB ↑ delay time	t_{DWST}	42		ns	
$\overline{WR}$ low-level width	t_{WWL1}	196		ns	
	t_{WWL2}	114		ns	Refresh mode
Address to $\overline{WAIT}$ ↓ input time	t_{DAWT}		146	ns	
ASTB ↓ to $\overline{WAIT}$ ↓ input time	t_{DSTWT}		84	ns	
$\overline{WAIT}$ hold time from X1 ↓	t_{HWTX}	0		ns	
$\overline{WAIT}$ setup time to X1 ↑	t_{SWTX}*	0		ns	

Notes:

(1) When accessing a pseudostatic RAM (μPD4168, etc.) that clocks in data at the falling edge of $\overline{WR}$, use t_{SODWF} instead of t_{SODWR} as the data setup time.

(2) The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions: C_L = 100 pF and R_L = 2 kΩ.

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Serial Port Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V; f_{XX} = 12 MHz; C_L = 100 pF

Item	Symbol	Min	Max	Unit	Conditions
Serial clock cycle time	t_{CYSK}	1.0		μs	External clock input
		1.3		μs	Internal clock/16 output
		5.3		μs	Internal clock/64 output
Serial clock low-level width	t_{WSKL}	420		ns	External clock input
		556		ns	Internal clock/16 output
		2.5		μs	Internal clock/64 output
Serial clock high-level width	t_{WSKH}	420		ns	External clock input
		556		ns	Internal clock/16 output
		2.5		μs	Internal clock/64 output
SI, SB0 setup time to $\overline{SCK}$ ↑	t_{SSSK}	150		ns	
SI, SB0 hold time from $\overline{SCK}$ ↓	t_{HSSK}	400		ns	
SO/SB0 output delay time from $\overline{SCK}$ ↓	t_{DSBSK1}	0	300	ns	CMOS push-pull output (3-line serial I/O mode)
	t_{DSBSK2}	0	800	ns	Open-drain output (SBI mode), R_L = 1 kΩ
SB0 high, hold time from $\overline{SCK}$ ↑	t_{HSBSK}	4		t_{CYX}	SBI mode
SB0 low, setup time to $\overline{SCK}$ ↓	t_{SSBSK}	4		t_{CYX}	SBI mode
SB0 low-level width	t_{WSBL}	4		t_{CYX}	
SB0 high-level width	t_{WSBH}	4		t_{CYX}	
RxD setup time to $\overline{SCK}$ ↑	t_{SRXSK}	80		ns	
RxD hold time after $\overline{SCK}$ ↑	t_{HSKRX}	80		ns	
$\overline{SCK}$ ↓ to TxD delay time	t_{DSKTX}		210	ns	

Comparator Port Operation

Item	Symbol	Min	Max	Unit	Conditions
Comparison accuracy	V_{ACOMP}		100	mV	—
			100	mV	μPD78P224
Comparison time	t_{COMP}	128	256	t_{CYX}	
Sampling time	t_{SAMP}	62		t_{CYX}	
PT input voltage	V_{IPT}	0	V_{DD}	V	

Interrupt Timing Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V

Item	Symbol	Min	Max	Unit	Conditions
NMI low-level width	t_{WNIL}	10		μs	
NMI high-level width	t_{WNIH}	10		μs	
INTP0-INTP6 low-level width	t_{WITL}	24		t_{CYX}	
INTP0-INTP6 high-level width	t_{WITH}	24		t_{CYX}	
$\overline{RESET}$ low-level width	t_{WRSL}	10		μs	
$\overline{RESET}$ high-level width	t_{WRSH}	10		μs	

Data Retention Characteristics

Item	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.5		5.5	V	STOP mode
Data retention current	I_{DDDR}		2	20	μA	V_{DDDR} = 2.5 V
			5	50	μA	V_{DDDR} = 5 V ±10%
V_{DD} rise time	t_{RVD}	200			μs	
V_{DD} fall time	t_{FVD}	200			μs	

Data Retention Characteristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Conditions
V_{DD} retention time (from STOP mode setting)	t_{HVD}	0			ms	
STOP release signal input time	t_{DREL}	0			ms	
Oscillation stabilization wait time	t_{WAIT}	30			ms	Crystal resonator
		5			ms	Ceramic resonator
Low-level input voltage	V_{IL}	0		0.1 V_{DDDR}	V	Specified pins (Note)
High-level input voltage	V_{IH}	0.9 V_{DDDR}		V_{DDDR}	V	Specified pins (Note)

Note: $\overline{RESET}$, $P2_0$/NMI, $P2_1$/INTP0, $P2_2$/INTP1, $P2_3$/INTP2/CI, $P2_4$/INTP3, $P2_5$/INTP4, $P2_6$/INTP5, $P2_7$/INTP6/SI, $P3_2/\overline{SCK}$, $P3_3$/SO/SB0, and $\overline{EA}$ pins.

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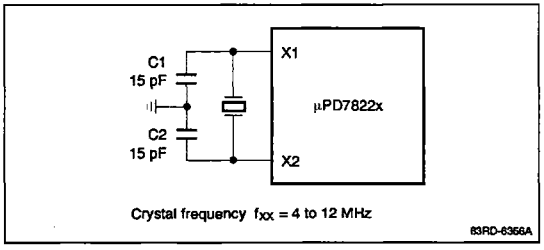
Timing Dependent on t_{CYX}

Item	Symbol	Calculation Formula (1, 2)	Min/Max	12 MHz	Unit
X1 input clock cycle time	t_{CYX}		Min	82	ns
Address setup time to ASTB ↓	t_{SAST}	$t_{CYX} - 30$	Min	52	ns
Address to $\overline{RD}$ ↓ delay time	t_{DAR}	$2t_{CYX} - 35$	Min	129	ns
Address float time from $\overline{RD}$ ↓	t_{FAR}	$t_{CYX}/2 - 30$	Min	11	ns
Address to data input time	t_{DAID}	$(4+2n)t_{CYX} - 100$	Max	228	ns
ASTB ↓ to data input time	t_{DSTID}	$(3+2n)t_{CYX} - 65$	Max	181	ns
$\overline{RD}$ ↓ to data input time	t_{DRID}	$(2+2n)t_{CYX} - 65$	Max	99	ns
ASTB ↓ to $\overline{RD}$ ↓ delay time	t_{DSTR}	$t_{CYX} - 30$	Min	52	ns
$\overline{RD}$ ↑ to address active time	t_{DRA}	$2t_{CYX} - 40$	Min	124	ns
$\overline{RD}$ ↑ to ASTB ↑ delay time	t_{DRST}	$2t_{CYX} - 40$	Min	124	ns
$\overline{RD}$ low-level width	t_{WRL}	$(2+2n)t_{CYX} - 40$	Min	124	ns
ASTB high-level width	t_{WSTH}	$t_{CYX} - 30$	Min	52	ns
Address to $\overline{WR}$ ↓ delay time	t_{DAW}	$2t_{CYX} - 35$	Min	129	ns
ASTB ↓ to data output time	t_{DSTOD}	$t_{CYX} + 60$	Max	142	ns
ASTB ↓ to $\overline{WR}$ ↓ delay time	t_{DSTW1}	$t_{CYX} - 30$	Min	52	ns
	t_{DSTW2}	$2t_{CYX} - 35$ (refresh mode)	Min	129	ns
Data setup time to $\overline{WR}$ ↑	t_{SODWR}	$(3+2n)t_{CYX} - 100$	Min	146	ns
Data setup time to $\overline{WR}$ ↓	t_{SODWF}	$t_{CYX} - 60$ (refresh mode)	Min	22	ns
$\overline{WR}$ ↑ to ASTB ↑ delay time	t_{DWST}	$t_{CYX} - 40$	Min	42	ns
$\overline{WR}$ low-level width	t_{WWL1}	$(3+2n)t_{CYX} - 50$	Min	196	ns
	t_{WWL2}	$(2+2n)t_{CYX} - 50$ (refresh mode)	Min	114	ns
Address to $\overline{WAIT}$ ↓ input time	t_{DAWT}	$3t_{CYX} - 100$	Max	146	ns
ASTB ↓ to $\overline{WAIT}$ ↓ input time	t_{DSTWT}	$2t_{CYX} - 80$	Max	84	ns

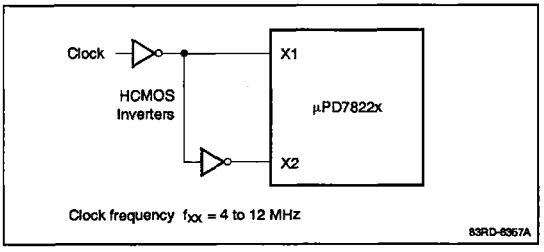
Note:

(1) n indicates the number of internal wait states.

Recommended Oscillator Circuit



Recommended External Clock Circuit



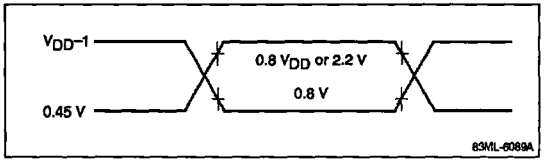
External Clock Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V

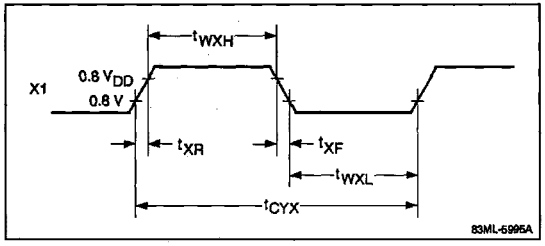
Item	Symbol	Min	Max	Unit	Conditions
X1 input low-level width	t_{WXL}	30	130	ns	
X1 input high-level width	t_{WXH}	30	130	ns	
X1 input rise time	t_{XR}	0	30	ns	
X1 input fall time	t_{XF}	0	30	ns	
X1 input clock cycle time	t_{CYX}	82	250	ns	

Timing Waveforms

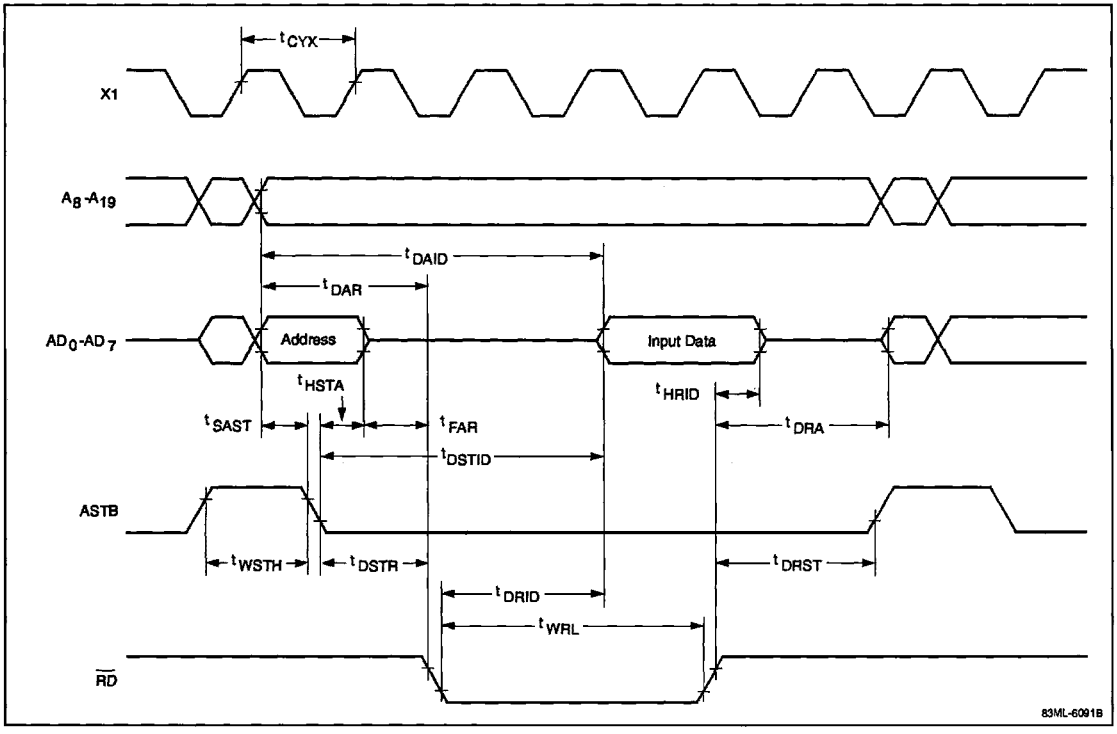
Voltage Thresholds for Timing Measurements



External Clock



Read Operation



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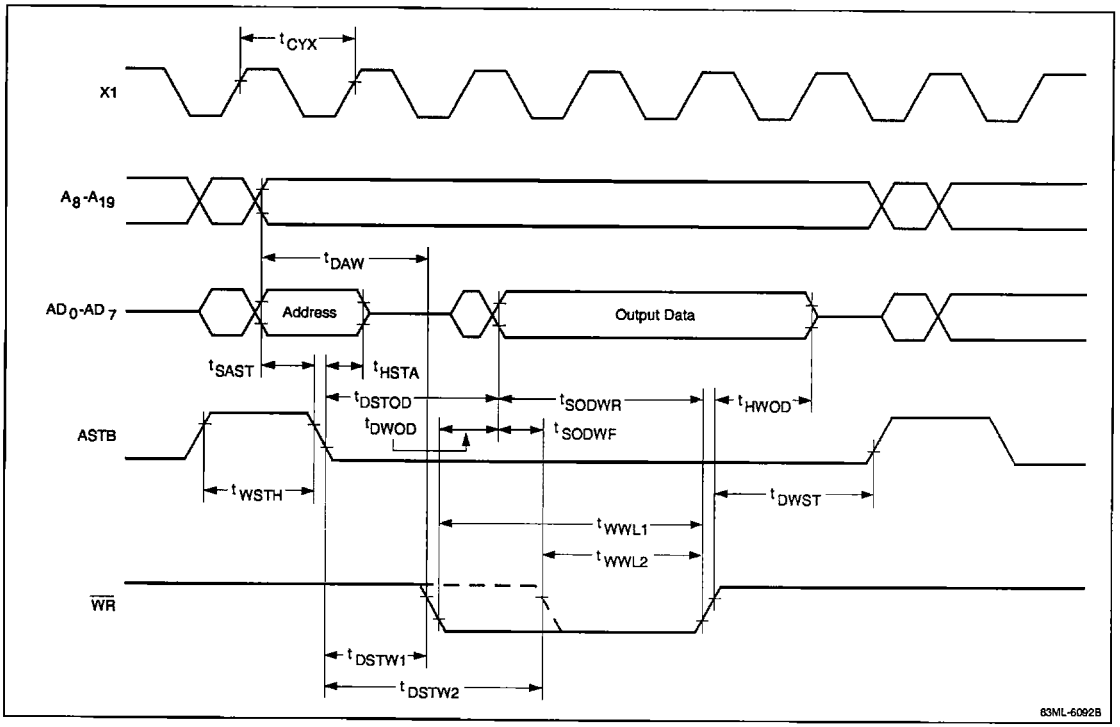
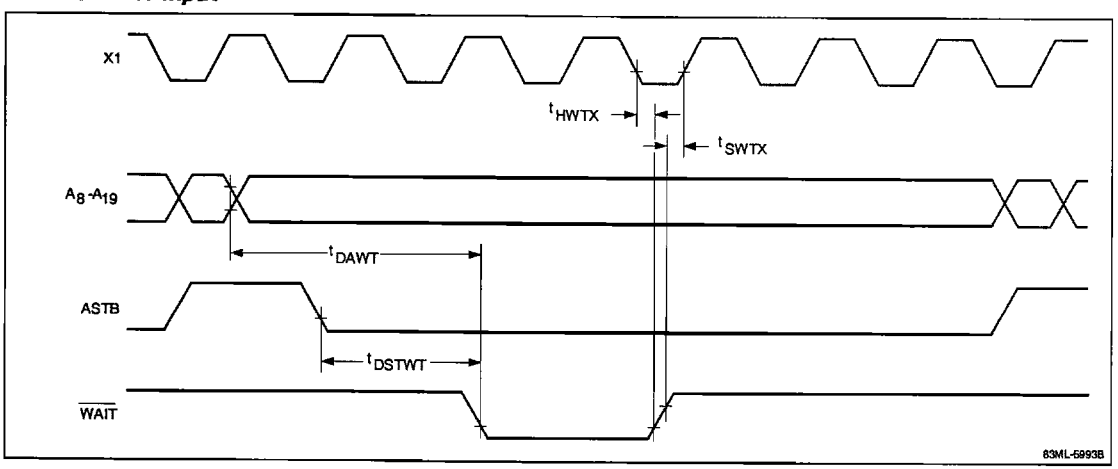
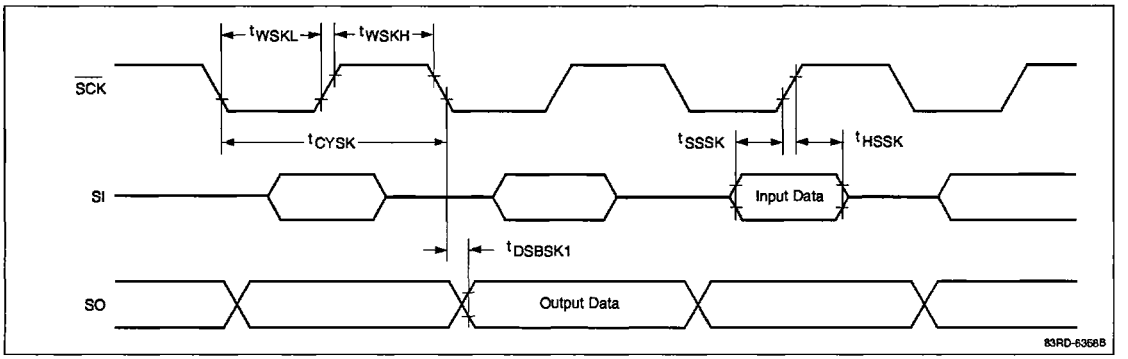
Write Operation



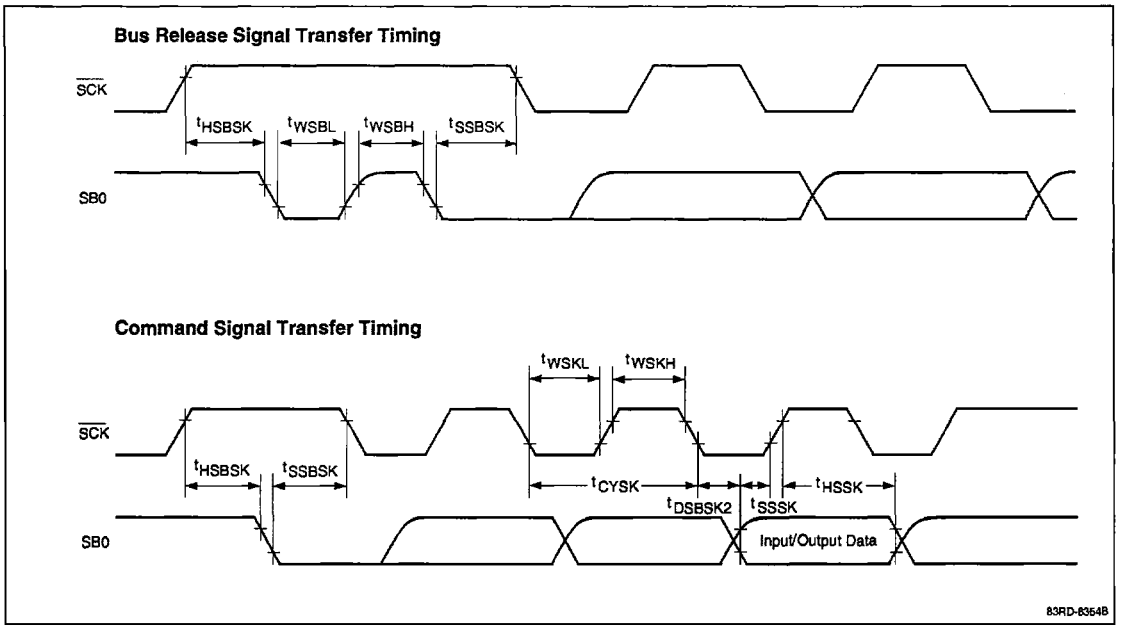
External WAIT Input



Clock-Synchronized Serial Interface; Three-Line I/O Mode



Clock-Synchronized Serial Interface; SBI Mode



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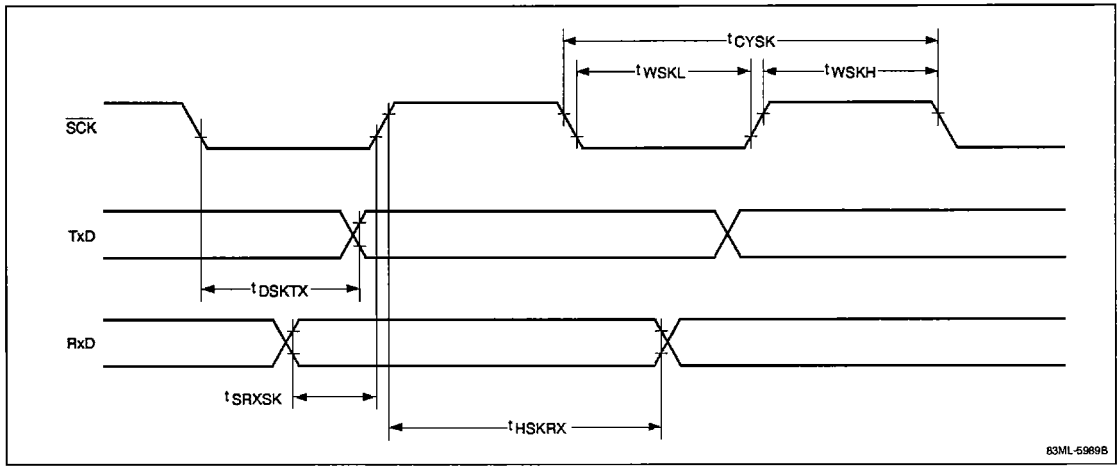
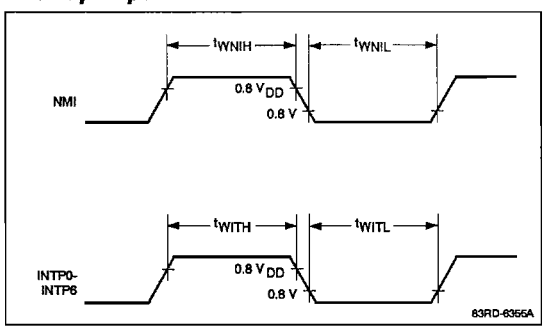
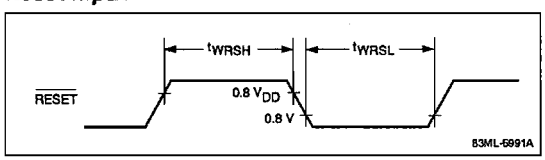
Asynchronous Mode



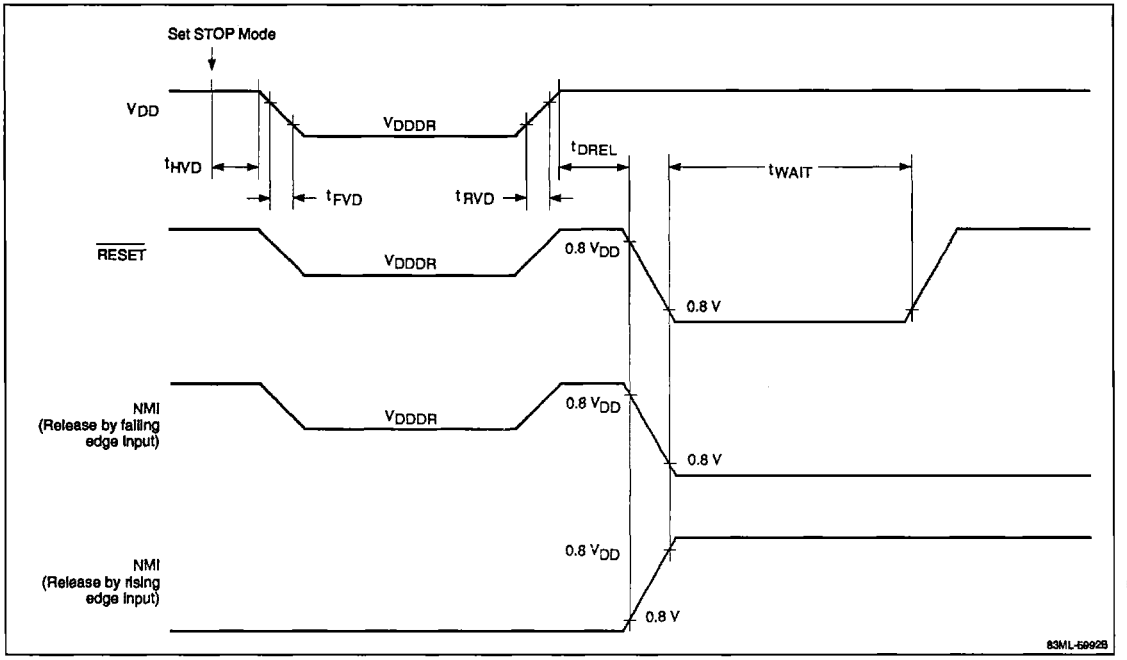
Interrupt Input



Reset Input



Data Retention Characteristics



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μPD78P224 PROGRAMMING

In the μPD78P224, the mask ROM of μPD78224 is replaced by a one-time programmable ROM (OTP ROM). The ROM is 16,384 x 8 bits and can be programmed using a general-purpose PROM writer with a μPD27C256A programming mode.

The PA-78P224GJ/L are the socket adaptors used for configuring the μPD78P224 to fit a standard PROM socket.

Refer to tables 3 through 6 and the PROM timing diagrams for special information applicable to PROM programming.

Table 3. Pin Functions During PROM Programming

Pin	Pin*	Function
$P0_0$ - $P0_7$	A_0 - A_7	Input pins for PROM write/verify operations
$P5_0/A_8$	A_8	Input pin for PROM write/verify operations
$P2_1$/INTP0	A_9	Input pin for PROM write/verify operations
$P5_2/A_{10}$ - $P5_6/A_{14}$	A_{10} - A_{14}	Input pins for PROM write/verify operations
$P4_0/AD_0$ - $P4_7/AD_7$	D_0 - D_7	Data pins for PROM operations
$P6_5/\overline{WR}$	$\overline{CE}$	Strobes data into the PROM
$P6_4/\overline{RD}$	$\overline{OE}$	Enables a data read from the PROM
$P2_0$/NMI	NMI	PROM programming mode is entered by applying a high voltage to this pin
$\overline{RESET}$	$\overline{RESET}$	PROM programming mode requires applying a low voltage to this pin
$\overline{EA}$	V_{PP}	High voltage applied to this pin for program write/verify
V_{DD}	V_{DD}	Positive power supply pin
V_{SS}	V_{SS}	Ground

* Pin name in PROM programming mode.

Table 4. Summary of Operation Modes for PROM Programming

Mode	NMI	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D_0 - D_7
Program write	+12.5 V	L	L	H	+12.5 V	+6 V	Data input
Program verify	+12.5 V	L	H	L	+12.5 V	+6 V	Data output
Program inhibit	+12.5 V	L	H	H	+12.5 V	+6 V	High Z
Read out	+12.5 V	L	L	L	+5 V	+5 V	Data output
Output disable	+12.5 V	L	L	H	+5 V	+5 V	High Z
Standby	+12.5 V	L	H	L/H	+5 V	+5 V	High Z

Note: When +12.5 V is applied to V_{PP} and +6 V to V_{DD}, both $\overline{CE}$ and $\overline{OE}$ cannot be set to low level (L) simultaneously.

DC Programming Characteristics

T_A = 25 ±5°C; V_{IP} = 12.5 ±0.5 V applied to NMI pin; V_{SS} = 0 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Condition
High-level input voltage	V_{IH}	V_{IH}	2.4		V_{DDP}+0.3	V	
Low-level input voltage	V_{IL}	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LIP}	I_{LI}			10	μA	$0 \le V_I \le V_{DDP}$
High-level output voltage	V_{OH1}	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{OH2}	V_{DD} − 0.7			V	I_{OH} = −100 μA
Low-level output voltage	V_{OL}	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}				10	μA	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}
NMI pin high-voltage input current	I_{IP}				±10	μA	
V_{DDP} power voltage	V_{DDP}	V_{CC}	5.75	6.0	6.25	V	Program memory write mode
			4.5	5.0	5.5	V	Program memory read mode
V_{PP} power voltage	V_{PP}	V_{PP}	12.2	12.5	12.8	V	Program memory write mode
				V_{PP} = V_{DDP}		V	Program memory read mode
V_{DDP} power current	I_{DD}	I_{CC}		5	30	mA	Program memory write mode
				5	30	mA	Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}
V_{PP} power current	I_{PP}	I_{PP}		5	30	mA	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}
				1	100	μA	Program memory read mode

* Corresponding symbols of the μPD27C256A.

AC Programming Characteristics (Write Mode)

T_A = 25 ±5°C; V_{IP} = 12.5 ±0.5 V applied to NMI pin; V_{SS} = 0 V; V_{DD} = 6 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Conditions
Address setup time to $\overline{CE}$ ↓	t_{SAC}	t_{AS}	2			μs	
Data input to $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}	2			μs	
Input data setup time to $\overline{CE}$ ↓	t_{SIDC}	t_{DS}	2			μs	
Address hold time from $\overline{CE}$ ↑	t_{HCA}	t_{AH}	2			μs	
Input data hold time from $\overline{CE}$ ↑	t_{HCID}	t_{DH}	2			μs	
Output data hold time from $\overline{OE}$ ↑	t_{HOOD}	t_{DF}	0		130	ns	
V_{PP} setup time to $\overline{CE}$ ↓	t_{SVPC}	t_{VPS}	1			ms	
V_{DDP} setup time to $\overline{CE}$ ↓	t_{SVDC}	t_{VCS}	1			ms	
Initial program pulse width	t_{WL1}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{WL2}	t_{OPW}	2.85		78.75	ms	
NMI high-voltage input setup time to $\overline{CE}$ ↓	t_{SPC}		2			μs	
Address to data output time	t_{DAOD}	t_{ACC}			200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ ↓ to data output time	t_{DCOD}	t_{CE}			200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ ↓ to data output time	t_{DOOD}	t_{OE}			75	ns	$\overline{CE}$ = V_{IL}
Data hold time from $\overline{OE}$ ↑	t_{HCOD}	t_{DF}	0		60	ns	$\overline{CE}$ = V_{IL}
Data hold time from address	t_{HAOD}	t_{OH}	0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

* Corresponding symbols of the μPD27C256A.

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PROM Write Procedure

(1) Connect the $\overline{\text{RESET}}$ pin to a low level, and apply +12.5 V to the NMI pin.

(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.

(3) Provide the initial address.

(4) Provide write data.

(5) Provide 1-ms program pulse (active low) to the $\overline{\text{CE}}$ pin.

(6) This data is now verified with a pulse (active low) to the $\overline{\text{OE}}$ pin. If the data has been written, proceed to step 8; if not, repeat steps 4 to 6. If the data cannot be correctly written after 25 attempts, go to step 7.

(7) Classify as defective and stop write operation.

(8) Provide write data and supply program pulse (for additional writing) for 3 ms times the number of writes performed in steps 5.

(9) Increment the address.

(10) Repeat steps 4 to 9 until the end address.

PROM Read Procedure

(1) Fix the $\overline{\text{RESET}}$ pin to a low level, and apply +12.5 V to the NMI pin.

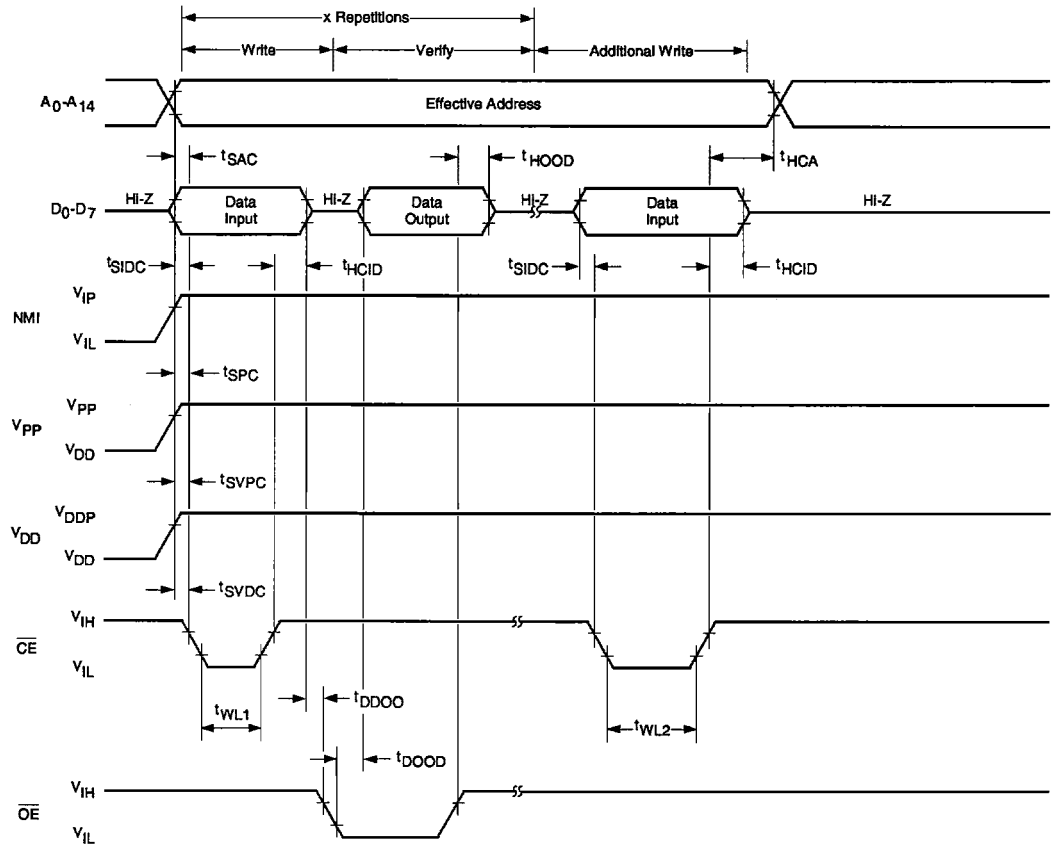
(2) Input the address of the data to be read to pins A_0 - A_{14}.

(3) Read mode is entered with a pulse (active low) on both the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins.

(4) Data is output to the D_0 to D_7 Pins.

PROM Timing Diagrams

PROM Write Mode



Notes:
(1) V_{DD} must be applied before applying V_{PP}. It should be removed after removing V_{PP}.
(2) V_{PP} must not exceed +13V, including overshoot.

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PROM Timing Diagrams

PROM Read Mode