DATA SHEET

FEBRUARY, 1999
Revision 1.2

LXT982/982A Single-Speed, 5-Port Fast Ethernet Repeater for 100BASE-TX/FX Applications

General Description

The LXT982 is a 5-port 100 Mbps Class II Repeater that is fully compliant with IEEE 802.3 standards. Four ports directly support 100BASE-TX copper media or 100BASE-FX fiber media via pseudo-ECL (PECL) interfaces. The fifth port, a 100 Mbps Media Independent Interface (MII), connects to Media Access Controllers MACs) for bridge/switch applications. The MII can also be configured to interface to another PHY device, such as the LXT970. This data sheet applies to all LXT982 products (LXT982, LXT982A, and any subsequent variants), except as specifically noted.

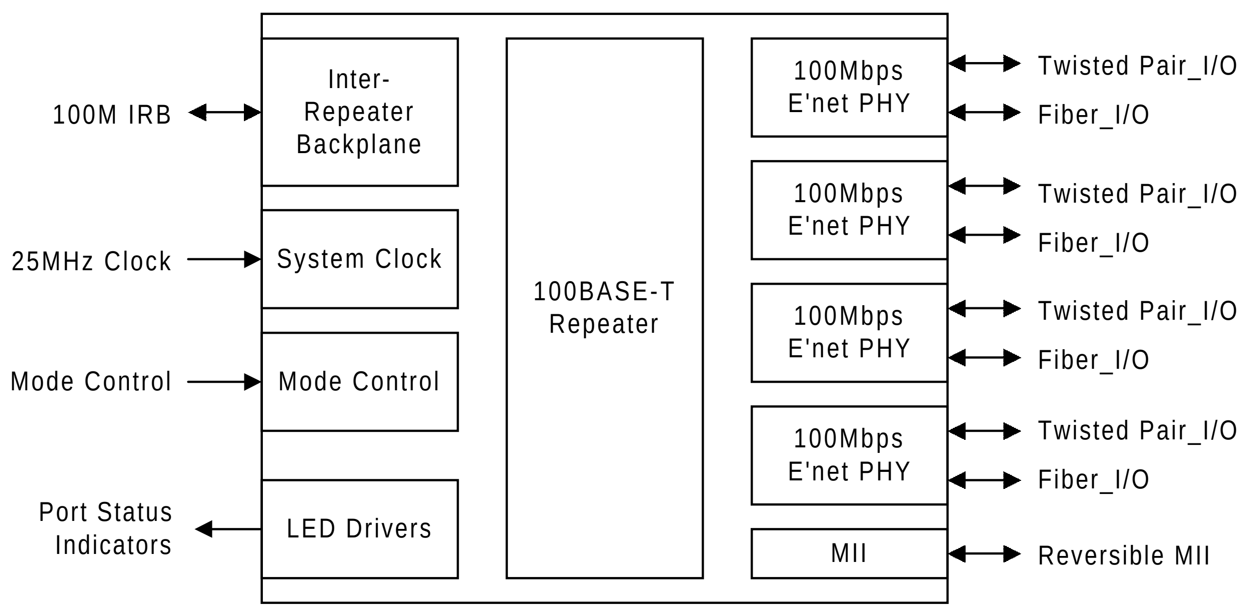
The LXT982 provides an Inter-Repeater Backplane (IRB) for expansion, operating at 100 Mbps. Up to 240 ports can logically be combined into one repeater using this bus.

The LXT982 is an advanced CMOS device packaged in a 208-pin PQFP which operates from a single 5V power supply.

Features

- Four 100BASE-TX ports with complete twisted-pair PHYs including integrated filters.
- Optional support for 100BASE-FX PECL interfaces.
- 100 Mbps MII port connection to either MAC or PHY enables system to meet Class II repeater requirements.
- Cascadable backplane for high-density designs.
- Integrated LED drivers with user-selectable modes.
- Available in 208-pin PQFP package.
- Case temperature range: 0-115°C.

LXT982/982A Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

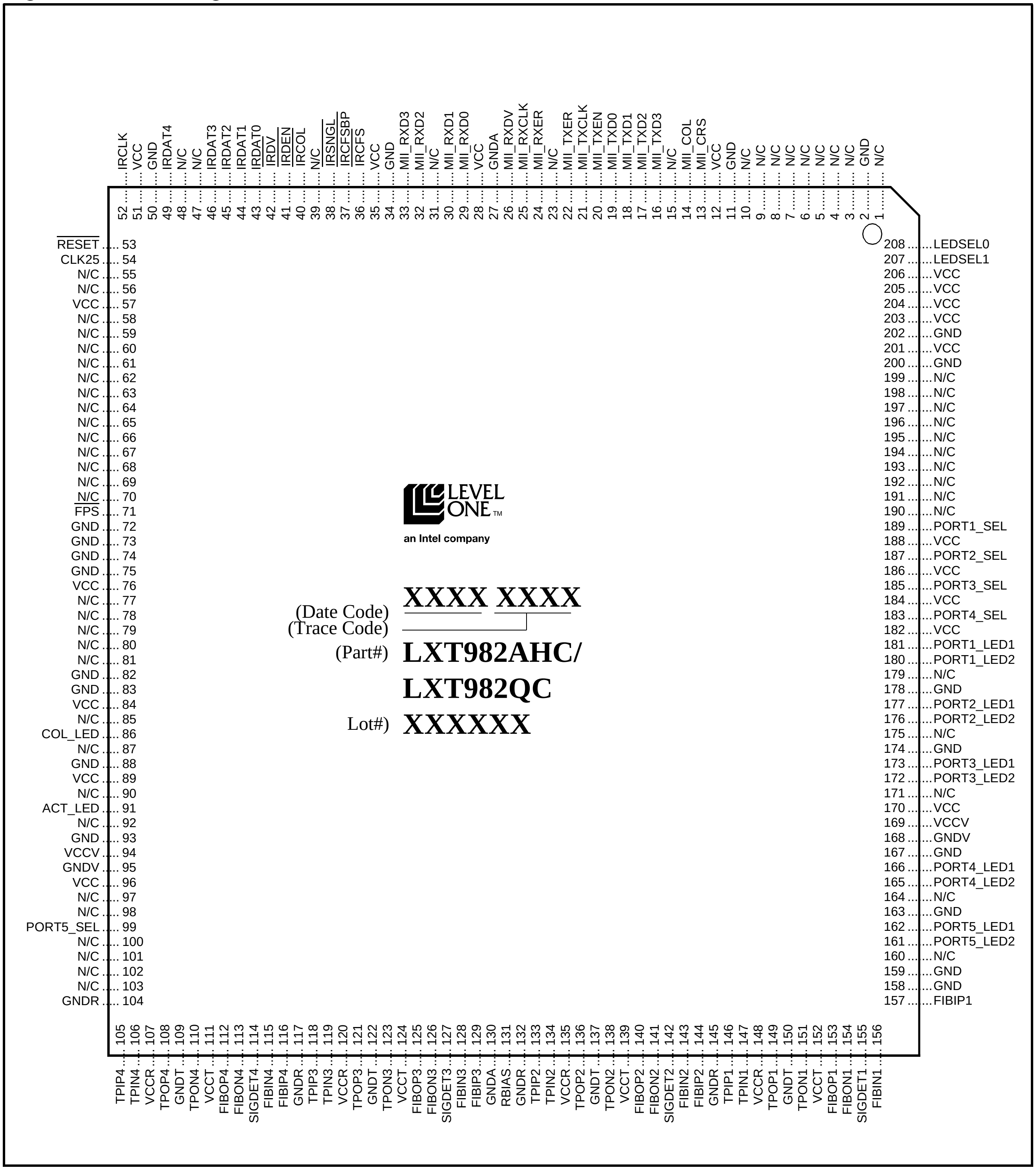

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Table 1: Mode Control Signal Descriptions

Pin	Symbol	Type[1]	Description
189 187 185 183	PORT1_SEL PORT2_SEL PORT3_SEL PORT4_SEL	Input TTL, PU Latched on reset	**Mode Select - Ports 1 through 4.** These pins determine operating mode (copper or fiber) for the associated port as follows: Low = FX High = TX
99	PORT5_SEL	Input TTL, PU	**Mode Select - Port 5.** Selects operating mode of the MII interface. Pin is monitored at power-up and reset. Subsequent changes have no effect. High = PHY Mode (LXT982 acts as PHY side of the MII) Low = MAC Mode (LXT982 acts as MAC side of the MII)

1. NC = No Clamp. Pad will not clamp input in the absence of power.
PU = Input contains pull-up.
PD = Input contains pull-down.
I/O = Input / Output.
TTL = Transistor-Transistor Logic.

Table 2: Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
149, 151 136, 138 121, 123 108, 110	TPOP1, TPON1 TPOP2, TPON2 TPOP3, TPON3 TPOP4, TPON4	Output Analog	**Twisted-Pair Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports twisted-pair line drivers. These pins can be left open when not used.
146, 147 133, 134 118, 119 105, 106	TPIP1, TPIN1 TPIP2, TPIN2 TPIP3, TPIN3 TPIP4, TPIN4	Input Analog	**Twisted-Pair Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports twisted-pair receivers. These pins can be left open when not used.

Table 3: Fiber Port Signal Descriptions

Pin	Symbol	Type	Description
153, 154 140, 141 125, 126 112, 113	FIBOP1, FIBON1 FIBOP2, FIBON2 FIBOP3, FIBON3 FIBOP4, FIBON4	Output PECL	**Fiber Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports PECL drivers. These pins can be left open when not used.
157, 156 144, 143 129, 128 116, 115	FIBIP1, FIBIN1 FIBIP2, FIBIN2 FIBIP3, FIBIN3 FIBIP4, FIBIN4	Input PECL	**Fiber Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports PECL receivers. They can be left open when not used.
155 142 127 114	SIGDET1 SIGDET2 SIGDET3 SIGDET4	Input PECL	**Signal Detect - Ports 1 through 4.** Signal detect for the fiber ports. These pins can be left open when not used.

1. PECL = Pseudo ECL.

Table 4: PHY Mode MII Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Output, TTL	**Receive Data.** The LXT982 transmits received data to the controller on these outputs. Data is driven on the falling edge of MII_RXCLK.
26	MII_RXDV	Output, TTL	**Receive Data Valid.** Active High signal, synchronous to MII_RXCLK, indicates valid data on MII_RXD<3:0>.
25	MII_RXCLK	Output, TTL	**Receive Clock.** MII receive clock for expansion port. This is a 2.5 or 25 MHz clock derived from the CLK25 input (refer to Table 9 on page 10).
24	MII_RXER	Output, TTL	**Receive Error.** Active High signal, synchronous to MII_RXCLK, indicates invalid data on MII_RXD<3:0>.
22	MII_TXER	Input, TTL	**Transmit Error.** The MAC asserts this input when an error has occurred in the transmit data stream. The LXT982 responds by sending "Invalid Code Symbols" on the line.
21	MII_TXCLK	Output, TTL	**Transmit Clock.** 25 MHz continuous output derived from the 25 MHz input clock.
20	MII_TXEN	Input, TTL	**Transmit Enable.** External controllers drive this input High to indicate that data is being transmitted on the MII_TXD<3:0> pins. Tie this input Low if it is unused.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for PHY mode.
2. TTL = Transistor-to-Transistor Logic.

Table 4: PHY Mode MII Interface Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Input, TTL	**Transmit Data.** External controllers use these inputs to transmit data to the LXT982. The LXT982 samples MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Output, TTL	**Collision.** The LXT982 drives this signal High to indicate that a collision has occurred.
13	MII_CRS	Output, TTL	**Carrier Sense.** Active High signal indicates that the LXT982 is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for PHY mode.
2. TTL = Transistor-to-Transistor Logic.

Table 5: MAC Mode MII Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Input, TTL	**Receive Data.** The LXT982 receives data from the PHY on these pins. Data is sampled on the rising edge of MII_RXCLK.
26	MII_RXDV	Input, TTL	**Receive Data Valid.** Active High signal, synchronous to MII_RXCLK, indicates valid data on MII_RXD<3:0>.
25	MII_RXCLK	Input, TTL	**Receive Clock.** MII receive clock for expansion port. This is a 25 MHz clock.
24	MII_RXER	Input, TTL	**Receive Error.** Active High signal, synchronous to MII_RXCLK, indicates invalid data on MII_RXD<3:0>.
22	MII_TXER	Output, TTL	**Transmit Error.** The LXT982 asserts this signal when an error has occurred in the transmit data stream.
21	MII_TXCLK	Input, TTL	**Transmit Clock.** 25 MHz continuous input clock. Must be supplied from same source as CLK25 system clock.
20	MII_TXEN	Output, TTL	**Transmit Enable.** The LXT982 drives this output High to indicate that data is being transmitted on the MII_TXD<3:0> pins.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Output, TTL	**Transmit Data.** The LXT982 drives these outputs to transmit data to the PHY. The device drives MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Input, TTL	**Collision.** High input indicates that a collision has occurred.
13	MII_CRS	Input, TTL	**Carrier Sense.** High indicates that the LXT982 is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for MAC mode.
2. TTL = Transistor-to-Transistor Logic.

Table 6: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type[1]	Description [2]
43 44 45 46 49	IRDAT0 IRDAT1 IRDAT2 IRDAT3 IRDAT4	I/O CMOS Tri-state Schmitt PU	**IRB Data.** These bidirectional signals carry data on the 100 Mbps IRB. Data is driven on the falling edge and sampled on the rising edge of IRCLK. These signals can be buffered between boards.
52	IRCLK	I/O CMOS Tri-state Schmitt PD	**IRB Clock.** This bidirectional, non-continuous, 25 MHz clock is recovered from received network traffic. This signal must be pulled to VCC when idle. One 1 kΩ pull-up resistor on both sides of a '245 buffer is recommended.
41	IRDEN	Output TTL, OD	**IRB Driver Enable.** This output provides directional control for an external bidirectional transceiver ('245) used to buffer the 100 Mbps IRB in multi-board applications. It must be pulled up by a 330Ω resistor. When there are multiple devices on one board, tie all IRDEN outputs together. If IRDEN is tied directly to the DIR pin on a '245, attach the on-board IRDAT, IRCLK and IRDV signals to the "B" side of the '245, and connect the off-board signals to the "A" side of the '245.
42	IRDV	I/O CMOS Schmitt OD, PU	**IRB Data Valid.** An active Low signal indicating repeater port activity. IRDV frames the clock and data of the packet on the backplane. This signal requires a 120Ω pull-up resistor.
36	IRCFS	I/O Analog	**IRB Collision Force Sense.** This three-level signal determines the number of active ports on the "logical" repeater. High level (5V) indicates no ports active; Mid-level (approx. 2.8V) indicates one port active; Low level (0V) indicates more than one port active, resulting in a collision. IRCFS connects between chips on the same board. Do not connect between boards. This signal requires a 240Ω pull-up resistor.
37	IRCFSBP	I/O Analog NC	**IRB Collision Force Sense - Backplane.** A three-level signal that functions the same as IRCFS; however, IRCFSPB connects between chips with ChipID = 0, on different boards. This signal requires a single 91Ω pull-up resistor on each stack.
38	IRSNGL	I/O CMOS Schmitt, PU	**IRB Single Driver State.** This active Low signal is asserted by the device with FPS Low when a packet is being received from one or more ports. It should not be connected between boards.
40	IRCOL	I/O CMOS Schmitt, PU	**IRB Multiple Driver State.** This active Low signal is asserted by the device with FPS Low when a packet is being received from more than one port (collision). It should not be connected between boards.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up
   PD = Input contains pull-down
   I/O = Input / Output
   OD = Open Drain
2. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 7: LED Signal Descriptions

Pin	Symbol	Type	Description
208 207	LEDSEL0 LEDSEL1	Input TTL, PD	**LED Mode Select**. Must be static. 00 = Mode 1, 01 = Mode 2, 10 = Mode 3
181 177 173 166 162	PORT1_LED1 PORT2_LED1 PORT3_LED1 PORT4_LED1 PORT5_LED1	Output TTL	**LED Driver 1 - Ports 1 through 5.** Programmable LED driver. Active Low. See “Per Port LEDs” on page 14.
180 176 172 165 161	PORT1_LED2 PORT2_LED2 PORT3_LED2 PORT4_LED2 PORT5_LED2	Output, TTL	**LED Driver 2 - Ports 1 through 5.** Programmable LED driver. Active Low. See “Per Port LEDs” on page 14.
86	COL_LED	Output, TTL	**Collision LED Driver.** Active Low indicates collisions.
91	ACT_LED	Output, TTL	**Activity LED Driver.** Active Low indicates activity.

1. TTL = Transistor-to-Transistor Logic.

Table 8: Power Supply and Indication Signal Descriptions

Pin	Symbol	Type	Description
12, 28, 35, 51, 57, 76, 84, 89, 96, 170, 182, 184, 186, 188, 201, 203-206	VCC	Digital	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to digital ground should be supplied for every one of these pins.
2, 11, 34, 50, 72-75, 82, 83, 88, 93, 158, 159, 163, 167, 174, 178, 200, 202	GND	Digital	**Ground.** Connect each of these pins to ground. For LXT982, Chip ID 1 is Pin 72; Chip ID 2 is Pin 73. If using an LXT982 device in an LXT981-based design, these pins do not have to be tied to ground.
94, 169	VCCV	Analog	**VCO Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDV should be supplied for every one of these pins.
95, 168	GNDV	Analog	**VCO Ground**.
111, 124, 139, 152	VCCT	Analog	**Transmitter Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDT should be supplied for every one of these pins.

Table 8: Power Supply and Indication Signal Descriptions – continued

Pin	Symbol	Type	Description
109, 122, 137, 150	GNDT	Analog	**Transmitter Ground.**
107, 120, 135, 148	VCCR	Analog	**Receiver Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDR should be supplied for every one of these pins
104, 117, 132, 145,	GNDR	Analog	**Receiver Ground.**
131	RBIAS	Analog	**RBIAS.** Used to provide bias current for internal circuitry. The 100 µA bias current is provided through an external 22.1 kΩ, 1% resistor to GNDA.
27, 130	GNDA	Analog	**Analog Ground.**

Table 9: Miscellaneous Signal Descriptions

Pin	Symbol	Type	Description
53	$\overline{\text{RESET}}$	Input CMOS Schmitt, NC	**Reset.** This active Low input causes internal circuits, state machines and counters to reset (address tracking registers do not reset). On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5 V. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an ‘LS14 or similar device.
54	CLK25	Input CMOS Schmitt	**25 MHz System Clock.** Drive with MOS levels.
71	$\overline{\text{FPS}}$	Input, TTL	**First Position Select.** Set Low for first device on PCB. Set High for all other devices on PCB. If using an LXT982 device in an LXT981-based design, $\overline{\text{FPS}}$ is analogous to Chip ID 0 on the LXT981.
1, 3-10, 15, 23, 31, 39, 47, 48, 55, 56, 58-70, 77-81, 85, 87, 90, 92, 97, 98, 100-103, 160, 164, 171, 175, 179, 190-199	NC	-	**No Connects.** Leave these pins unconnected.

1. NC = No Clamp. Pad will not clamp input in the absence of power.

FUNCTIONAL DESCRIPTION

Introduction

As a fully integrated IEEE 802.3 repeater capable of 100 Mbps functionality, the LXT982 is a very versatile device allowing great flexibility in Ethernet design solutions. Figure 2 shows a typical application, and Figure 3 shows a more complete I/O circuit. Refer to Application Information (page 19) for specific circuit implementations.

This multi-port repeater provides four 100BASE-TX/ 100BASE-FX ports. In addition, there is a bidirectional Media Independent Interface (MII) expansion port that may be connected to either a 100 Mbps MAC, or to a 100 Mbps PHY.

The LXT982 provides a repeater state machine and an Inter-Repeater Backplane (IRB). The 100 Mbps repeater fully meets IEEE 802.3 Class II requirements.

Port Configuration

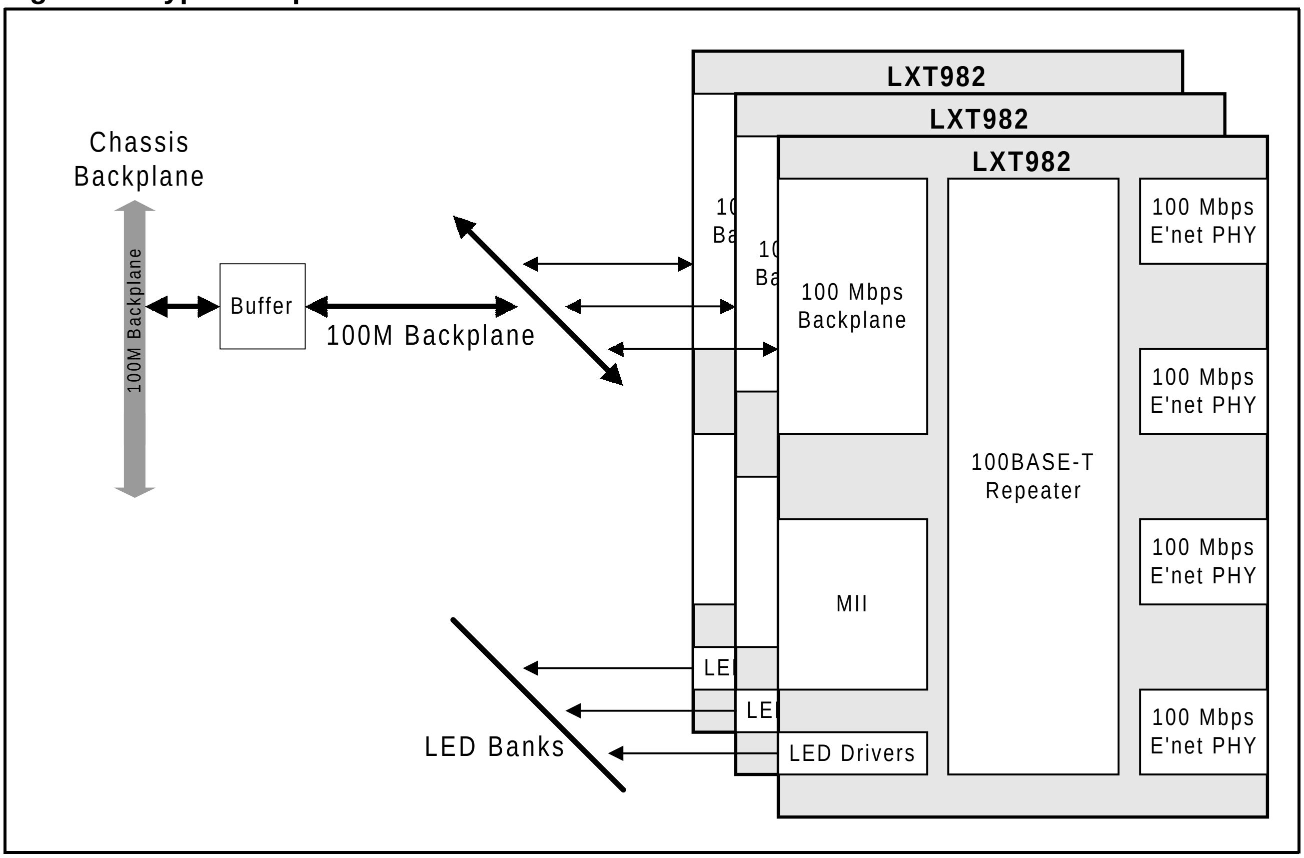
The LXT982 reads the hardware configuration pins at power-up, hardware reset or software reset (but not at repeater reset), to determine operating conditions for each of its ports. Each of the four media ports has its own configuration pin (PORT*n*_SEL) to select 100TX or 100FX operation (High = TX, Low = FX).

Interface Descriptions

100BASE-TX Interface

The twisted-pair interface for each port consists of two differential signal pairs — one for transmit and one for receive. The transmit signal pair is TPOP/TPON, the receive signal pair is TPIP/TPIN. Refer to Table 2 for 100BASE-T port pin assignments and signal descriptions. The twisted-pair interface for a given port is always enabled except when 100FX is selected.

Figure 2: Typical Repeater Architectures



The transmitter is current driven and requires magnetics with 2:1 turns ratio. A 400Ω resistive load should be placed across the TPOP/N pair, in parallel with the magnetics. The center tap of the primary side of the transmit winding must be tied to a quiet VCC for proper operation. When the twisted-pair interface is disabled, the transmitter outputs are tri-stated.

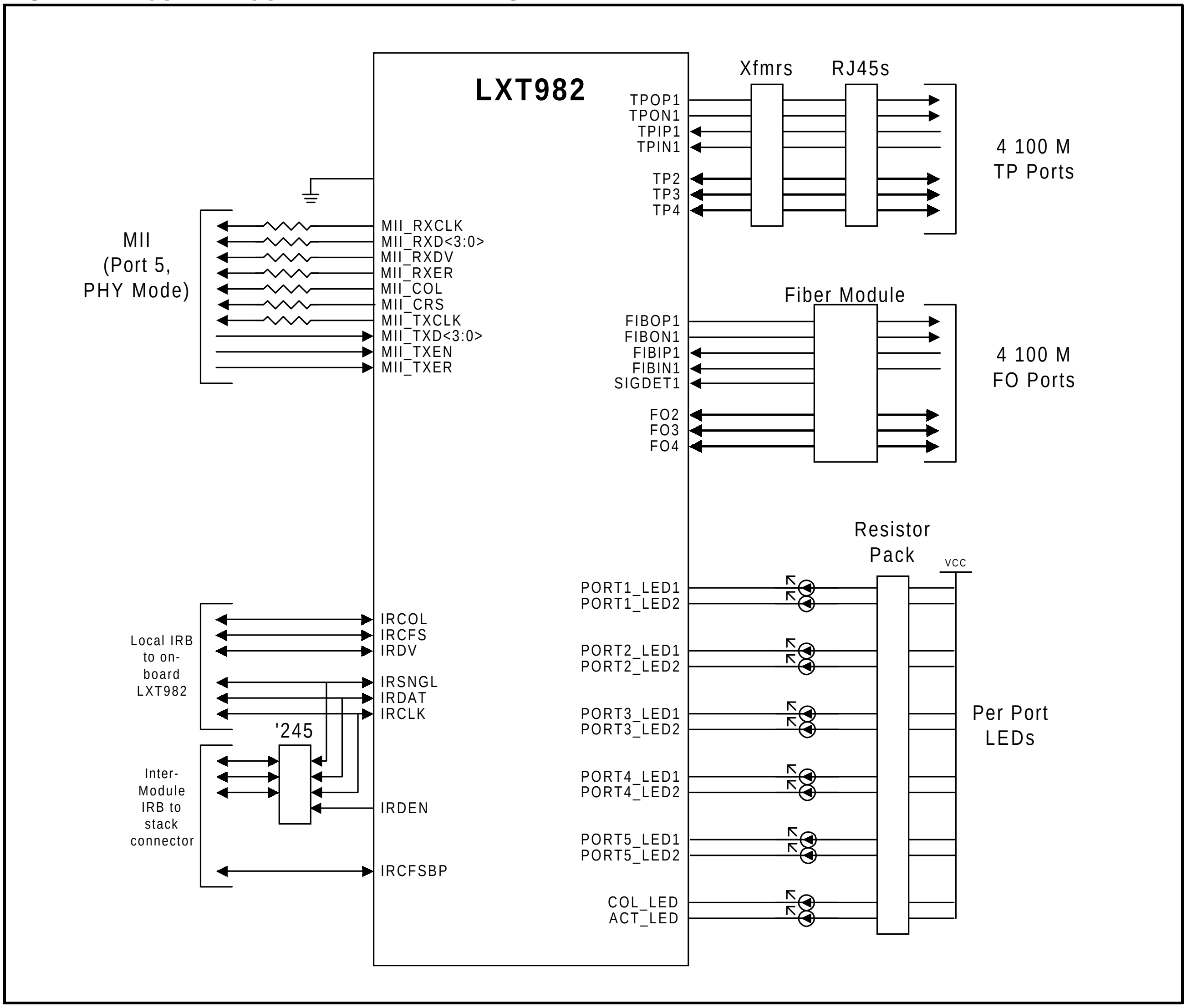
The receiver requires magnetics with a 1:1 turns ratio, and a load of 100Ω. When the twisted-pair port is enabled, the receiver actively biases its inputs to approximately 2.8V. When the twisted-pair interface is disabled, no biasing is provided. A 4 kΩ load is always present across the TPIP/TPIN pair.

The LXT982 sends and receives a continuous, scrambled 125Mbaud MLT-3 waveform on this interface. In the absence of data, *IDLE* symbols are sent and received in order to keep the link up.

100BASE-FX Interface

Each fiber interface consists of the FIBOP/FIBON (transmit) and FIBIP/FIBIN (receive) signal pair. Refer to Table 3 for 100BASE-FX port pin assignments and signal descriptions. Each interface also provides a "Signal Detect" input that can be tied to the corresponding output on the fiber transceiver for determining signal presence and quality.

Figure 3: Typical Application Block Diagram



The transmit pair is biased to approximately 1.5V and generally must be AC-coupled to the transceiver. The receive pair will accommodate an input bias in the 2V-5V range, and can be DC-coupled to the transceiver. Refer to Figure 10 on page 24 for a typical interface circuit.

The fiber interface for each port is enabled when the mode select is set to 100FX, and is disabled in all other cases. When a fiber port is disabled, its outputs are pulled to ground, and its inputs are tri-stated. The input and output pins on unused fiber ports may be left unconnected.

Each fiber port transmits and receives a continuous, 1V peak-to-peak, non-scrambled, NRZI waveform. The LXT982 does not support scrambling on the fiber interface.

Remote Fault Reporting

The SD pin detects signal quality and reports a remote fault if the signal quality starts to degrade. Loss of signal quality will also block any further data from being received and causes loss of the link. The remote fault code consists of 84 consecutive 1s followed by a single 0, and is transmitted at least three times. The LXT982 transmits the remote fault code when both of the following conditions are true:

- Fiber mode is selected.
- Signal Detect indicates no signal, or the receive PLL cannot lock.

Media Independent Interface

The LXT982 supports a standard Media Independent Interface (MII) interface. This interface can be programmed to operate either as the PHY side of the interface (PHY mode) or as the MAC side of the interface (MAC mode). The MII always operates as a nibble-wide (4B) interface. Symbol mode (5B interface) is not supported on the LXT982 MII.

NOTE: The MII does not auto-negotiate, auto-speed select, or partition.

Inter-Repeater Backplane

The LXT982 provides an Inter-Repeater Backplane (IRB) that allows multiple cascaded LXT982 devices to function as one large repeater. Up to 240 ports can be supported in a single cascade (192 TP ports + 48 MII ports). This provides support for stackable and modular hub architectures. Refer to Table 6 for IRB pin assignments and signal descriptions.

Repeater Operation

The LXT982 contains a complete 100 Mbps repeater state machine that is fully IEEE 802.3 Class II compliant. Multiple LXT982s can be cascaded on the IRB and operate as one repeater segment. Data from any port will be forwarded to any other port in the cascade. The IRB is a 5-bit symbol-mode interface. It is designed to be stackable.

The LXT982 performs the following 100 Mbps repeater functions:

- Signal amplification, wave-shape restoration, and data-frame forwarding.
- Handling received code violations. The LXT982 substitutes the “H” symbol for all invalid received codes.
- SOP, SOJ, EOP, EOJ delay <46 BT (class II compliant).
- Collision Enforcement. During a collision, the LXT982 drives a 1010 jam signal (encoded as Data 5 on TX links) to all ports until the collision ends. There is no minimum enforcement time.
- Partition. The LXT982 partitions any port that participates in excess of 60 consecutive collisions or one collision that is approximately 575.2 µs long. Once partitioned, the LXT982 continues monitoring and transmitting to the port, but will not repeat data received from the port until it properly unpartitions.
- Un-partition. The LXT982 un-partitions a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.
- Isolate. The LXT982 will isolate any port that transmit more than two successive false carrier events. A false carrier event is defined as a packet that does not start with a /J/K symbol pair. Note: this is not the same function as the IRB isolate function, which involves segmenting the backplane.
- Un-isolate. The LXT982 will un-isolate a port that remains in the IDLE state for 33000 +/- 25% BT or that receives a valid frame at least 450-500BT in length.
- Jabber. The LXT982 ignores any receiver that remains active for more than 57,500 bit times. The LXT982 exits this state when all jabbering receivers return to the idle condition.

The isolate and symbol error functions do not apply to the MII port.

Requirements

Power

The LXT982 has four types of +5V power supply input pins (VCC, VCCV, VCCR, and VCCT). These inputs may be supplied from a single power supply although ferrites should be used to filter the analog and digital power planes. As a matter of good practice, these supplies should be as clean as possible. Specific operating recommendations are shown in the Test Specifications section, Table 15 on page 27.

Each supply input should be decoupled to its respective ground. Refer to Table 6 on page 8 for power and ground pin assignments, and to the Design Recommendations section on page 19.

Clock

A stable, external 25 MHz system clock source (CMOS) is required by the LXT982. This is connected to the CLK25 pin. Refer to Test Specifications, Table 16 on page 27, for clock input requirements.

Bias Current

The LXT982 requires a 22.1 kΩ, 1% resistor connecting its RBIAS input to ground.

Reset

At power-up, the reset input must be held low until VCC reaches at least 4.5V. An 'LS14 or equivalent should be used to drive reset if there are multiple LXT982 devices. Refer to Figure 13 on page 26 for circuit details.

IRB Bus Pull-ups

Even when the LXT982 is used in a stand-alone configuration, pull-up resistors are required on the following IRB signals: IRCFS, IRCFSBP, IRCLK, and IRDV. Refer to Table 6 for IRB pin assignments and signal descriptions. See Figure 12 on page 26 for sample circuits.

LED Operation

The LXT982 provides 2 mode-selectable per-port LED drivers (10 total), and 2 global LED drivers. Refer to Table 7 for LED Interface pin assignments and signal descriptions.

Power-Up and Reset Conditions

During reset or power-up, all LEDs turn on solid and remain on for approx. 2 seconds after reset goes away.

Per Port LEDs

The Per Port LEDs apply to the four twisted-pair ports and the MII port. The LXT982 has 2 LED driver pins for each port as described in Table 7. These pins can drive standard LEDs (see Table 10).

Global LEDs

These outputs can directly drive LEDs to indicate activity and collision status. Pulse stretchers extend the on-time for these LEDs.

Collision LED

The collision LED will turn on for approximately 120 µs when the LXT982 detects a collision. During the time that the collision LED is on, any additional collisions will be ignored by the collision LED logic.

Activity LED

The activity LED will turn on for approximately 4 ms when the LXT982 detects any activity. During the time that the activity LED is on, any additional activity will be ignored by the activity LED logic.

Table 10: LED Indicators (Per Port)

Mode	Port LED	LED State	Indication
1	1	On	Link is good, port is not partitioned and not isolated.
	2	On	Link is good and port is partitioned or isolated.
2	1	On steady	Port enabled, link is good, port is not partitioned and not isolated.
		1.6s Blink	Link is good, port enabled, (partitioned or isolated).
	2	Off	Always off.
3	1	On	Link is good, and port is not isolated and not partitioned.
	2	On	20 ms pulse for receive activity on port.
	3	On	Link is good and port is partitioned or isolated.

IRB Operation

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. This backplane uses a combination of digital and analog signals. IRB signals can be characterized by connection type as Local (connected between devices on the same board), Stack (connected between boards) or Full (connected between devices on the same board *and* between different boards). Refer to Tables 11 and 12 for details on buffering and pull-up requirements, and to Figure 12 on page 26 for application circuitry.

IRB Isolation

The ISOLATE output is provided to control the enable pin of an external bidirectional transceiver. In multi-board applications, it can be used to isolate one board from the rest of the system. Only one device (the device with $\overline{\text{FPS}}$ Low) can control these signals. The output states of this pin are controlled by the internal repeater state machine.

Inter-board analog signals are isolated internally by the device.

If an LXT982 device is used in an LXT981-based design, Chip ID 0 of the LXT981 is renamed $\overline{\text{FPS}}$ for the LXT982.

Table 11: IRB Signal Types

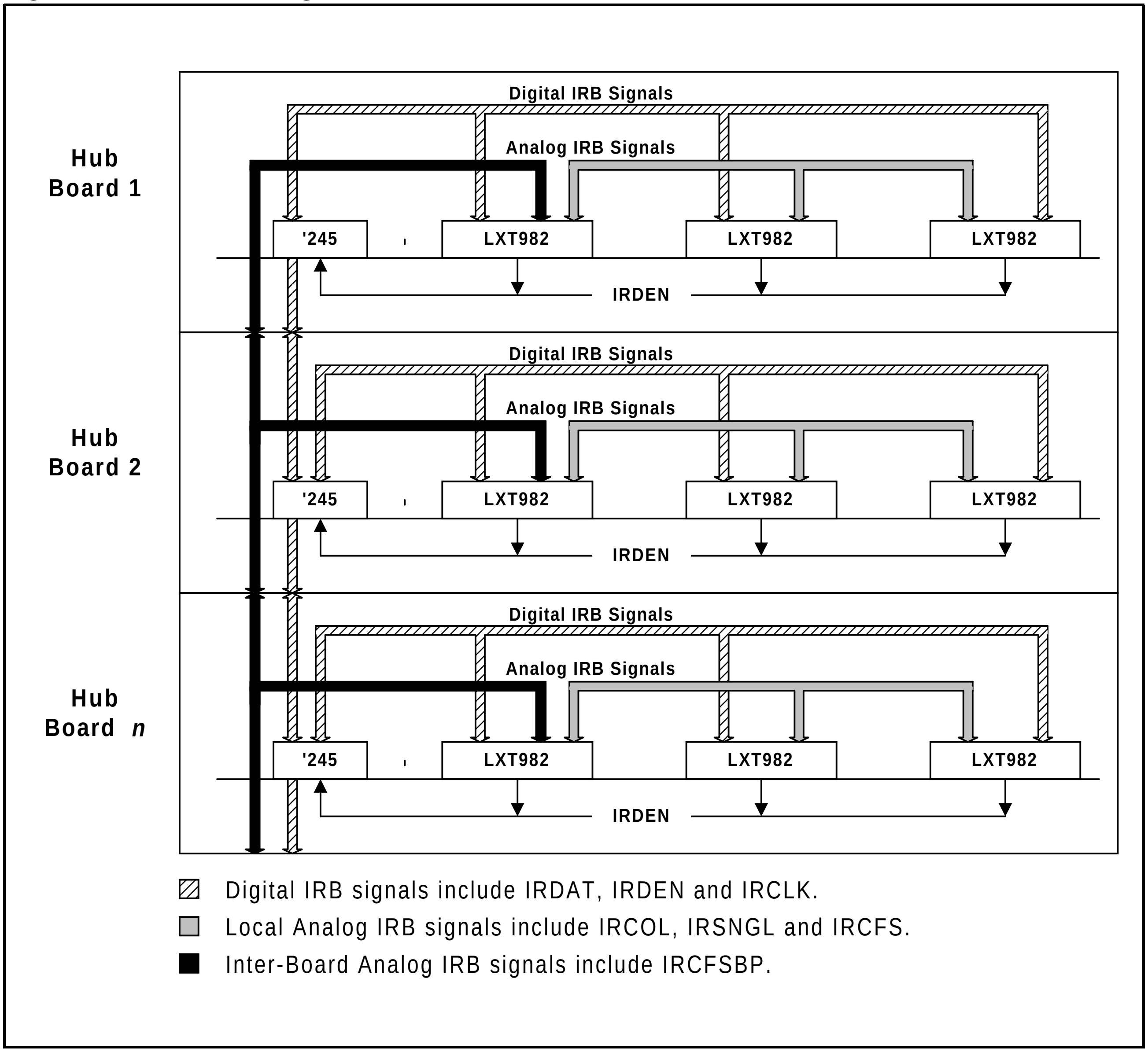
Connection Type	Connections Between Devices (same board)	Connections Between Boards
Full	Connect All.	Connect using buffers.
Local	Connect All.	Do not connect.
Stack	For devices with $\overline{\text{FPS}}$ High, pull-up at each device and do not interconnect.	Connect devices with $\overline{\text{FPS}}$ Low between boards. Use one pull-up resistor per stack.
Special (xxISO)	For devices with $\overline{\text{FPS}}$ High, leave open. For device with $\overline{\text{FPS}}$ Low, connect to buffer enable.	Do not connect.

Table 12: IRB Signal Details

Name	Pad Type	Buffer	Pull-up	Connection Type
IRDAT<4:0>	Digital	Yes	No	Full
IRCLK	Digital	Yes	1 kΩ	Full
$\overline{\text{IRDV}}$	Digital, Open Drain	Yes	120Ω	Full
$\overline{\text{IRCFS}}$	Analog	No	240Ω, 1%	Local
$\overline{\text{IRCFSBP}}$	Analog	No	91Ω, 1%[2]	Stack
$\overline{\text{IRCOL}}$	Digital	No	No	Local
$\overline{\text{IRSNGL}}$	Digital	No	No	Local
$\overline{\text{IRDEN}}$	Digital, Open Drain	N/A[1]	330Ω	Local
IRISO	Digital	N/A[1]	No	Special

1. Isolate and Driver Enable signals are provided to control an external bidirectional transceiver.
2. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

Figure 4: IRB Block Diagram



MII Port Operation

The LXT982 MII allows a MAC or PHY to directly connect into the repeater environment. The LXT982 can emulate either the PHY (PHY Mode) or MAC (MAC Mode) side of the MII as shown in Figure 5. Mode control is provided via the PORT5_SEL pin (High = PHY Mode, Low = MAC Mode).

PHY Mode Operation

PHY Mode allows the LXT982 to interface to a 100 Mbps MAC. The LXT982 passes the full 56 bits of preamble through before sending the SFD.

MAC Mode Operation

MAC Mode allows the user to attach an additional PHY to the LXT982. In this mode the PHY provides both MII_TXCLK and MII_RXCLK. The MII_TXCLK must be frequency-locked to the 25 MHz oscillator used by the LXT982. The LXT982 does not provide an elasticity buffer to compensate for frequency differences. When operating in MAC mode, the LXT982 generates the full 56 bits of preamble before sending the SFD across the MII.

MII Port Timing Considerations

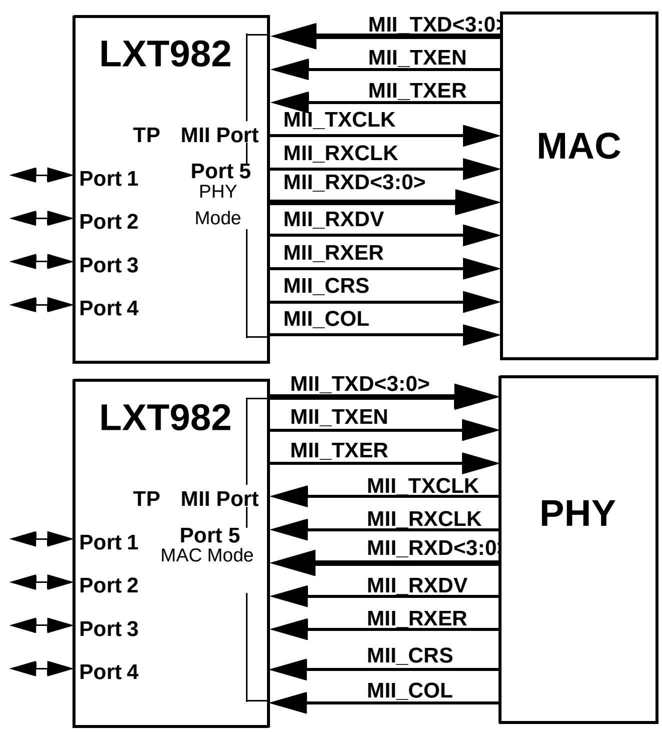
The IEEE 802.3u specification provides propagation delay constraints for standard PHY devices in Section 24.6, and for Repeater devices in Section 27. The LXT982 MII port is a hybrid that does not fit either of these categories. The critical consideration that applies to the LXT982 MII port is the overall end-to-end system propagation delay (132 Bit Times maximum). The LXT982 supports the intent of the Class II repeater application. Figure 6 summarizes the propagation delay issues relevant to the LXT982 MII port.

Figure 5: MII (Port 5) Operation

The LXT982 MII port is reversible.

When PHY mode is selected, the LXT982 acts as the PHY side of the MII. In this mode an external MAC sends TXData to the LXT982 to be repeated to the network. The LXT982 repeats network data to the MAC via the RXData lines.

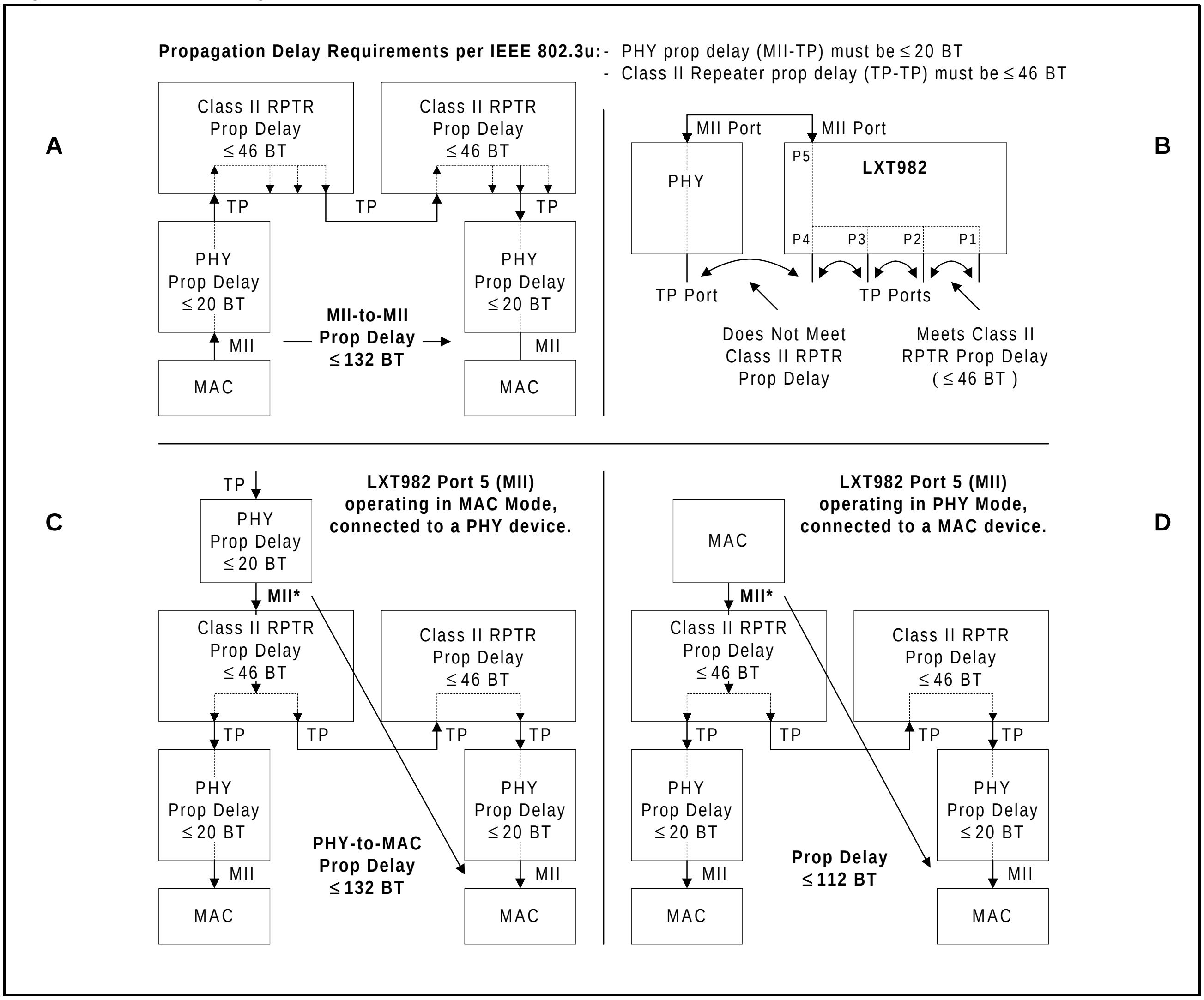
When MAC mode is selected, the LXT982 acts as the MAC side of the MII. In this mode the LXT982 repeats network data to the PHY via the TX Data lines.



The LXT982 architecture treats the MII port as a fifth repeater port. The timing delay (latency) from the MII port to any other port meets the requirements for a Class II repeater (≤ 46 BT). It does not meet the requirements for a standard MII-PHY interface (20 - 24 BT). When operating in MAC mode with a PHY connected to the LXT982 MII port (Figure 6B), the fifth TP port does not have the latency characteristics of a Class II repeater with respect to the other ports.

With a MAC connected to the LXT982 MII port (Figure 6D), the maximum latency to any other MAC is 112 BT (not including cable delay). The MAC connected to the LXT982 has an advantage relative to other MACs because it has one less transceiver delay.

Figure 6: MII Timing Issues



APPLICATION INFORMATION

Design Recommendations

The LXT982 has been designed to comply with IEEE requirements and to provide outstanding receive BER and long-line-length performance. Lab testing has shown that the LXT982 can perform well beyond the required distance of 100m. As with any finely crafted device, reaping the full benefits of the LXT982 requires attention to detail and good design practice.

General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of .01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT982 and the RJ45 connectors at the edge of the board.
- Do not extend any circuit power or ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having these problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (>32-bits) running at a high clock rate.
- DC-to-DC converters.

Many of these issues can be improved just by following good general design guidelines. In addition, Level One also recommends filtering between the power supply and the analog VCC pins of the LXT982. Filtering has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT982, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

The recommended implementation is to divide the VCC plane into two sections. The digital section supplies power to the digital VCC pin, MII VCC pin, and to the external components. The analog section supplies power to VCCH, VCCT, and VCCR pins of the LXT982. The break between the two planes should run under the device. In designs with more than one LXT982, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. The beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. Each LXT982 draws a maximum of 500 mA from the analog supply so beads rated at 750 mA should be used. A bulk cap (2.2 -10 µF) should be placed on each side of each ferrite bead to stop switching noise from traveling through the ferrite.

In addition, a high-frequency bypass cap (.01 µf) should be placed near each analog VCC pin.

Ground Noise

The best approach to minimize ground noise is strict use of good general design guidelines and by filtering the VCC plane.

Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes. The following guidelines are recommended:

- Follow the guidelines in the *LXT980 Design and Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPOP/N and TPIP/N signals, away from the magnetics, and away from the RJ45 connectors.
- Place the layers so that the TPOP/N and TPIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPOP and TPIP/N.

Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ45 connectors to the magnetics, and can be used to terminate unused signal pairs (‘Bob Smith’ termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2kV isolation to the Bob Smith termination.

MII Terminations

Series termination resistors are recommended on all MII signals driven by the LXT982. The proper value equals nominal trace impedance minus 13Ω. If the nominal trace impedance is not known, use 55Ω.

The RBIAS Pin

The LXT982 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to a ground. Surround the RBIAS trace with a ground; do not run high-speed signals next to RBIAS.

The Twisted-Pair Interface

Because the LXT982 transmitter uses 2:1 magnetics, system designers must take extra precautions to minimize parasitic shunt capacitance in order to meet return loss specifications. These steps include:

- Use compensating inductor in the output stage (see Figure 11).
- Place magnetics as close as possible to the LXT982.
- Keep transmit pair traces short.
- Do not route transmit pair adjacent to a ground plane. If possible, eliminate planes under the transmit traces completely. Otherwise, keep planes 3-4 layers away.
- Some magnetic vendors are producing magnetics with higher than average return loss performance. Use of these improved magnetics increases the return loss budget available to the system designer.
- Improve EMI performance by filtering the output centertap. A single ferrite bead may be used to supply centertap current to all four ports.

In addition, follow all the standard guidelines for a twisted-pair interface:

- Route the signal pairs differentially, close together. Allow nothing to come between them.
- Keep distances as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- If possible, place entire receive termination network on one side and transmit on the other.
- Keep termination circuits close together and on the same side of the board.
- Always put termination circuits close to the source end of any circuit.
- Bypass common-mode noise to ground on the in-board side of the magnetics using 0.01 µF capacitors.

The Fiber Interface

The fiber interface consists of a pseudo-ECL (PECL) transmit and receive pair to an external fiber optic transceiver. The transmit pair should be AC coupled to the transceiver, and biased to 3.7V with a 50Ω equivalent impedance. The receive pair can be DC-coupled, and should be biased to 3.0V with a 50Ω equivalent impedance. Figure 10 on page 24 shows the correct bias networks to achieve these requirements.

Magnetics Information

The LXT982 requires a 1:1 ratio for the receive transformers and a 2:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Tables 13 for specifications. Refer to *Magnetic Manufacturers for Networking Product Applications* (App. Note 73) for a reference list of compatible magnetic components from various manufacturers. Before committing to a specific component, designers should test and validate the magnetics in the specific application to verify that system requirements are met.

Table 13: Magnetics Specifications

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	2 : 1	–	–	
Insertion loss	0.0	–	1.1	dB	80 MHz
Primary inductance	350	–	–	µH	
Transformer isolation	–	2	–	kV	
Differential to common mode rejection	–	–	-40	dB	.1 to 60 MHz
	–	–	-35	dB	60 to 100 MHz
Return Loss - Standard	–	–	-16	dB	30 MHz
	–	–	-10	dB	80 MHz
Return Loss - Improved	–	–	-20	dB	30 MHz
	–	–	-15	dB	80 MHz

Typical Application Circuitry

Figures 7 and 8 are simplified block diagrams showing typical applications. Figures 9 through 13 show application circuitry details.

Figure 7: Typical Repeater Stack

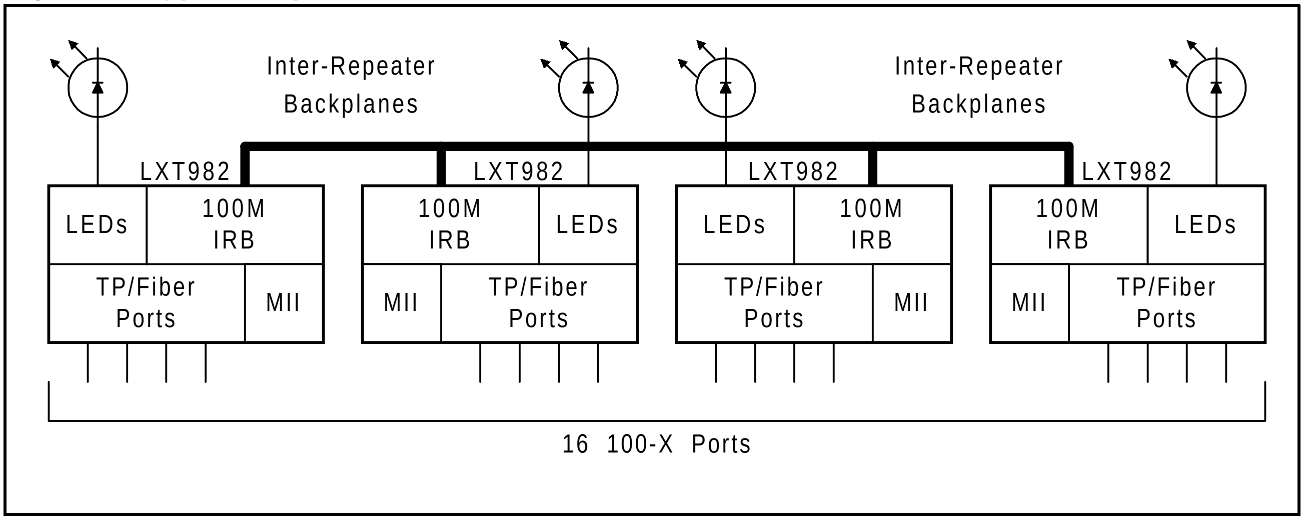


Figure 8: Hybrid Switch/Repeater Application

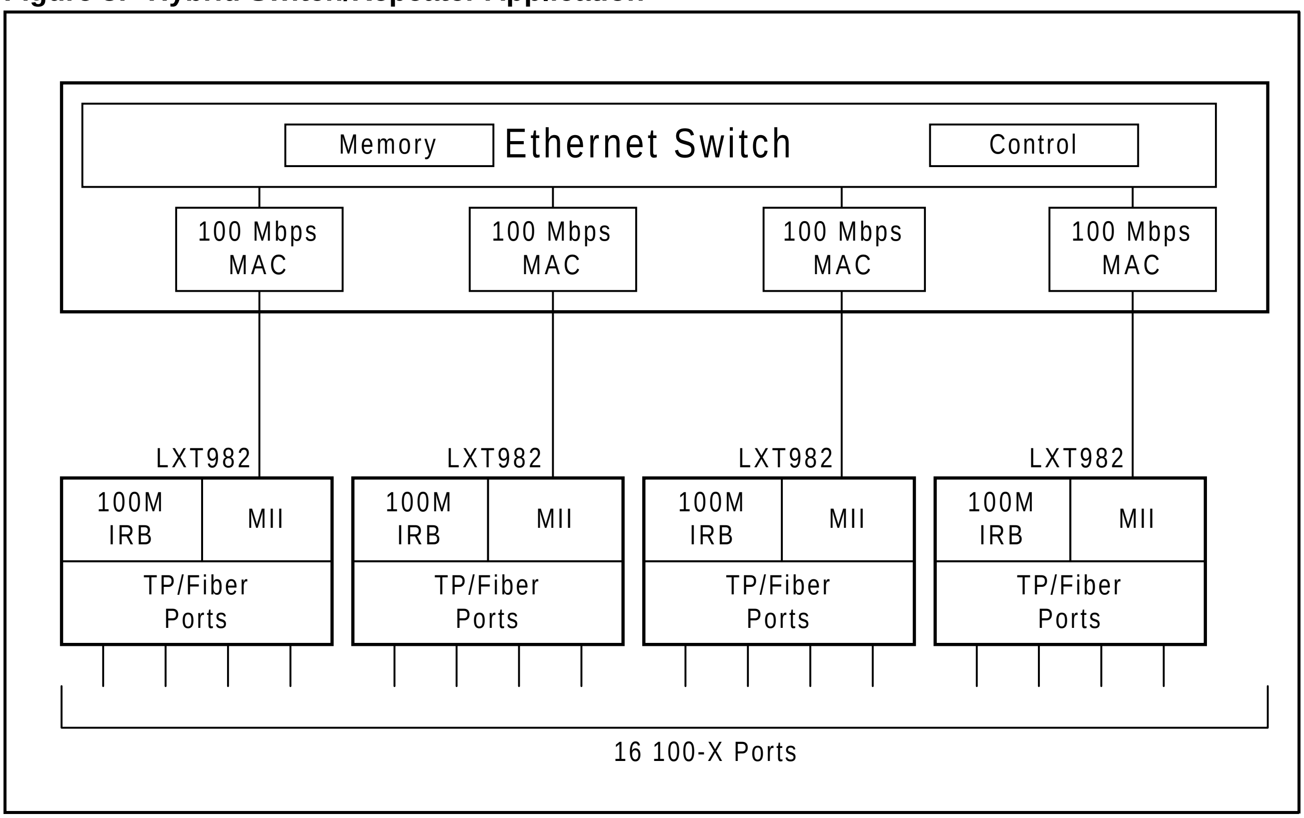


Figure 9: Power and Ground Connections

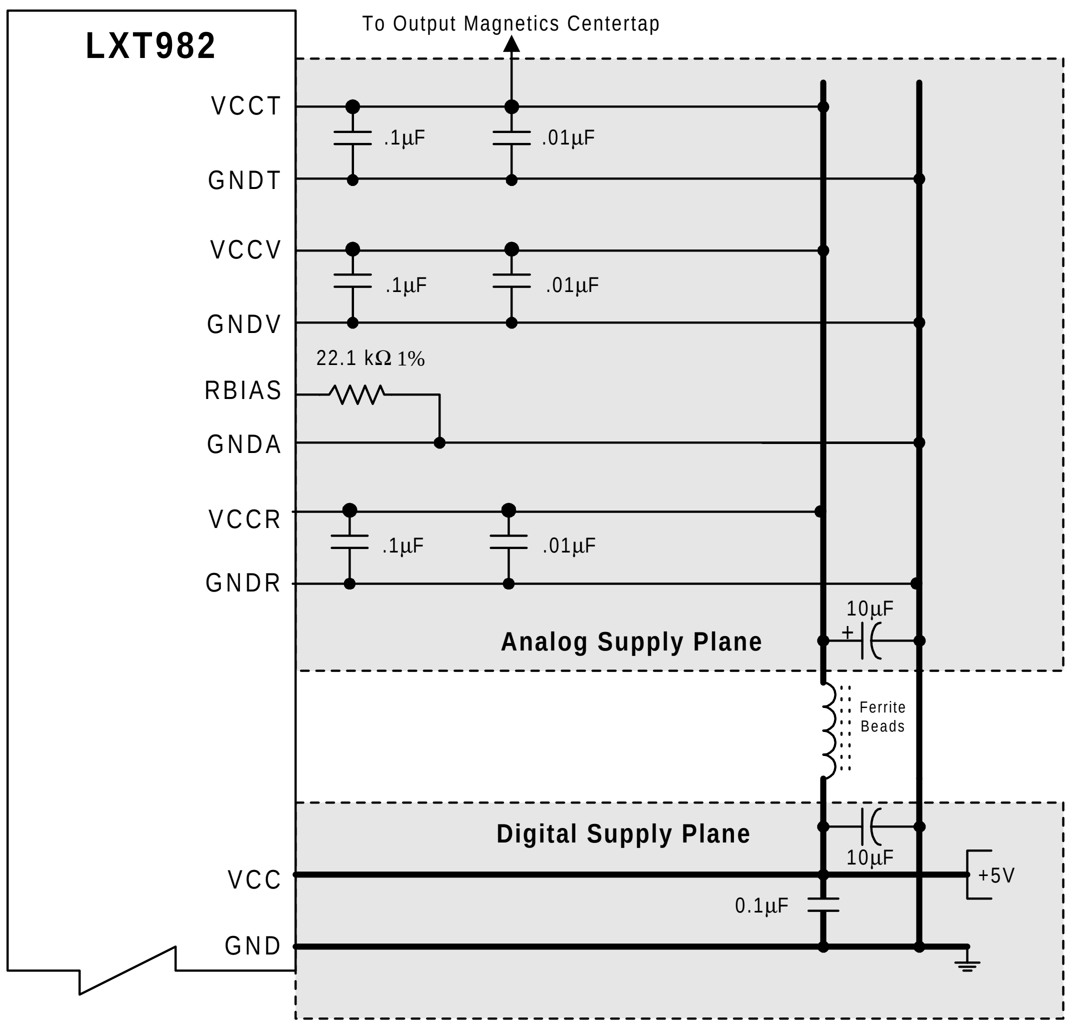
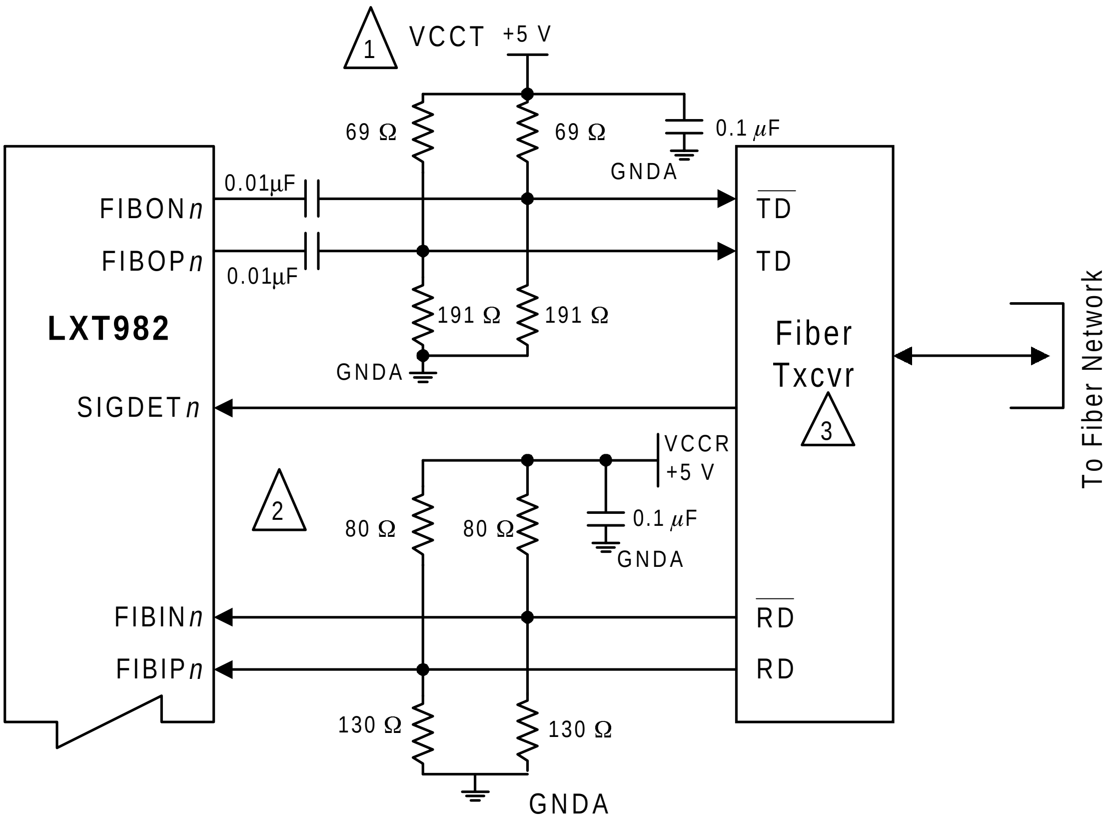


Figure 10: Typical Fiber Port Interface

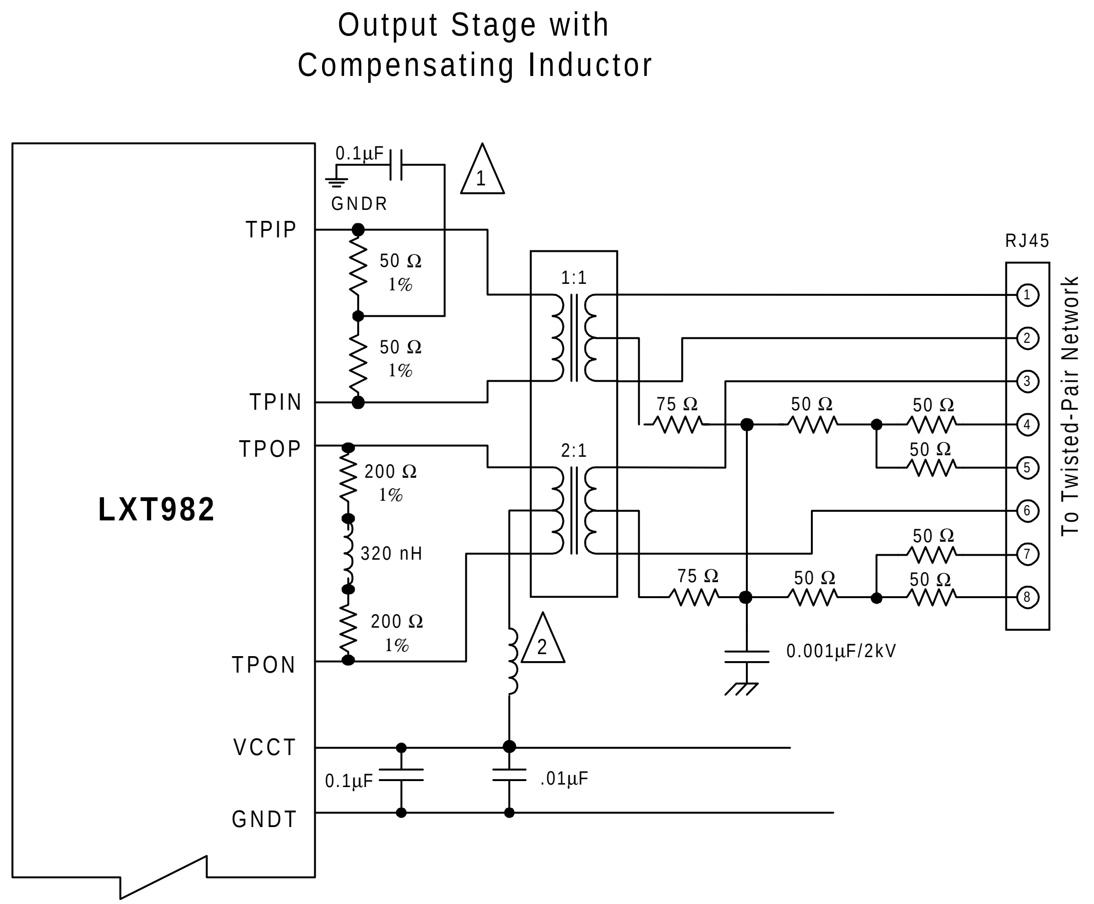


1. Suggested supply layout for fiber-only applications. In combination twisted-pair and fiber applications, use VCCD/GNDD.

2. If the Fiber Interface is not used, FIBIN, FIBIP, FIBON, FIBOP and SIGDET may be left unconnected.

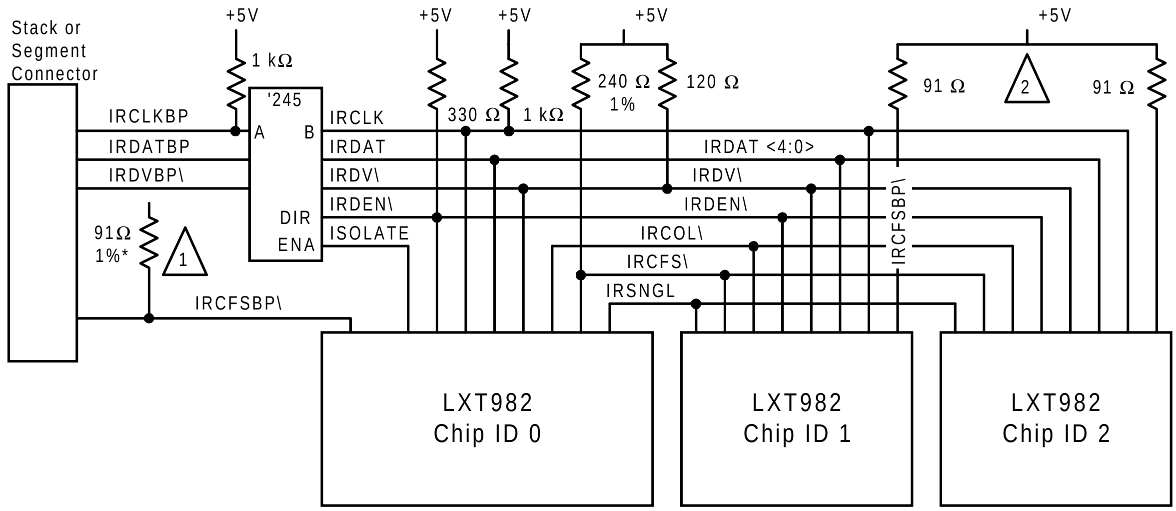
3. Refer to fiber transceiver manufacturers recommendations for termination circuitry. Suitable fiber transceivers include the HFBR-5103 and HFBR-5105.

Figure 11: Typical Twisted-Pair Port Interface



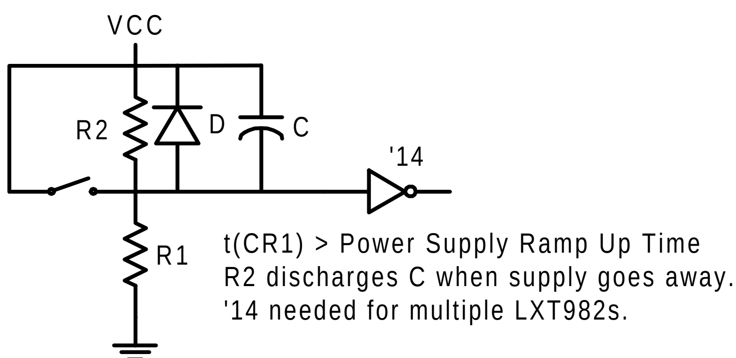
1. Receiver common mode bypass cap may improve BER performance in systems with noisy power supplies.
2. A single ferrite bead may be used to supply center tap current to all 4 ports.

Figure 12: Typical IRB Implementation



1. In stacked configurations, all devices with $\overline{\text{FFS}}$ = Low are tied together at $\overline{\text{IR10CFSBP}}$. The entire stack must be pulled up by only one resistor per signal. Pull-up resistors are installed in the base board only.
2. All devices with $\overline{\text{FPS}}$ = High require individual pull-up resistors at $\overline{\text{IRCFSBP}}$. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

Figure 13: Typical Reset Circuit



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TEST SPECIFICATIONS

NOTE

Tables 14 through 30 and Figures 14 through 23 represent the performance specifications of the LXT982/982A and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Tables 16 through 30 are guaranteed over the recommended operating conditions specified in Table 15

Table 14: Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply voltage		V_{CC}	-0.3	6	V
Operating temperature	Ambient	T_{OPA}	-15	+80	ºC
	Case	T_{OPC}	–	+130	ºC
Storage temperature		T_{ST}	-65	+150	ºC
CAUTION Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.					

Table 15: Operating Conditions

Parameter		Sym	Min	Typ	Max	Units
Recommended supply voltage		V_{CC}	4.75	5.0	5.25	V
		V_{CCV}	4.75	5.0	5.25	V
		V_{CCR}	4.75	5.0	5.25	V
		V_{CCT}	4.75	5.0	5.25	V
Recommended operating temperature	Ambient	T_{OPA}	0	–	70	°C
	Case	T_{OPC}	0	–	115	°C
Power consumption	100BASE-TX, 4 ports active	P_C	–	–	3.5	W
	100BASE-FX, 4 ports active	P_C	–	–	3.0	W

Table 16: Input Clock Requirements

Parameter[1]	Min	Typ[2]	Max	Units
Frequency	–	25	–	MHz
Frequency Tolerance	–	–	±100	ppm
Duty Cycle	40	–	60	%

1. This table lists requirements which apply to the external clock supplied to the LXT982, not to LXT982 test specifications.
2. Typical values are at 25°C and are for design aid only. Not guaranteed and not subject to production testing.

Table 17: I/O Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	TTL inputs
		–	–	30	% V_{CC}	CMOS inputs [2]
		–	–	1.0	V	Schmitt triggers [3]
Input High voltage	V_{IH}	2.0	–	–	V	TTL inputs
		70	–	–	% V_{CC}	CMOS inputs [2]
		V_{CC}-1.0	–	–	V	Schmitt triggers [3]
Hysteresis voltage	–	1.0	–	–	V	Schmitt triggers [3]
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Low voltage (LED)	V_{OLL}	–	–	1.0	V	I_{OLL} = 10 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Input Low current	I_{IL}	-100	–	–	µA	–
Input High current	I_{IH}	–	–	100	µA	–
Output rise / fall time	–	–	3	10	ns	C_L = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 18 for IRB I/O characteristics.
3. Applies to RESET and CLK25 pins only.

Table 18: 100 Mbps IRB Electrical Characteristics

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage		V_{OL}	–	.3	.7	V	R_L = 330 Ω
Output rise or fall time		T_{RF}	–	4	10	ns	C_L = 15 pF
Input High voltage		V_{IH}	V_{CC} - 2.0	–	–	V	CMOS inputs
			V_{CC} - 1.0	–	–	V	IR100CLK (Schmitt trigger)
Input Low voltage		V_{IL}	–	–	2.0	V	CMOS inputs
			–	–	1.0	V	IR100CLK (Schmitt trigger)
Hysteresis voltage		–	1.0	–	–	V	IR100CLK (Schmitt trigger)
$\overline{IRCFS}$ current	single drive	–	7.0	–	9.0	mA	R_L = 240Ω
	collision	–	–	–	20.5	mA	R_L = 240Ω
$\overline{IRCFSBP}$ current	single drive	–	20.0	–	25.0	mA	R_L = 91Ω[2]
	collision	–	–	–	55.0	mA	R_L = 91Ω[2]
$\overline{IRCFSBP}$ voltage	single drive	–	3.4	–	4.35	V	–
	collision	–	1.4	–	1.9	V	–

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

Table 19: 100BASE-TX Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage (single ended)	V_P	0.95	1.0	1.05	V	Note 2
Signal amplitude symmetry	–	98	–	102	%	Note 2
Signal rise/fall time	T_{RF}	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	T_{RFS}	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 8 ns pulse width at 50% of pulse peak,
Overshoot	V_O	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at line side of transformer, line replaced by 100Ω (± 1%) resistor.

Table 20: 100BASE-FX Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	V_{OP}	0.6	–	1.0	V	–
Signal rise/fall time	T_{RF}	–	–	1.6	ns	10 <-> 90%, 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak differential input voltage	V_{IP}	0.55	–	1.5	V	–
Common mode input range	V_{CMIR}	2.25	–	V_{CC} - 0.5	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 14: 100 Mbps Port-to-Port Delay Timing

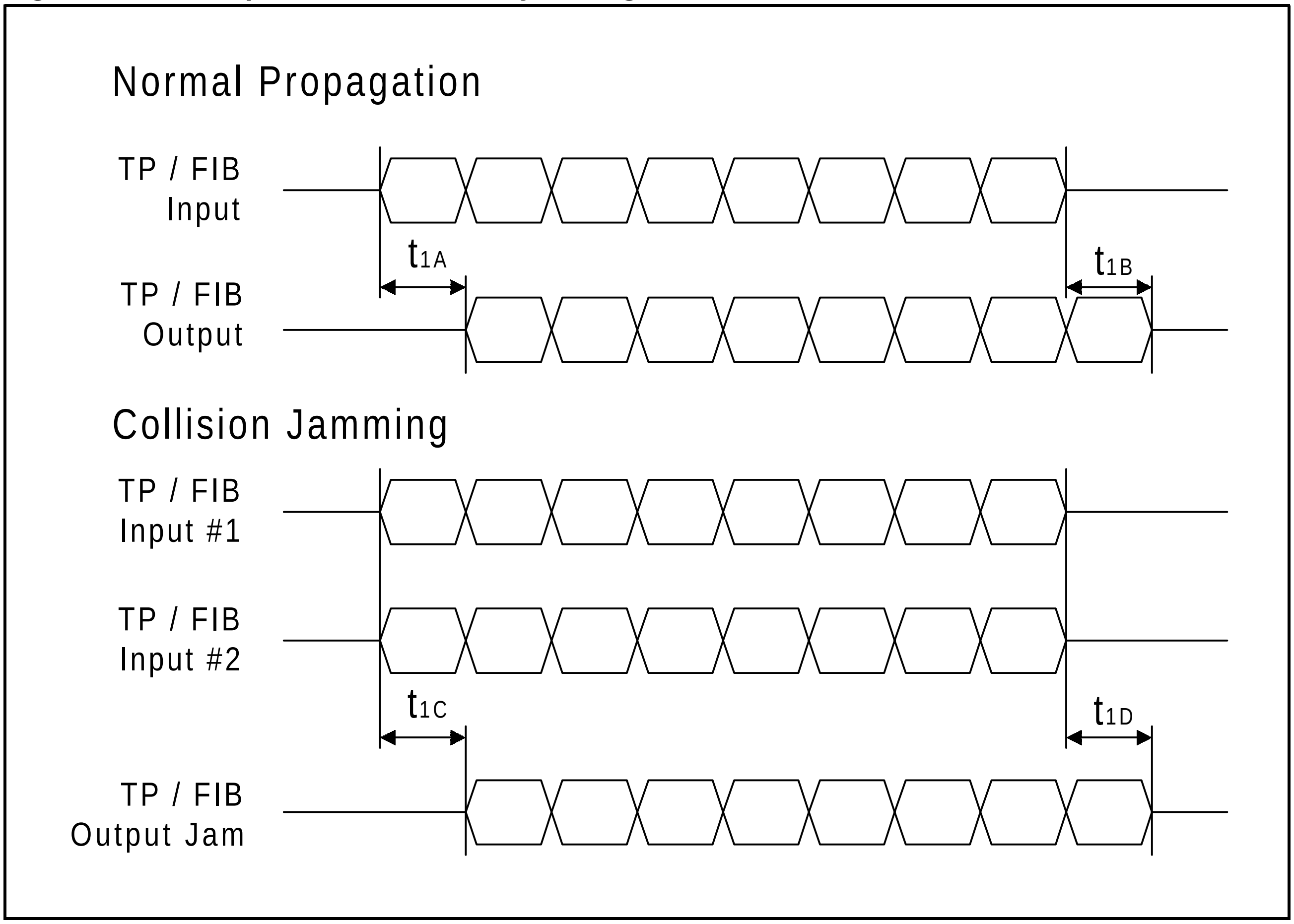


Table 21: 100 Mbps Port-to-Port Delay Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, start of transmission	t1A	–	–	46	BT	–
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, end of transmission	t1B	–	–	46	BT	–
TPIP/N or FIBIP/N collision to TPOP/N or FIBOP/N, start of jam	t1C	–	–	46	BT	–
TPIP/N or FIBIP/N idle to TPOP/N or FIBOP/N, end of jam	t1D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 15: 100BASE-TX Transmit Timing - PHY Mode MII

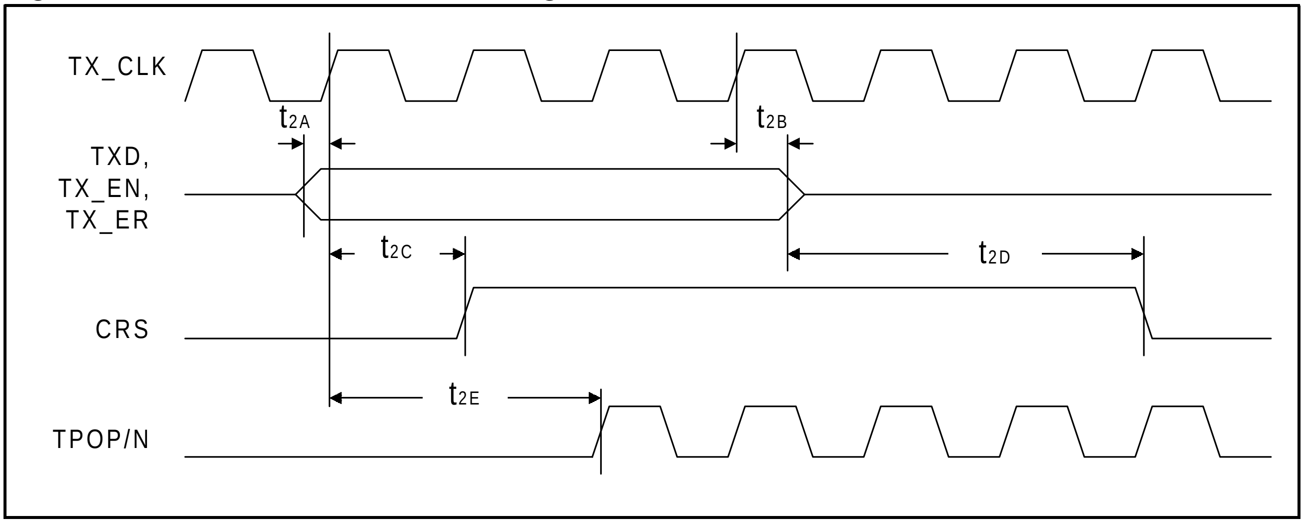


Table 22: 100BASE-TX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t2A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t2C	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t2D	0	–	16	BT	–
TX_EN sampled to TPOP/N active (Tx latency)	t2E	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 16: 100BASE-TX Receive Timing - PHY Mode MII

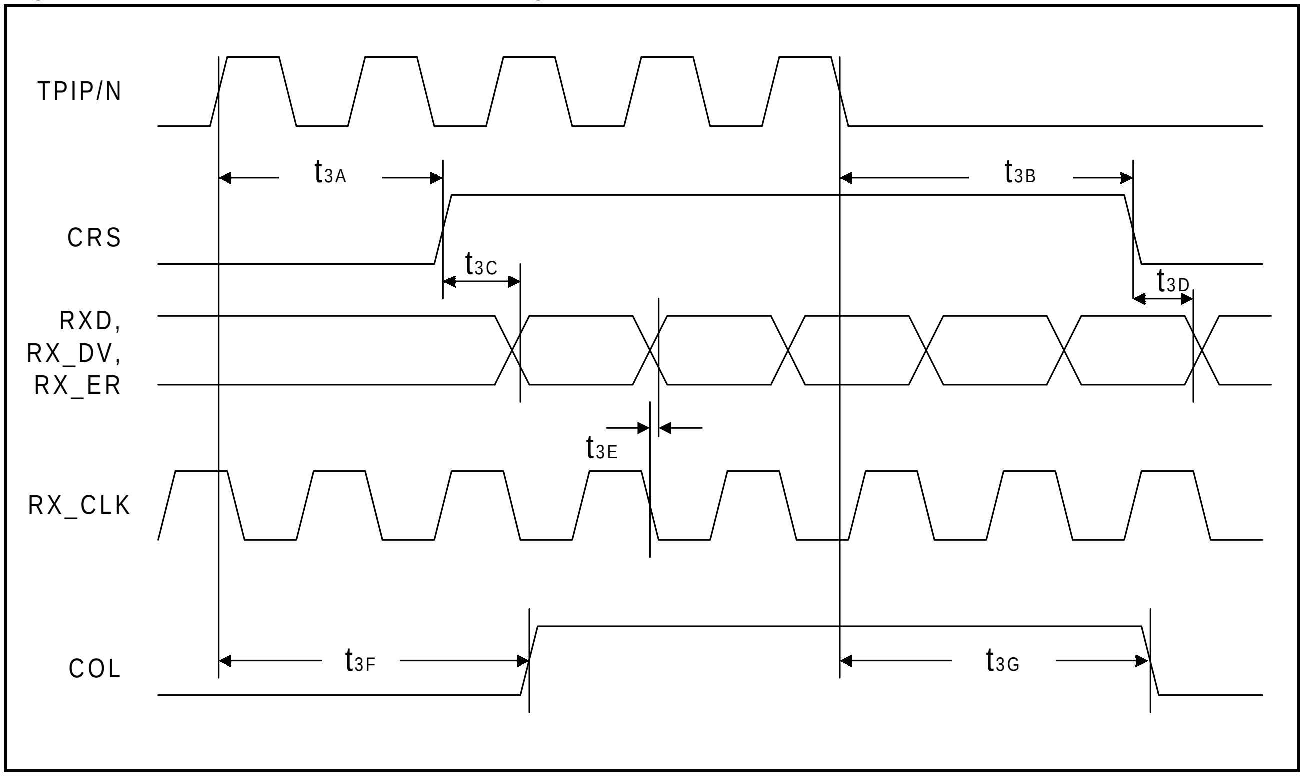


Table 23: 100BASE-TX Receive Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to CRS asserted	t3A	–	–	46	BT	–
TPIP/N quiet to CRS de-asserted	t3B	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t3C	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t3D	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t3E	–	–	10	ns	–
TPIP/N in to COL asserted	t3F	–	–	46	BT	–
TPIP/N quiet to COL de-asserted	t3G	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 17: 100BASE-TX Transmit Timing - MAC Mode MII

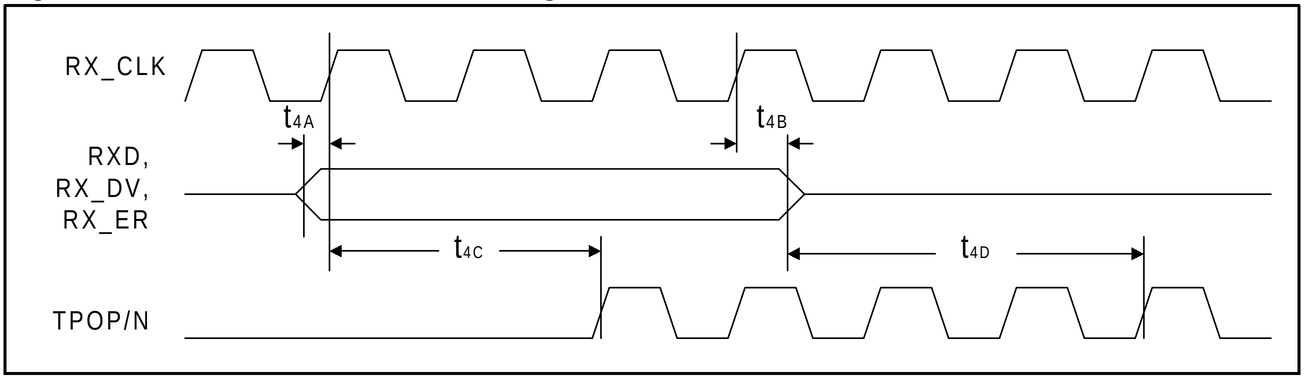


Table 24: 100BASE-TX Transmit Timing Parameters - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t4A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t4B	5	–	–	ns	–
RXD sampled to TPO asserted	t4C	–	–	46	BT	–
RXD sampled to TPO de-asserted	t4D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 18: 100BASE-TX Receive Timing - MAC Mode MII

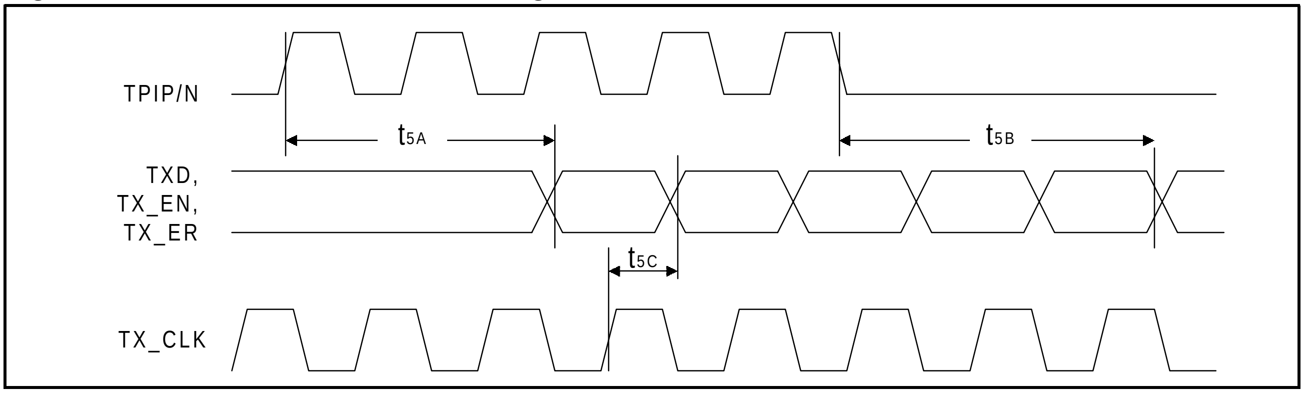


Table 25: 100BASE-TX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to TXD, TX_EN, TX_ER	t5A	–	–	46	BT	–
TPIP/N quiet to TXD de-asserted	t5B	13	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t5C	0	–	25	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 19: 100BASE-FX Transmit Timing - PHY Mode MII

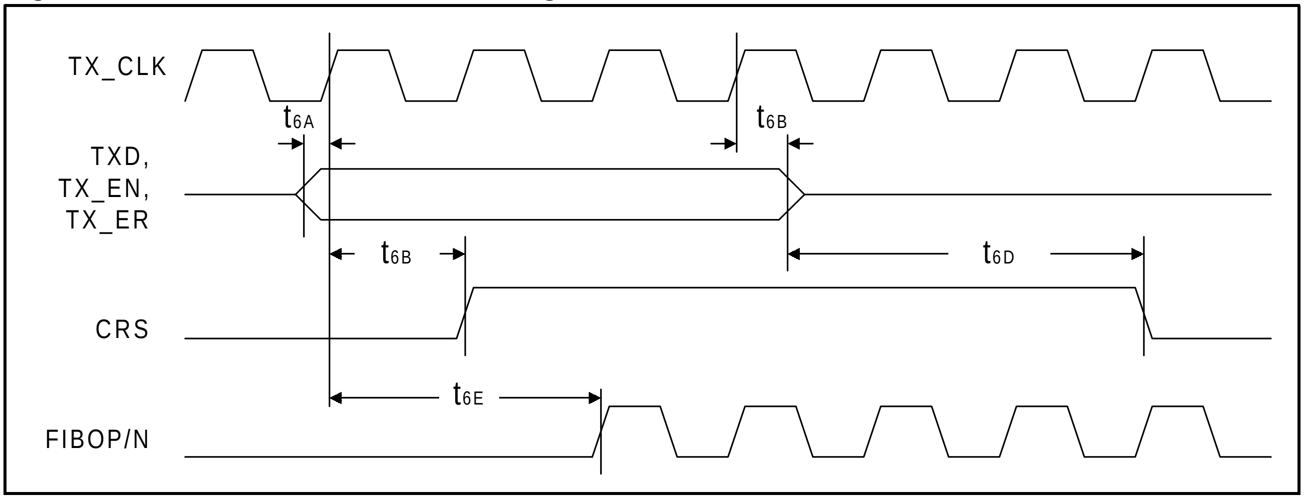


Table 26: 100BASE-FX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t6A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t6B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t6C	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t6D	0	–	16	BT	–
TX_EN sampled to FIBOP/N out (Tx latency)	t6E	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 20: 100BASE-FX Receive Timing - PHY Mode MII

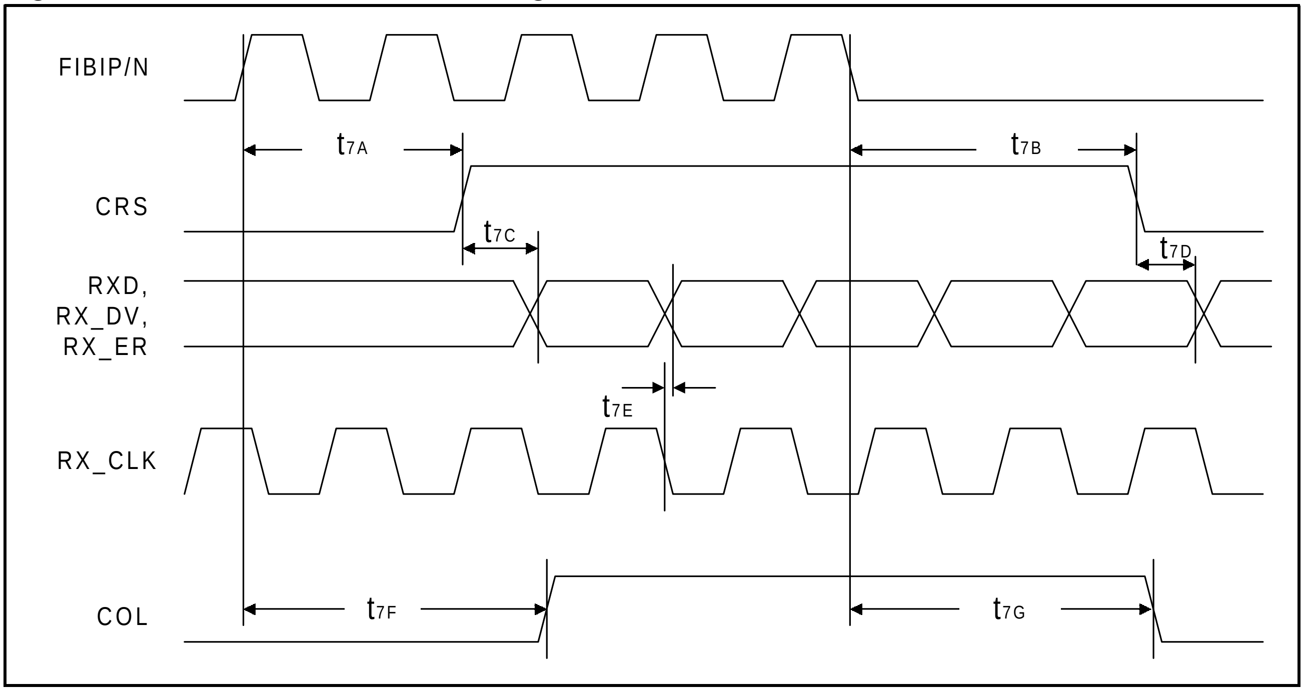


Table 27: 100BASE-FX Receive Timing - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
FIBIP/N in to CRS asserted	t7A	–	–	46	BT	–
FIBIP/N quiet to CRS de-asserted	t7B	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t7C	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t7D	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t7E	–	–	10	ns	–
FIBIP/N in to COL asserted	t7F	–	–	46	BT	–
FIBIP/N quiet to COL de-asserted	t7G	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 21: 100BASE-FX Transmit Timing - MAC Mode MII

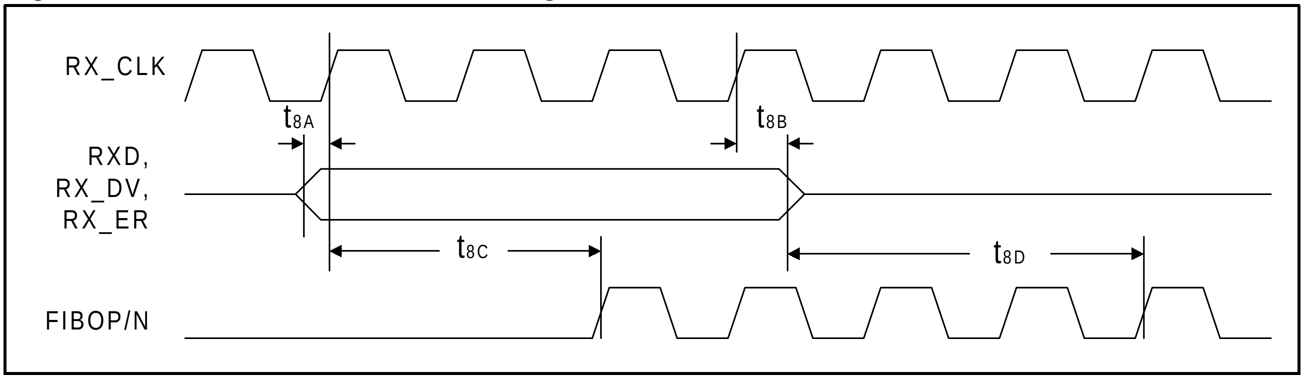


Table 28: 100BASE-FX Transmit Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t8A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t8B	5	–	–	ns	–
RXD sampled to FIBOP/N asserted	t8C	–	–	46	BT	–
RXD sampled to FIBOP/N de-asserted	t8D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 22: 100BASE-FX Receive Timing - MAC Mode MII

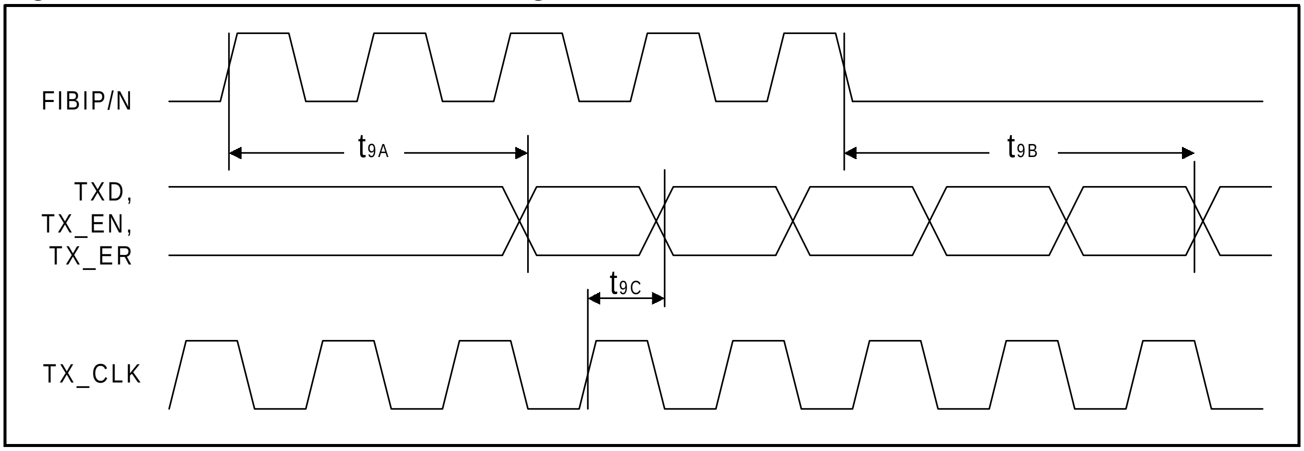


Table 29: 100BASE-FX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
FIBIP/N in to TXD, TX_EN, TX_ER	t9A	–	–	46	BT	–
FIBIP/N quiet to TXD de-asserted	t9B	–	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t9C	0	–	25	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 23: 100 Mbps IRB Timing

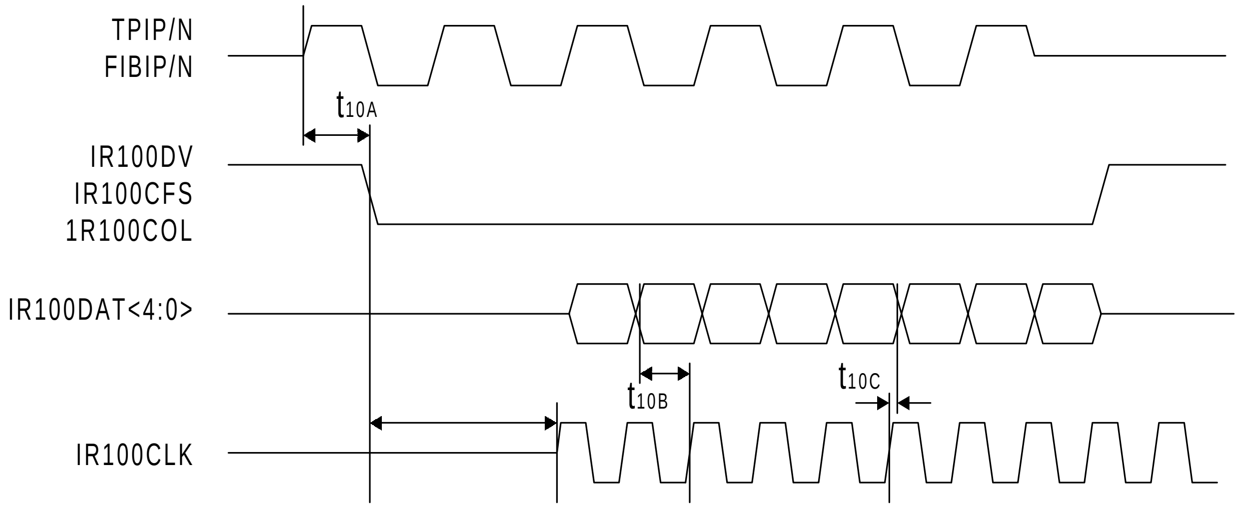


Table 30: 100 Mbps IRB Timing Parameters[1]

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N or FIBP/N to $\overline{\text{IRDV}}$ Low	t10A	18	24	30	BT	–
IRDAT to IRCLK setup time.	t10B	–	10	–	ns	–
IRDAT to IRCLK hold time.	t10C	–	0	–	ns	–

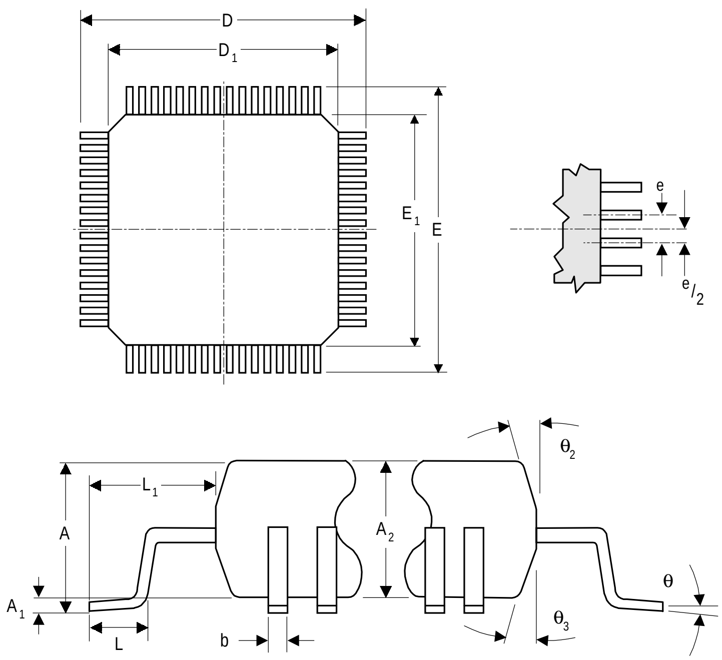
1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

MECHANICAL SPECIFICATIONS

Figure 24: Package Specifications

208-Pin Plastic Quad Flat Package

- Part Numbers
  - LXT982QC
  - LXT982AHC
- Commercial Temperature Range (0°C to 70°C)



Dim	Millimeters	
	Min	**Max**
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

REVISION HISTORY

This Revision History assumes a baseline of Revision 1.0.

Table 31: Changes from Rev. 1.1 to Rev. 1.2 (02/99)

Section	Page	Change	Description
General Description	1	Add	To the first paragraph, add the following sentence: “This data sheet applies to all LXT982 products (LXT982, LXT982A, and any subsequent variants), except as specifically noted.”
Signal Descriptions	5-10	Modify Add	Editorial clean-up: re-order, clarify information in “Type” column.
IRB Signal Description	8	Modify	For $\overline{IRCFSBP}$ signal, change pull-up resistor value from 82Ω to 91Ω .
Power Supply Signal Desc.	9		Rewrite GND desc.: “For LXT982, Chip ID 1 is Pin 72; Chip ID 2 is Pin 73. If using an LXT982 device in an LXT981-based design, these pins do not have to be tied to ground.”
Misc. Signal Desc	10	Add	Add to FPS description: “If using an LXT982 device in an LXT981-based design, $\overline{FPS}$ is analogous to Chip ID 0 on the LXT981.”
LED Operation Table 10	14	Modify	Correct and re-write Mode 2 and Mode 3 Indications.
IRB Signal Details Table 12	15		For $\overline{IRCFSBP}$ signal, change pull-up resistor value from 82Ω to 91Ω .
Typ. IRB Implementation Fig. 12	26		Correct Figure 12 to include $\overline{IRCFSBP}$ signals for Chip ID 1 and 2. Add notes. For $\overline{IRCFSBP}$ signal, change pull-up resistor value from 82Ω to 91Ω . Correct Notes 1,2: ChipID = 0 should read “$\overline{FFS}$ = Low”; ChipID $\neq$ 0 should read “$\overline{FPS}$ = High”.
100 Mbps IRB Elect. Char.	28		For $\overline{IRCFSBP}$ signal, change pull-up resistor value from 82Ω to 91Ω .
Backpage	44		Update.

Table 32: Changes from Rev. 1.0 to Rev. 1.1 (12/98)

Section	Page #	Change	Description
Cover Page Subtitle	1	Delete	Remove “and 10BASE-T Applications” from subtitle.
Features		Modify	Change 0 - 70° temperature range to “Case temperature range: 0 - 115°”.
100M IRB Sigs Table 6	8	Add	Add “Schmitt MOS PU” to IR100SNGL, IR100COL, IR100DV, IR100DAT<0:4>.
			Add “PD” to IR100CLK.
			Add a 1 kΩ pull-up resistor to IRCLK line.
		Modify	Rewrite and expand signal descriptions for $\overline{IRDV}$, $\overline{IRCFSBP}$, and $\overline{IRCFSBP}$.

Section	Page #	Change	Description
Power Supply and Indication Signals Table 8	9	Modify	Replace “-” marks under “Type” column with appropriate “Analog” and “Digital” indications.
	10		Change external resistor value from 22 KΩ to 22.1 kΩ.
Pin Assignments/ Misc. Signals Table 9		Delete	Delete pins 182, 184, 186 & 188 from the No Connect listing. These pins are correctly identified as VCC in Figure 1 and in Table 8.
		Add	Add Pins 48 and 100 to “NC” indicated listing.
Remote Fault Reporting	13	Delete	Remove “ . . . sets the associated interrupts . . .” phrase.
Repeater Operation		Add	The LXT982 partitions any port that participates in excess of . . .”one collision that is approximately 575.2 µs long.”
Bias Current	14	Modify	Change external resistor value from 22 KΩ to 22.1 kΩ .
IRB Bus Pull-ups	15	Add	Add IRCLK to listing of IRB signals requiring pull-up resistor.
IRB Signals Table 12		Modify	Change “No” to “Yes in Pull-up column for IRCLK.
			$\overline{\text{IRCFSBP}}$ Pull-up Resister = 82Ω
MII Port Timing	17-18	Modify	Rewrite to clarify MII Port Timing Considerations section.
Figure 6			Clarify MII-to-MII, PHY-to-MAC prop. delay graphics.
General Design Guidelines Entire Section	19-20		Update section, removing references to separate analog & digital ground planes and associated ferrite bead filter.
RBIAS Pin	20	Modify	RBIAS pin: Change external resistor value from 22 KΩ to 22.1 kΩ.
Magnetics Information Table 13	21		Update Suggested Magnetics List and Magnetics Specifications. Move differential to CMR from “Min” to “Max” column; indicate as -40 and -35 for .1 to 60 MHz and 60 to 100 MHz, respectively.
Table 13 (former)	21	Delete	Delete “Suggested Magnetics List”
Power and Gnd Connections Figure 9	23	Modify	Update per changes to General Design Guidelines section, removing elements showing separate analog & digital ground planes and associated ferrite bead filter.
Twisted-Pair I/F Figure 11	25	Correct	Reverse RJ45 connections to show repeater I/F, not NIC. Should be: TPOP = 3, TPON = 6 TPIP = 1, TPIN = 2
Typical IRB Implementation Figure 12	26	Add	Add two 1 kΩ pull-up resistors to IRCLK signal line, on either side of the ‘245 buffer.
		Modify	$\overline{\text{IRCFSBP}}$ Pull-up Resistor = 82Ω

Section	Page #	Change	Description
Test Specifications	27	Modify Delete	Re-write “NOTE”; Delete “Over Recommended Range” from all Table titles (17-30).
Absolute Max Ratings Table 14		Modify	Increase Max Case Temp to 130.
			Revise Warning to address immediate EOS damage.
100 Mbps IRB Elect. Char.	29		$\overline{\text{IRCFSBP}}$ current Test Conditions RL value = 82Ω
Test Spec Tables 21 - 30	30 - 38	Modify	Clarify definition of Bit times (BT) for both 10 and 100BASE-TX. This appears as a note to the “Unit” column.
			Change Timing Parameter Symbol convention.
Test Spec Figures 14 - 23			Modify figures to correspond to Timing Parameter convention changes.
100 IRB Timing Table 30 Figure 23	38	Delete Modify	Delete IR100ENA asserted to TPOP/N or FIBOP/N active and corresponding figure element.
			TPIP/N or FIBP/N to IR100DV Low: change Min, Typ, and Max values.
Throughout	All	Modify	Replace “module” with “board” where appropriate.
All			Light editing throughout.
Backpage	42		Update.

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NOTES

NOTES

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Revision	Date	Status
1.2	02/99	Document changes due to A8 design revisions.
1.1	12/98	Additions to Signal Descriptions; correct Pin Assignments; correct Twisted-Pair I/F figure; change Max. Case temperature.
1.0	02/98	Initial Release, Preliminary Information.

This product is covered by one or more of the following patents. Additional patents pending.
The products listed in this publication are covered by one or more of the following patents. Additional patents pending.
5,008,637; 5,028,888; 5,057,794; 5,059,924; 5,068,628; 5,077,529; 5,084,866; 5,148,427; 5,153,875; 5,157,690; 5,159,291; 5,162,746; 5,166,635; 5,181,228; 5,204,880; 5,249,183; 5,257,286; 5,267,269; 5,267,746; 5,461,661; 5,493,243; 5,534,863; 5,574,726; 5,581,585; 5,608,341; 5,671,249; 5,666,129; 5,701,099

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