Document Title

Multi-Chip Package MEMORY

128M Bit (16Mx8) Nand Flash Memory / 64M Bit (4Mx16) U*t*RAM *2

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft.	May 29, 2002	Preliminary
0.1	Revise - Change U*t*RAM output load(C_L) from 50pF to 80pF	July 4, 2002	Preliminary
0.2	Revise - Change U*t*RAM Operating Current(Icc1) from 5mA to 7mA	October 21, 2002	Preliminary
1.0	Finalize	January 10, 2003	Final

Multi-Chip Package MEMORY

128M Bit (16Mx8) Nand Flash Memory / 64M Bit (4Mx16) UtRAM *2

FEATURES

- Power Supply Voltage
  - Flash : 2.7 ~ 3.6V
  - U*t*RAM : 2.3 ~ 2.7V(In Battery Backup Mode, Max. Vcc = 3.1V)
- Organization
  - Flash : (16M + 512K)bit x 8bit
  - U*t*RAM : 4M x 16 bit(Each component)
- Access Time
  - Flash : Random Access : 10us(Max.),
    Serial Page Access : 50ns(Min.)
  - U*t*RAM : 80ns
- Power Consumption (typical value)
  - Flash Read Current : 10 mA(@20MHz)
    Program/Erase Current : 10 mA
    Standby Current : 10 μA
  - U*t*RAM Operating Current : 35mA
    Standby Current : 80μA(per 1 U*t*RAM)
- Flash Automatic Program and Erase
  Page Program : (512 + 16)Byte
  Block Erase : (16K + 512)Byte
- Flash Fast Write Cycle Time
  Program time : 200us(Typ.)
  Block Erase Time : 2ms(Typ.)
- U*t*RAM Support 16Mb Partial Refresh
- Flash Endurance : 100,000 Program/Erase Cycles Minimum
- Flash Data Retention : 10 years
- Operating Temperature : -25°C ~ 85°C
- Package : 111 - ball TBGA Type - 10 x 11mm, 0.8 mm pitch

GENERAL DESCRIPTION

The KAE00C400M is a Multi Chip Package Memory which combines 128Mbit Nand Flash and two 64Mbit Unit Transistor CMOS RAM.

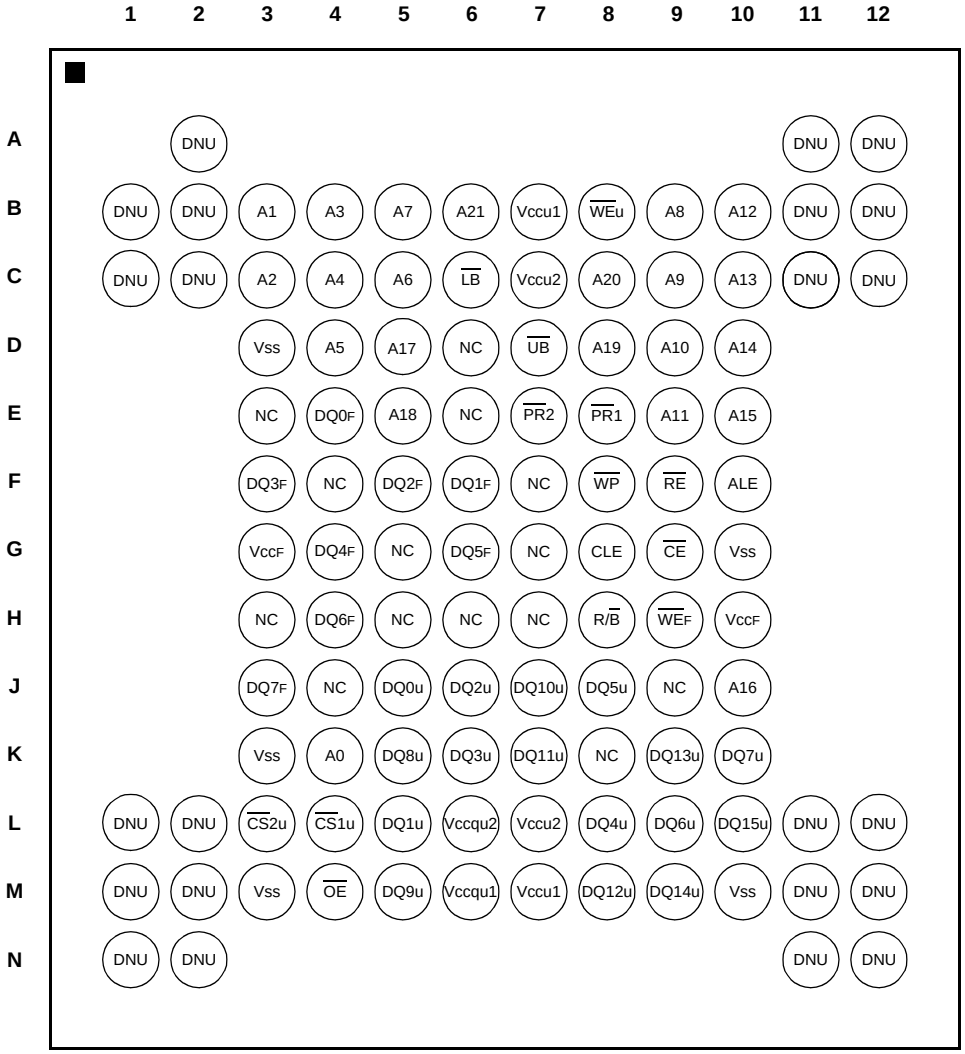
128Mbit Flash memory is organized as 16M x8 bit and 64Mbit U*t*RAM is organized as 4M x16 bit. In 128Mb NAND Flash a 528-byte page program can be typically achieved within 200us and an 16K-byte block erase can be typically achieved within 2ms. In serial read operation, a byte can be read by 50ns. Even the write-intensive systems can take advantage of the FLASH′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC.

The 64Mbit U*t*RAM is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports partial refresh mode for low standby current.

The KAE00C400M is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption.

This device is available in 111-ball TBGA Type.

PIN CONFIGURATION



111-TBGA: Top View (Ball Down)

PIN DESCRIPTION

Ball Name	Description	Ball Name	Description
A_0 to A_{21}	Address Input Balls (U*t*RAM)	CLE	Command Latch Enable (Flash Memory)
DQ_{0F} to DQ_{7F}	Command, Address, Data Input/Output Balls (Flash Memory)	R/$\overline{B}$	Ready/Busy (Flash Memory)
		$\overline{PR}$1	Partial Refresh (U*t*RAM1)
DQ_{0u} to DQ_{15u}	Data Input/Output Balls (U*t*RAM)	$\overline{PR}$2	Partial Refresh (U*t*RAM2)
$\overline{WP}$	Write Protection (Flash Memory)	$\overline{CE}$	Chip Enable (Flash Memory)
V_{CCF}	Power Supply (Flash Memory)	$\overline{CS}$1u	Chip Select (U*t*RAM1)
Vccu1	Power Supply (U*t*RAM1)	$\overline{CS}$2u	Chip Select (U*t*RAM2)
Vccu2	Power Supply (U*t*RAM2)	$\overline{WE}_F$	Write Enable (Flash Memory)
Vccqu1	Data Out Power (U*t*RAM1)	$\overline{WE}_u$	Write Enable (U*t*RAM)
Vccqu2	Data Out Power (U*t*RAM2)	$\overline{OE}$	Output Enable (U*t*RAM)
Vss	Ground (Common)	$\overline{RE}$	Read Enable (Flash Memory)
$\overline{UB}$	Upper Byte Enable (U*t*RAM)	NC	No Connection
$\overline{LB}$	Lower Byte Enable (U*t*RAM)	DNU	Do Not Use
ALE	Address Latch Enable (Flash Memory)		

ORDERING INFORMATION

K A E 00 C 4 0 0 M - T GNN

Samsung
MCP(3 Chip) Memory

Device Type
NAND Flash+U*t*RAM+U*t*RAM

NOR Flash Density , Vcc , Org.
00 : NONE

NAND Flash Density , Vcc , Org.
C : 128Mbit, 3.0V, x8

U*t*RAM Density , Vcc , Org.
4 : 64Mbit + 64Mbit, 2.5V, x16, Partial Refresh

Access Time
G : NAND Flash:50ns
N : U*t*RAM: 80ns
N : U*t*RAM: 80ns

Package
T : TBGA

Version
M : 1st Generation

SDRAM Density , Vcc , Org.
0 : NONE

SRAM Density , Vcc , Org.
0 : NONE

Figure 1. FUNCTIONAL BLOCK DIAGRAM

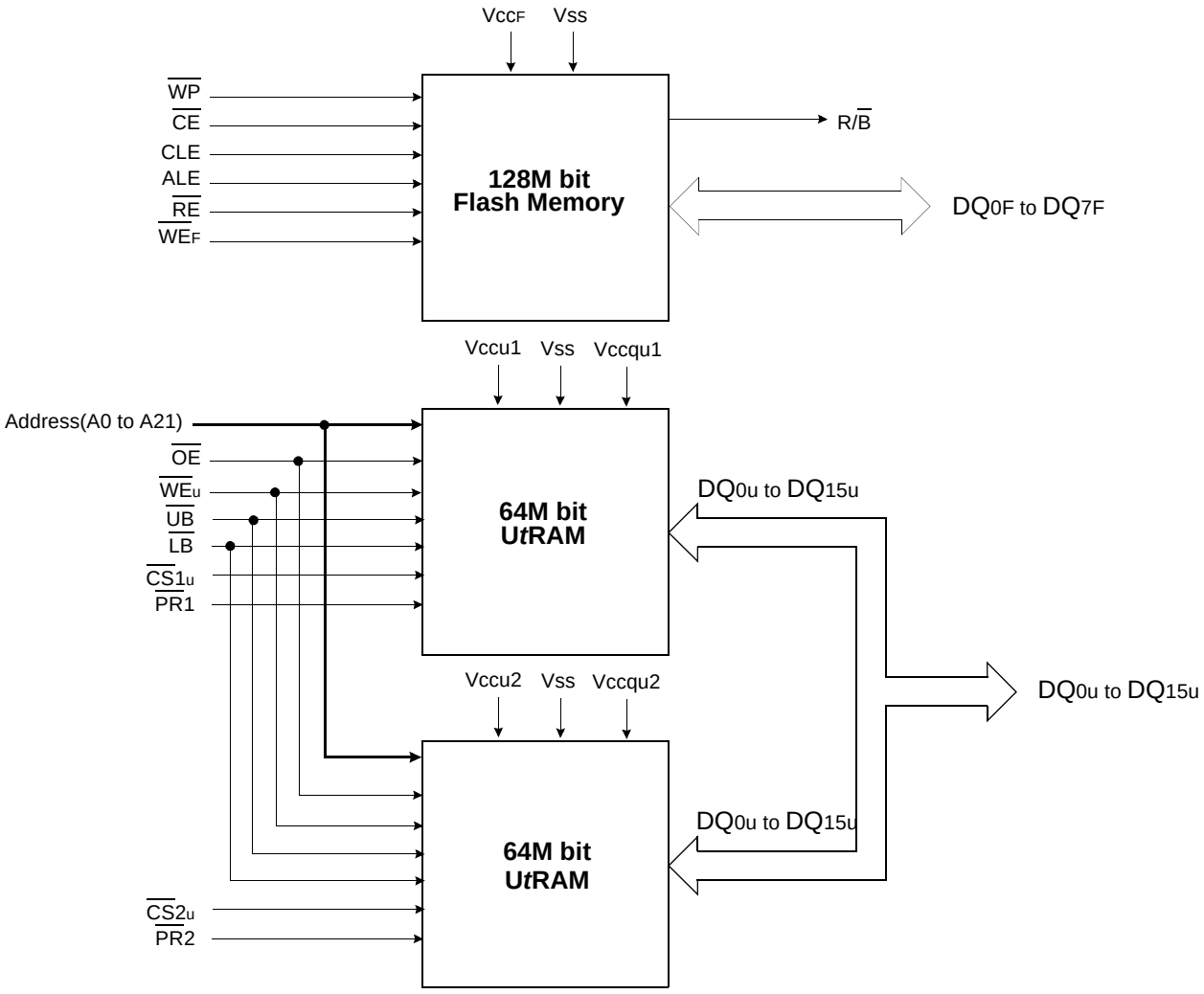
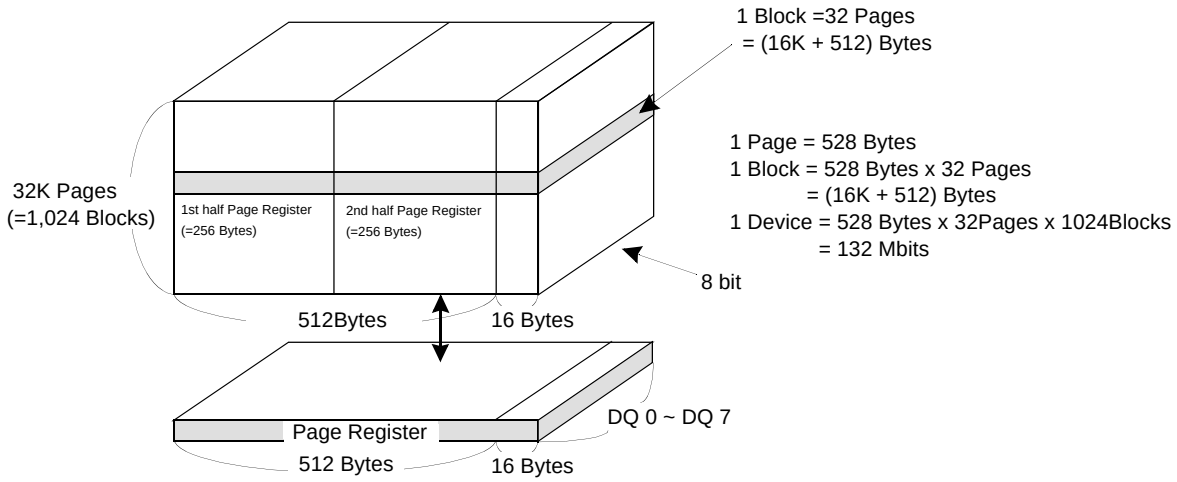


Figure 2. Flash ARRAY ORGANIZATION



	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	*L	**(Page Address)**

NOTE : Column Address : Starting Address of the Register.

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

* A_8 is set to "Low" or "High" by the 00h or 01h Command.

* L must be set to "Low"

NAND FLASH PRODUCT INTRODUCTION

The Flash Memory is a 132Mbit(138,412,032 bit) memory organized as 32,768 rows(pages) by 528 columns. Spare 16 columns are located in 512 to 527 column address. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected like NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by one NAND structures, totaling 8448 NAND structures of 16 cells. The array organization is shown in Figure 2. Program and read operations are executed on a page basis, while erase operation is executed on a block basis. The memory array consists of 1024 blocks, and a block is separately erasable by 16K-byte unit. It indicates that the bit by bit erase operation is prohibited on the Flash Memory.

The Flash Memory has addresses multiplexed with 8 I/O′s. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except Page Program command and Block Erase command which require two cycles: one cycle for setup and another for execution. The 16M byte physical space requires 24 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following required command input. In Block Erase operation, however, only two row address cycles are used. Device operations are selected by writing specific commands into command register. Table 1 defines the specific commands of the Flash Memory.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE: 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the start pointer is automatically moved to the 1st half register(00h) on the next cycle.

Table 2. FLASH MEMORY OPERATIONS TABLE

CLE	ALE	$\overline{CE}$	$\overline{WE}_F$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⌐‾_/‾¬	H	X	Read Mode	Command Input
L	H	L	⌐‾_/‾¬	H	X		Address Input(3clock)
H	L	L	⌐‾_/‾¬	H	H	Write Mode	Command Input
L	H	L	⌐‾_/‾¬	H	H		Address Input(3clock)
L	L	L	⌐‾_/‾¬	H	H	Data Input	
L	L	L	H	¬_/¬	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Table 3. U*t*RAM OPERATIONS TABLE

$\overline{CS_{iU}}$2)	$\overline{PR_i}$2)	$\overline{OE}$	$\overline{WE_U}$	$\overline{LB}$	$\overline{UB}$	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	H	X1)	X1)	X1)	X1)	High-Z	High-Z	Deselected	Standby
L	H	X1)	X1)	H	H	High-Z	High-Z	Deselected	Standby
X1)	L	X1)	X1)	X1)	X1)	High-Z	High-Z	Deselected	Partial Refresh
L	H	H	H	L	X1)	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X1)	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X1)	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X1)	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X1)	L	L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)
2. i = 1 or 2.
When $\overline{CS1u}$ is active, $\overline{CS2u}$ must be standby. and when $\overline{CS2u}$ is active, $\overline{CS1u}$ must be standby.

FLASH MEMORY OPERATION

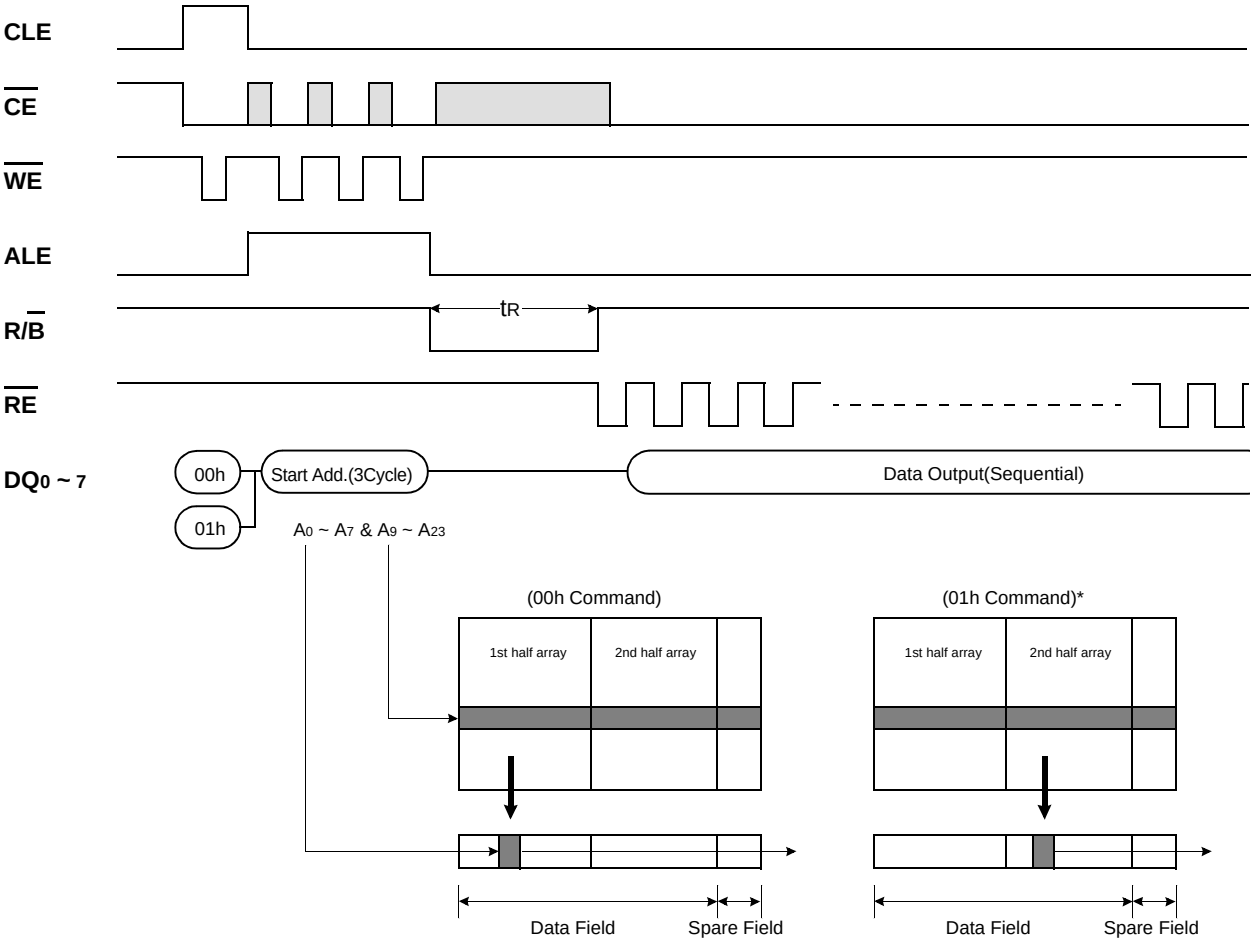
PAGE READ

Upon initial device power up, the device status is initially Read1 command(00h) latched. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operation are available : random read, serial page read. The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out by sequential RE pulse of 50n period cycle. High to low transitions of the RE clock take out the data from the selected column address up to the last column address.

Read1 and Read2 commands determine pointer which selects either main area or spare area. The spare area(512 to 527 bytes) may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of spare area while addresses A_4 to A_7 are ignored. To move the pointer back to the main area, Read1 command(00h/01h) is needed. Figures 3 through 8 show typical sequence and timing for each read operation.

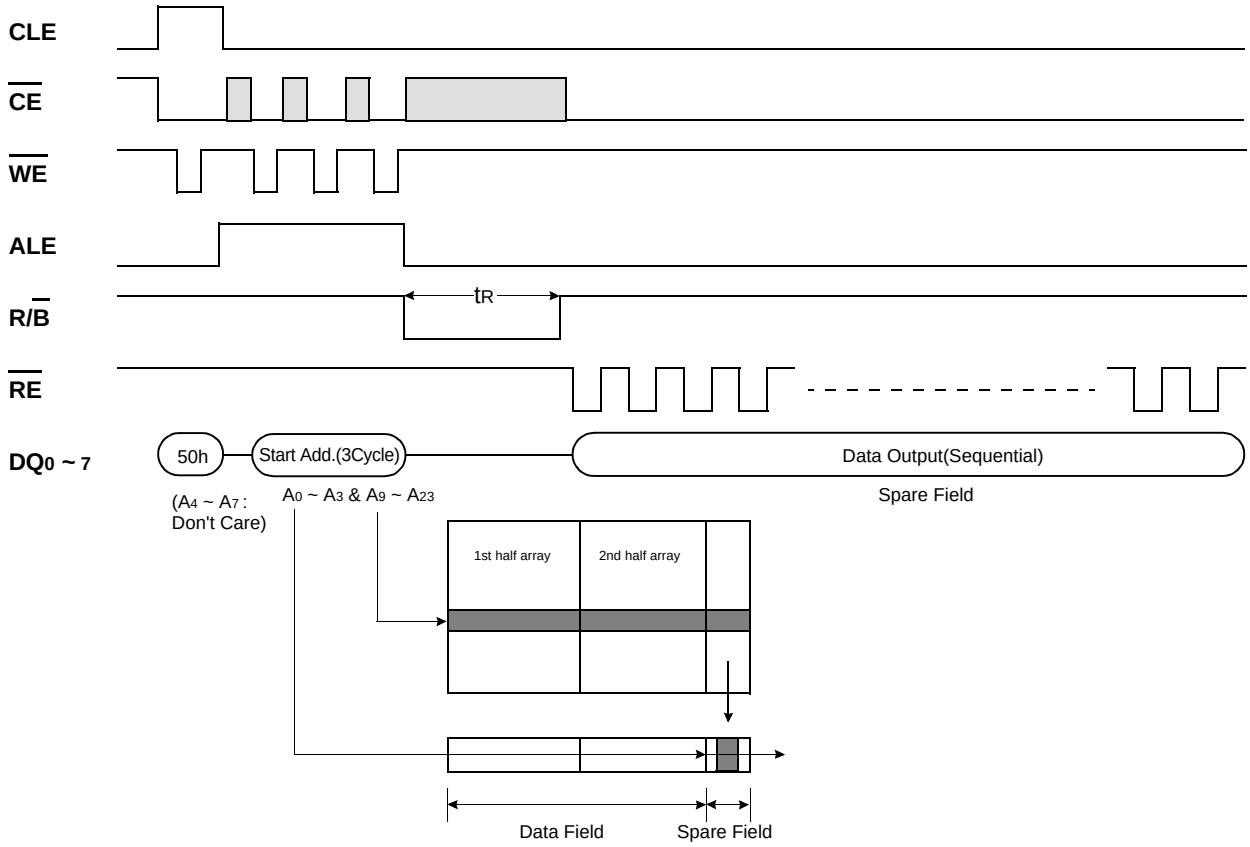
Figure 3,4 details the sequence.

Figure 3. Read1 Operation



* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 4. Read2 Operation

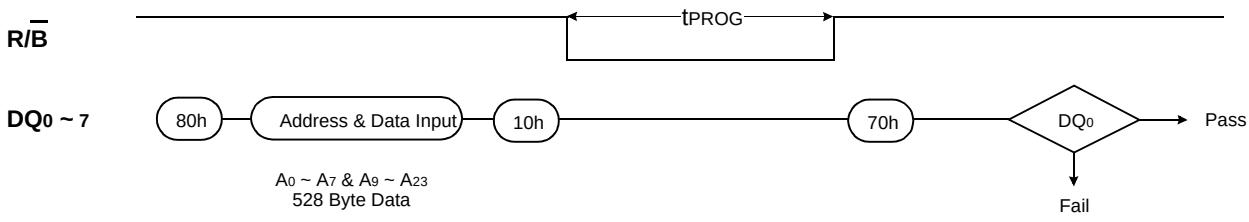


PAGE PROGRAM

The device is programmed basically on a page basis, but it allows multiple partial page program of one byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page program operation within the same page without intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. Page program cycle consists of a serial data loading(up to 528 bytes of data) into the page register, and program of loaded data into the appropriate cell. Serial data loading can start in 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes. Serial data loading is executed by entering the Serial Data Input command(80h) and three cycle address input and then serial data loading. The bytes except those to be programmed need not to be loaded. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering 80h will not initiate program process. The internal write controller automatically executes the algorithms and timings necessary for program and verification, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is completed, the Write Status Bit(I/O 0) may be checked(Figure 5). The internal write verification detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 5 details the sequence.

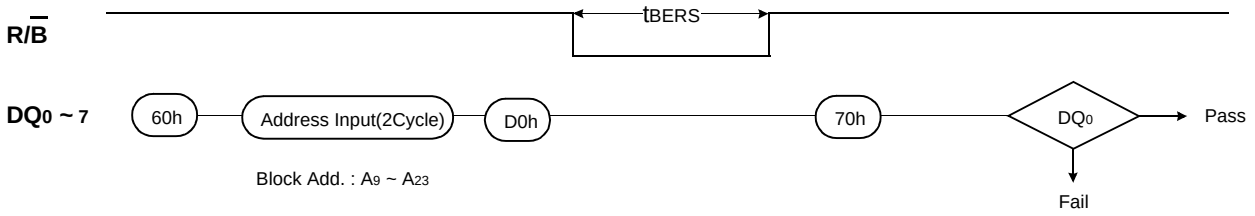
Figure 5. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(16K Bytes) basis. Block Erase is executed by entering Erase Setup command(60h) and 2 cycle block addresses and Erase Confirm command(D0h). Only address A14 to A23 is valid while A9 to A13 is ignored. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise condition. At the rising edge of $\overline{WE}$ after erase confirm command input, internal write controller handles erase and erase-verification. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.
Figure 6 details the sequence.

Figure 6. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to command register, a read cycle takes out the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

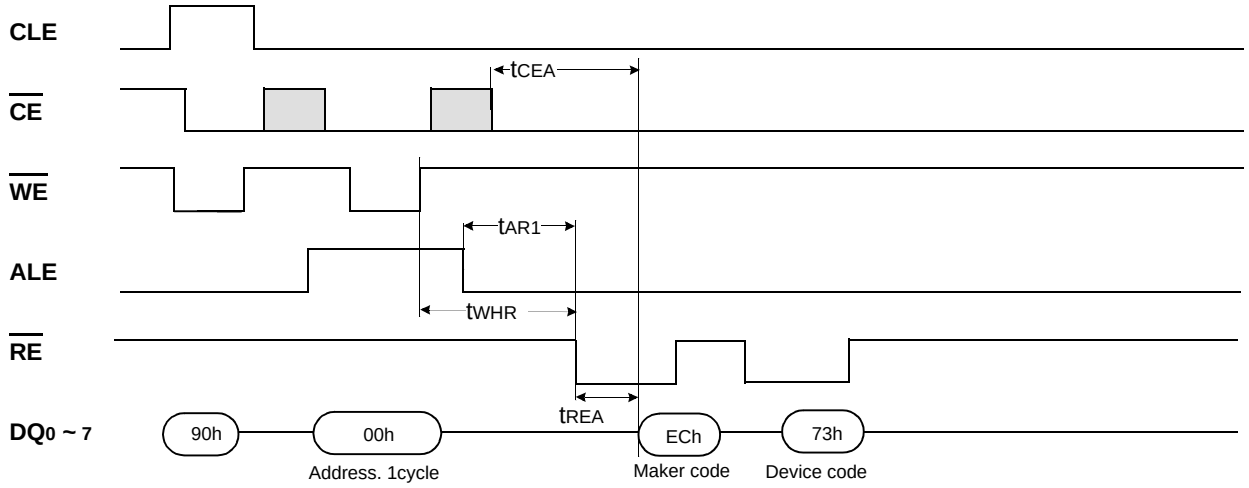
Table4. Read Status Register Definition

DQ #	Status	Definition
DQ_0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
DQ_1	Reserved for Future Use	"0"
DQ_2		"0"
DQ_3		"0"
DQ_4		"0"
DQ_5		"0"
DQ_6	Device Operation	"0" : Busy "1" : Ready
DQ_7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (73h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 7 shows the operation sequence.

Figure 7. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 5 for device status after reset operation. If the device is already in reset state, new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 8 below.

Figure 8. RESET Operation

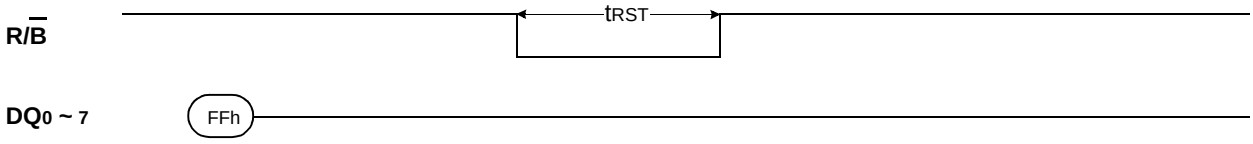


Table5. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 9). Its value can be determined by the following guidance.

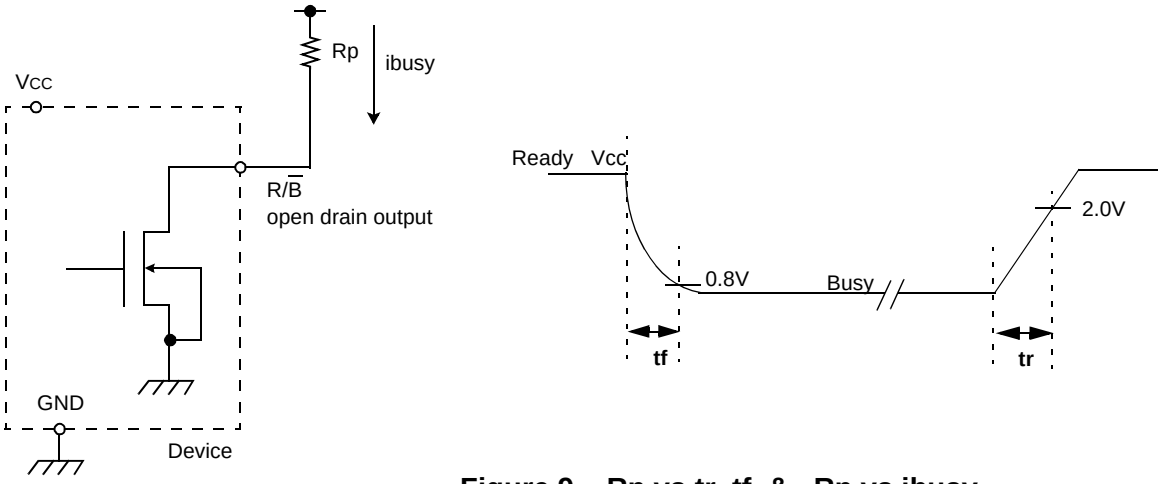
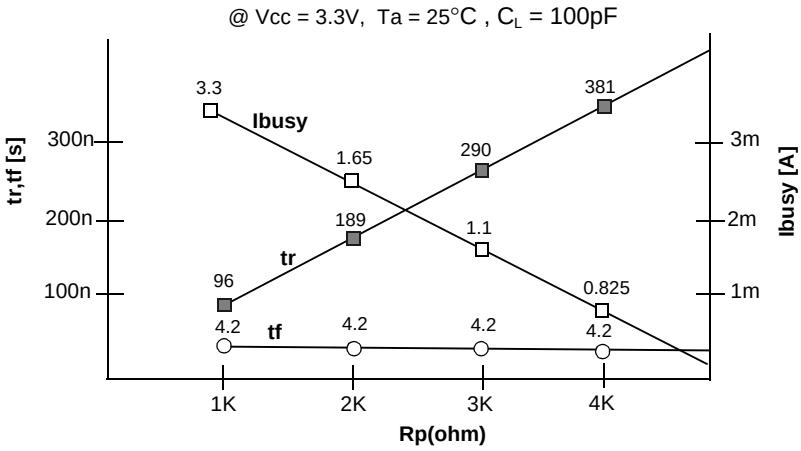


Figure 9. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

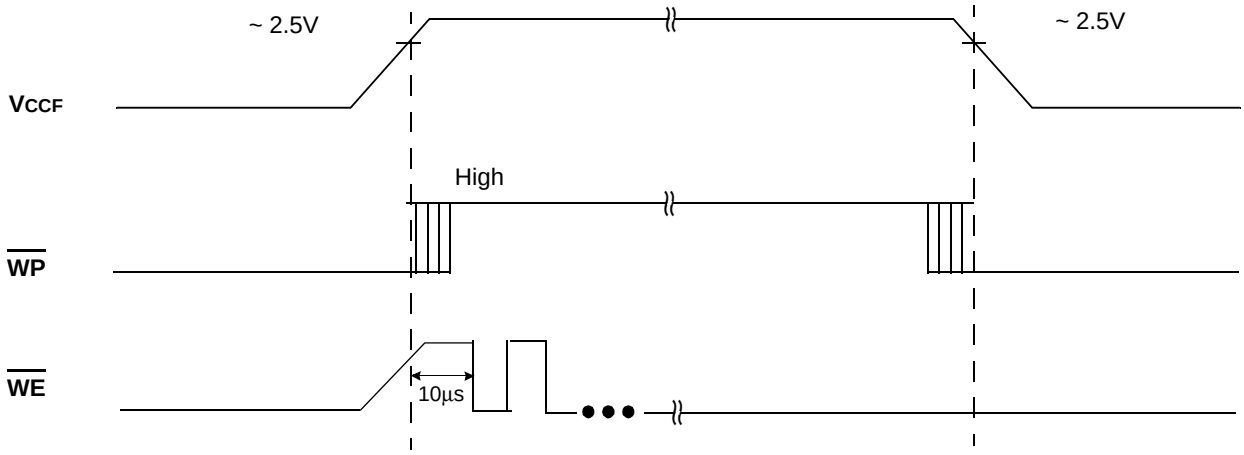
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Powerup sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.3V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 1μs is required before internal circuit gets ready for any command sequences as shown in Figure 10. The two step command sequence for program/erase provides additional software protection.

Figure 10. AC Waveforms for Power Transition



Flash ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN/OUT}$	-0.6 to + 4.6	V
	V_{CC}	-0.6 to + 4.6	
Temperature Under Bias	T_{BIAS}	-40 to +125	°C
Operating Temperature	T_A	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE:

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC},+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

U*t*RAM ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-25 to 85	°C
Storage temperature	T_{STG}	-65 to 150	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

Flash RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND, T_A=-25 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

U*t*RAM RECOMMENDED DC OPERATING CONDITIONS (T_A=-25 to 85°C, otherwise specified.)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.3	2.5	2.7[1)]	V
Ground	Vss	0	0	0	V

1. In Battery Backup Mode, Max. Vcc = 3.1V

Flash DC AND OPERATING CHARACTERISTICS(Recommended operating conditions)

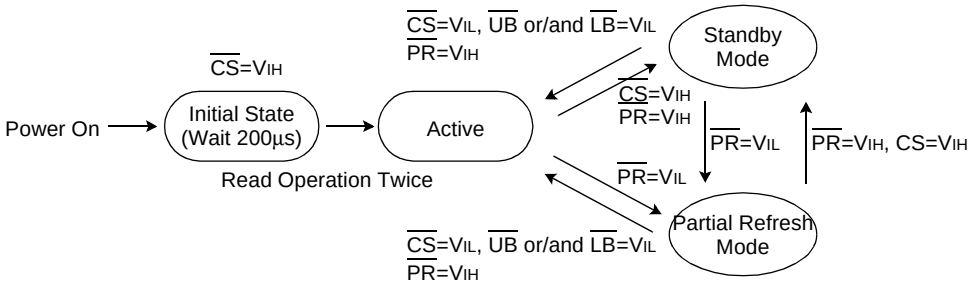
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	µA
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	
Operating Current	Sequential Read	$I_{CC}1$	tRC=50ns, $\overline{CE}$=V_{IL} I_{OUT}=0mA	-	10	20	mA
	Program	$I_{CC}2$	-	-	10	20	
	Erase	$I_{CC}3$	-	-	10	20	
Input High Voltage		V_{IH}	-	2.0	-	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA
Stand-by Current(TTL)		$I_{SB}1$	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	mA
Stand-by Current(CMOS)		$I_{SB}2$	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA

U*t*RAM DC AND OPERATING CHARACTERISTICS (Each component)

Item	Symbol	Test Conditions	Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{PR}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{PR}$≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	3	7	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{PR}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	35	40	mA
Input high voltage	V_{IH}	-	2.0	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-	-0.3[3)]	-	0.6	V
Output high voltage	V_{OH}	I_{OH}=-0.5mA	2.0	-	-	V
Output low voltage	V_{OL}	I_{OL}=0.5mA	-	-	0.4	V
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, $\overline{PR}$≥Vcc-0.2V, Other inputs=Vss to Vcc	-	80	100	µA
Partial Refresh Current	I_{SBP}	$\overline{PR}$≤0.2V, Other inputs=Vss to Vcc	-	50	60	µA

1. Typical values are tested at V_{CC}=2.5V, T_A=25°C and not guaranteed.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

STANDBY MODE STATE MACHINES(U*t*RAM)



STANDBY MODE CHARACTERISTIC(U*t*RAM)

Power Mode	Address	Memory Cell Data	Standby Current(µA)
Standby	00000h ~ 3FFFFFh	Valid	100
Partial Refresh	00000h ~ 0FFFFFh	Vaild	60

CAPACITANCE (T_A = 25 °C, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C_{DQ}	V_{IL}=0V	-	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	20	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

VALID BLOCK(Flash)

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1004	-	1024	Blocks

NOTE:

1. The Flash memory may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not try to access these invalid blocks for program and erase. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Flash AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL GATE and CL=50pF

Flash Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

Flash AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

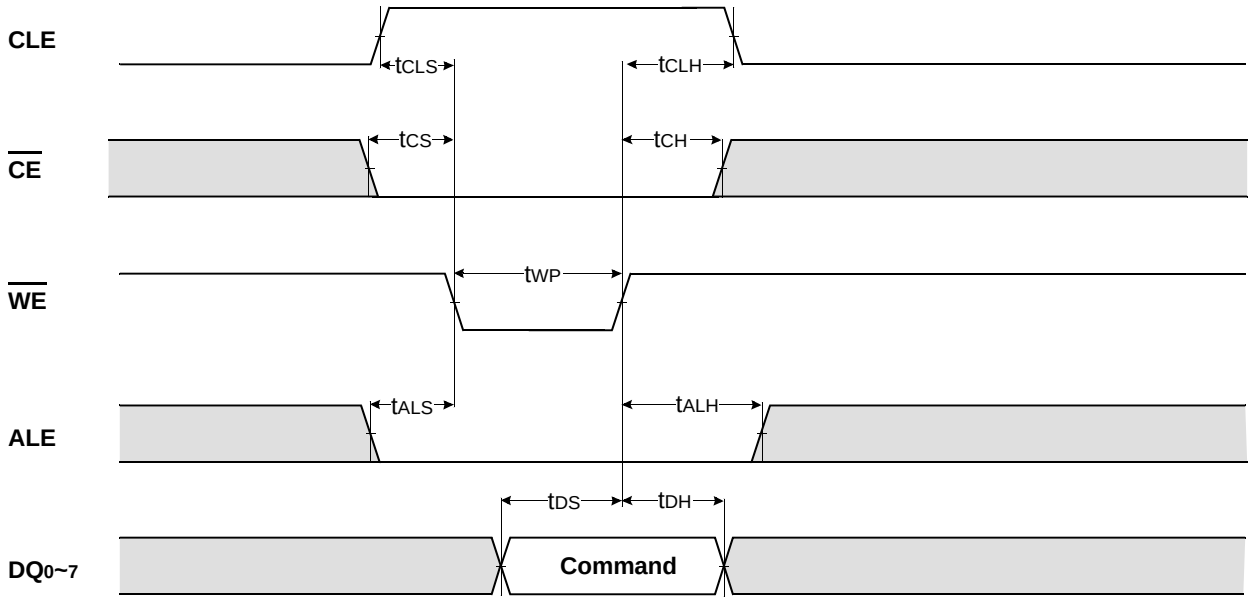
NOTE: 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

Flash AC Characteristics for Operation

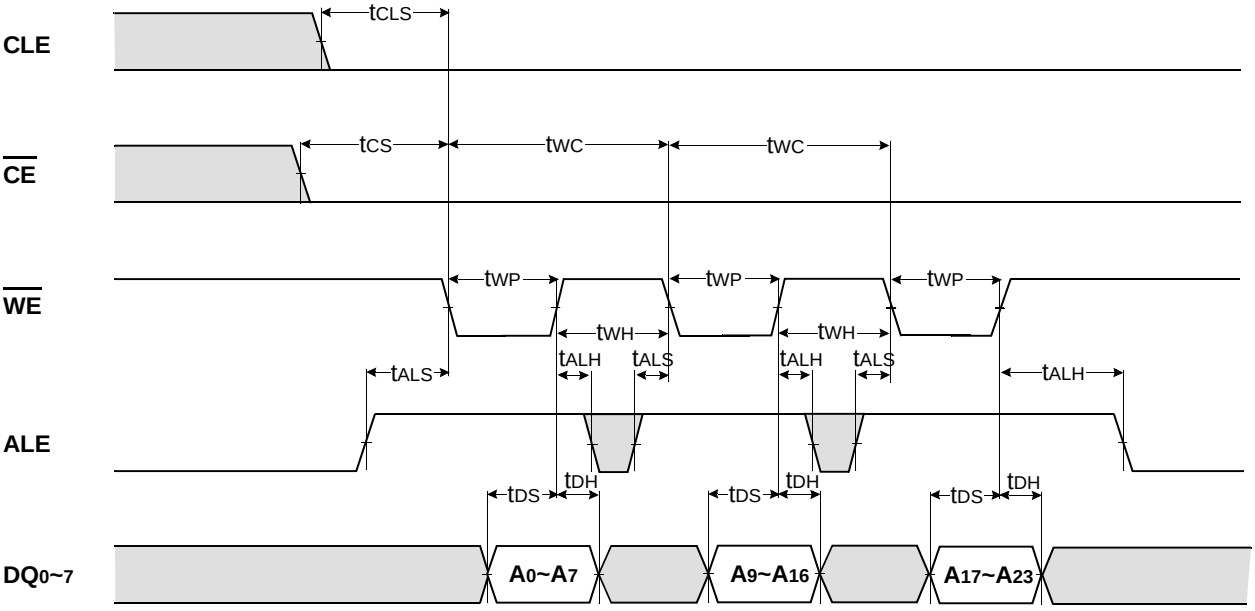
Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	25	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{CE}$ Access Time	t_{CEA}	-	45	ns
$\overline{RE}$ Access Time	t_{REA}	-	30	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NOTE :
1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.

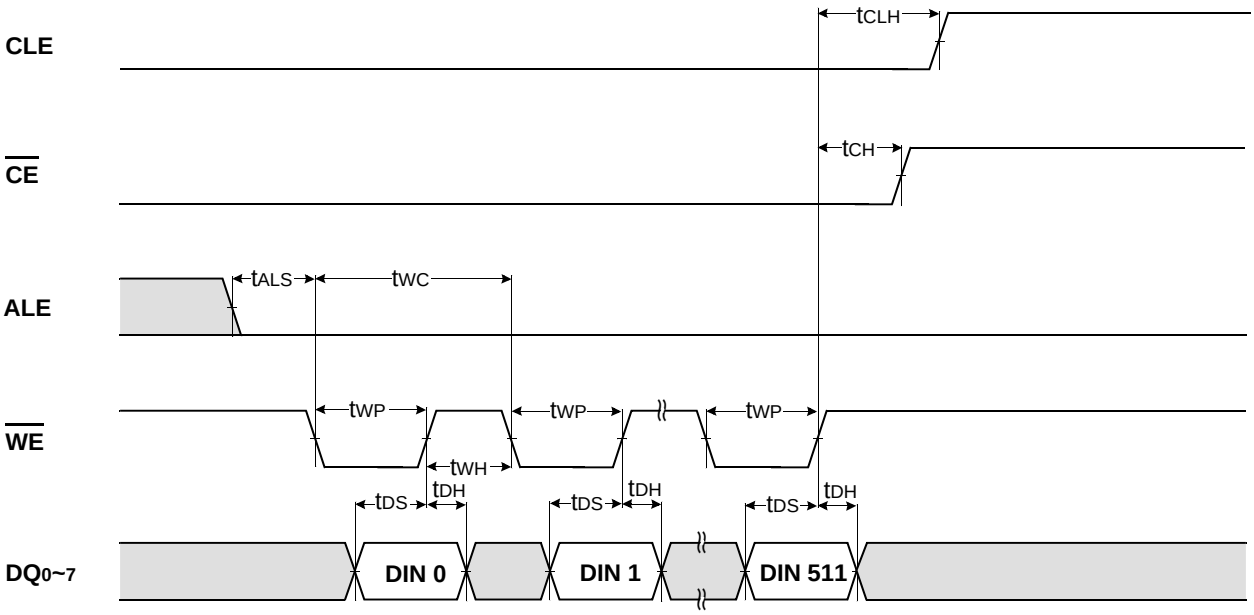
Flash Command Latch Cycle



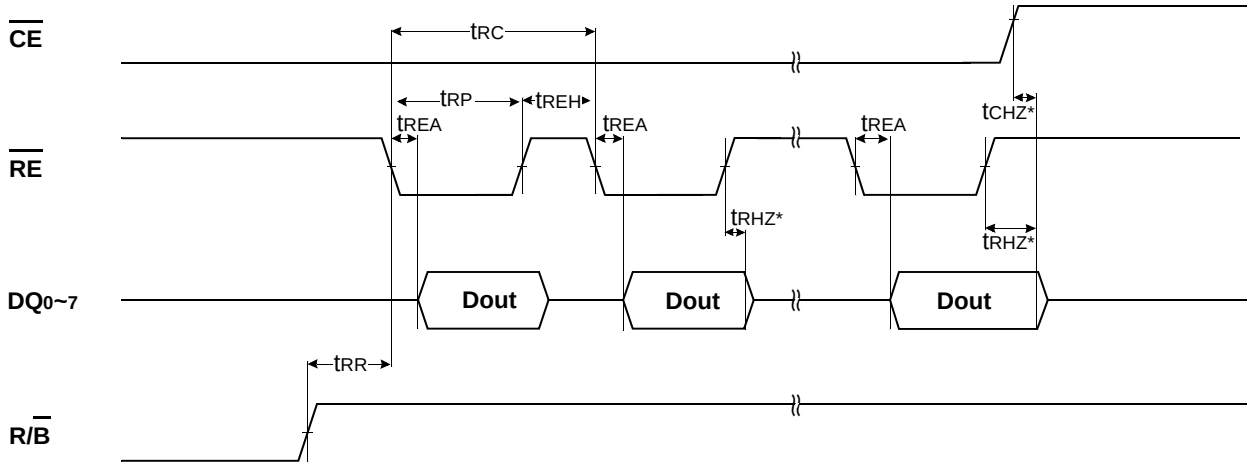
Flash Address Latch Cycle



Flash Input Data Latch Cycle

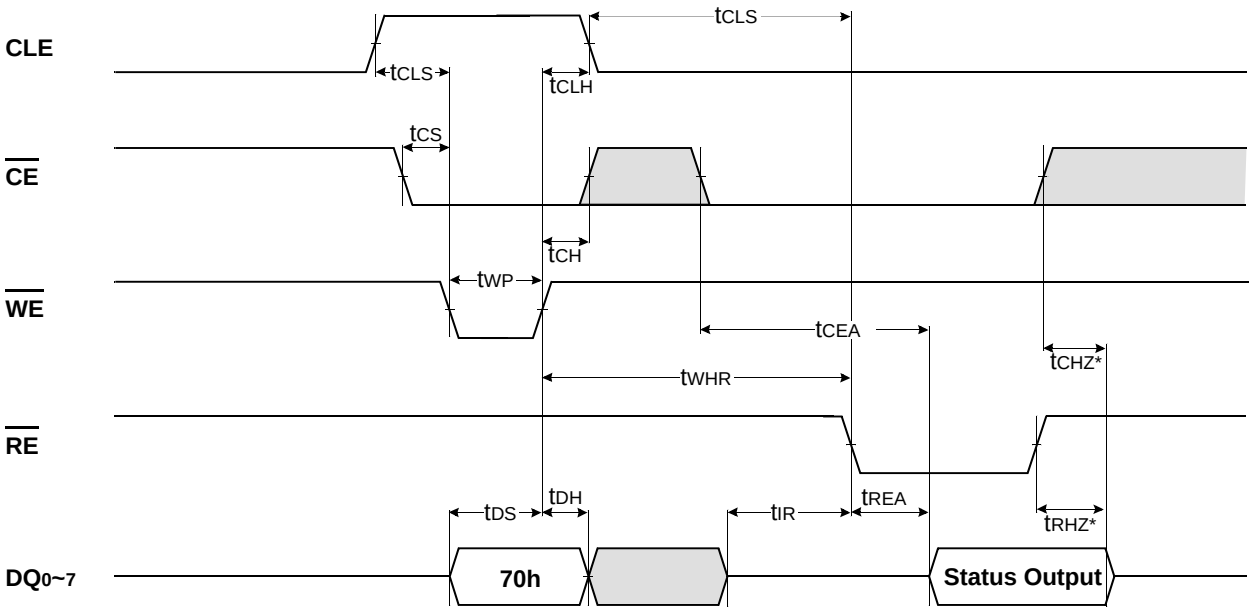


Flash Sequential Out Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

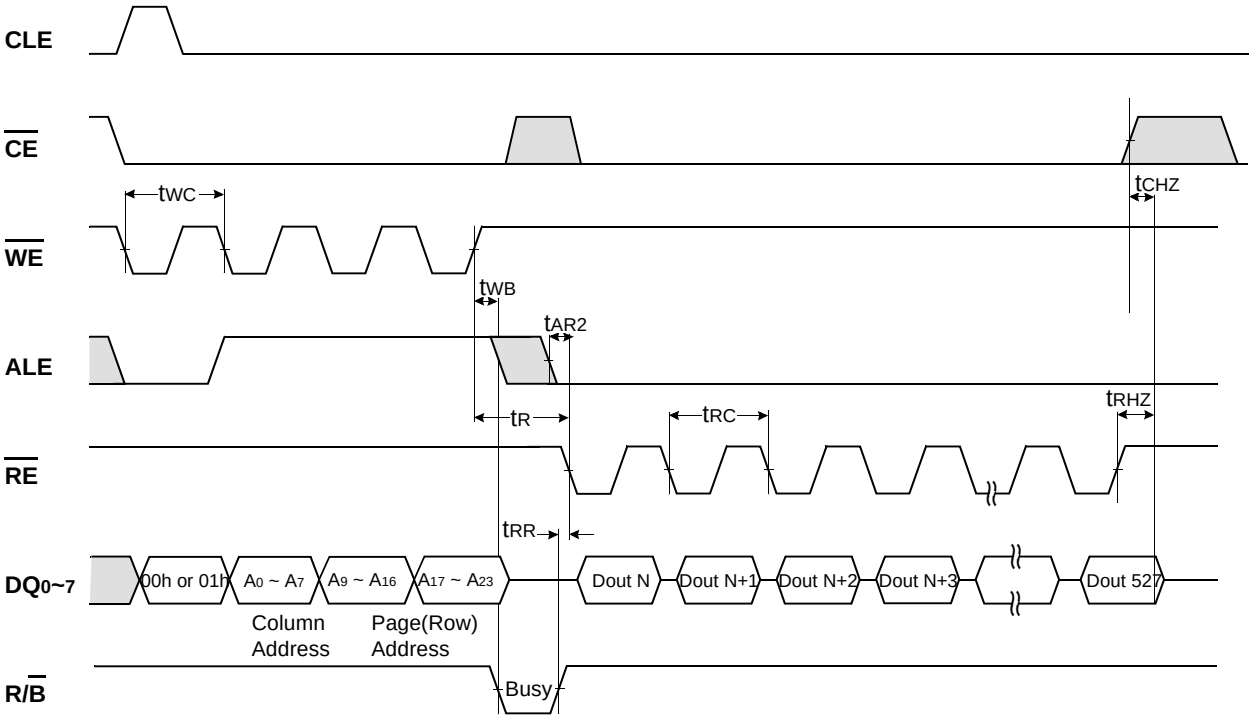


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

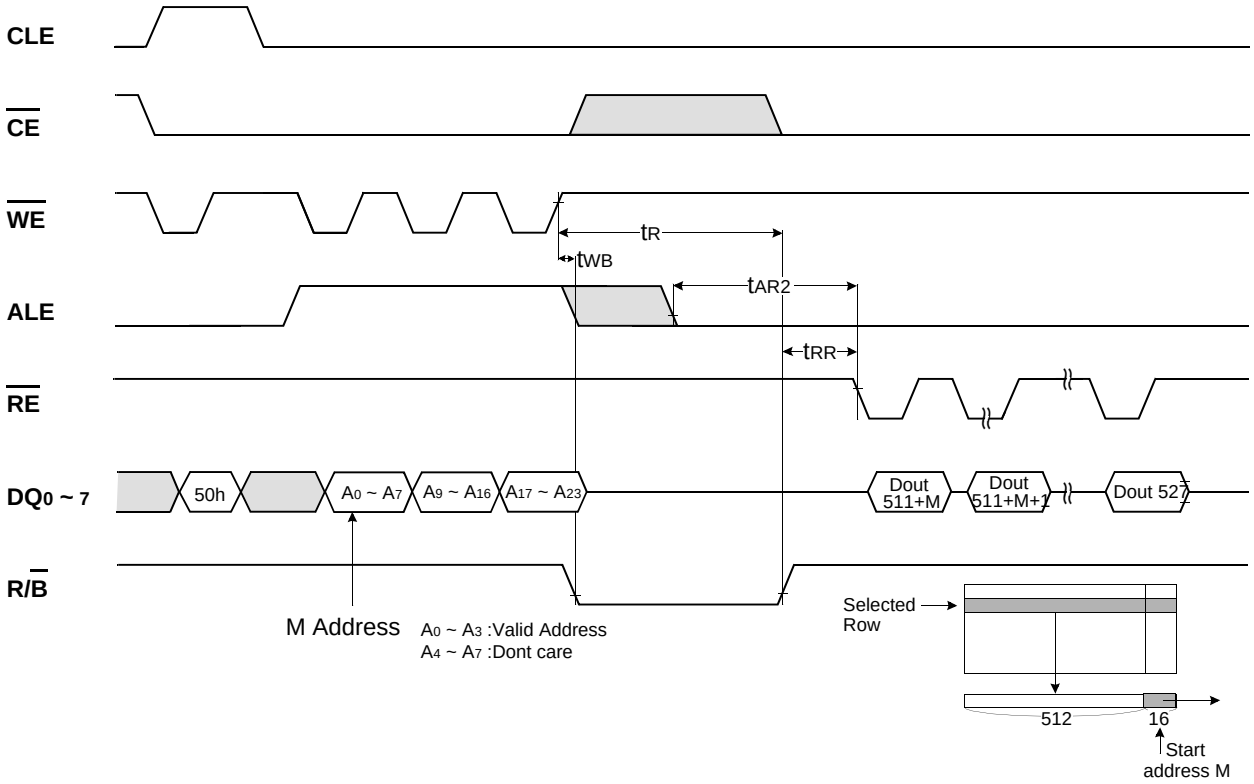
Flash Status Read Cycle



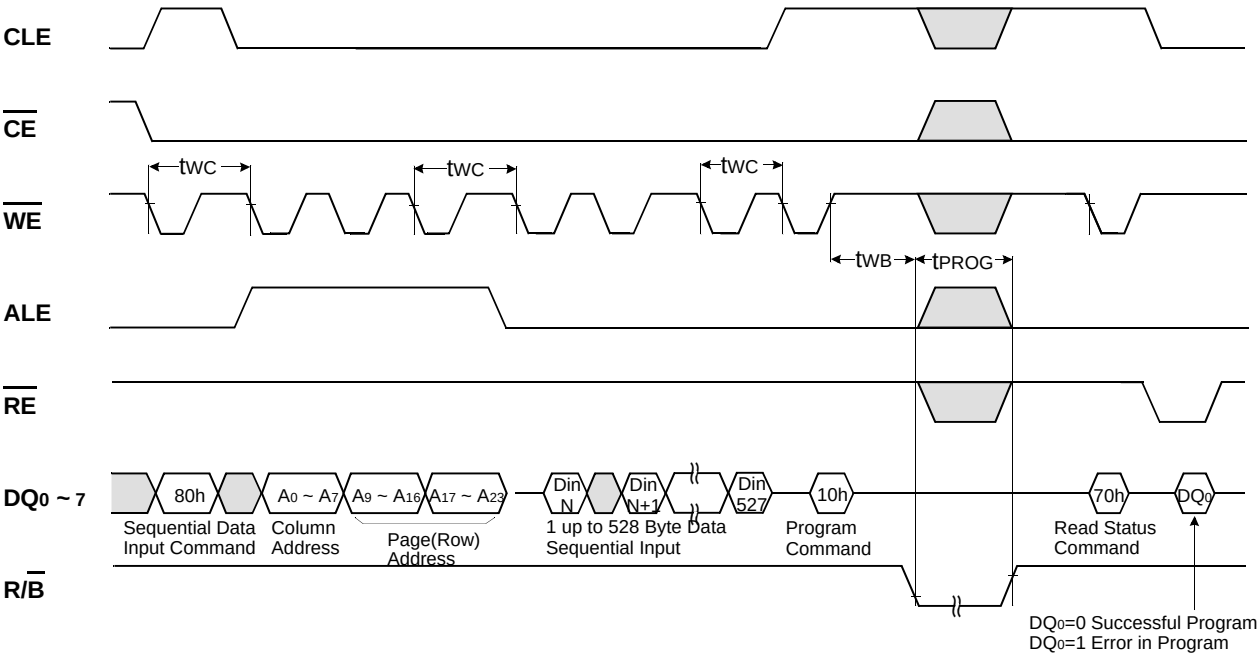
FLASH READ1 OPERATION(READ ONE PAGE)



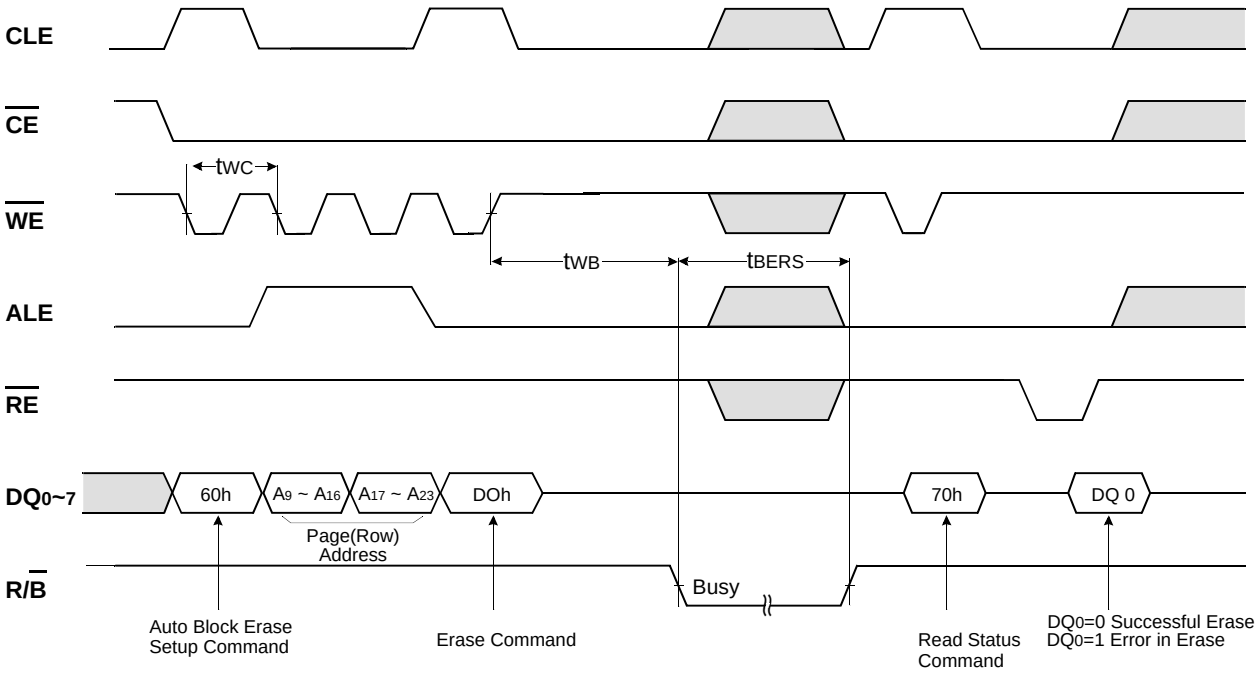
FLASH READ2 OPERATION(READ ONE PAGE)



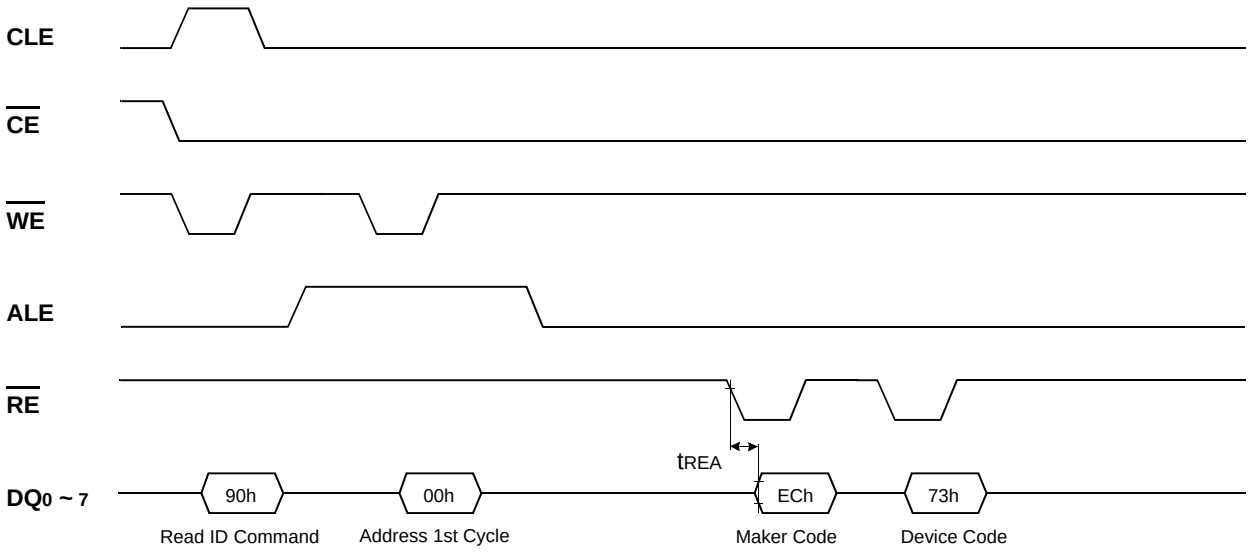
FLASH PAGE PROGRAM OPERATION



FLASH BLOCK ERASE OPERATION(ERASE ONE BLOCK)



FLASH MANUFACTURE & DEVICE ID READ OPERATION



UtRAM AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.1V
Output load: C_L=80pF

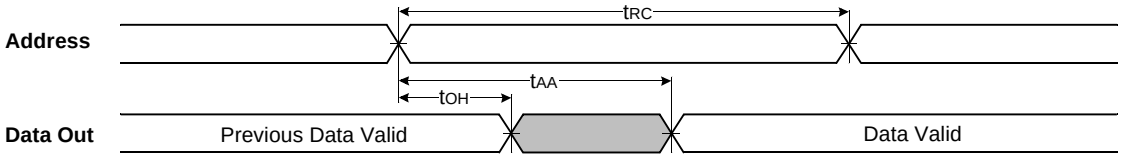
UtRAM AC CHARACTERISTICS(V_{CC}=2.3~2.7V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed		Units
			80ns		
			Min	Max	
Read	Read Cycle Time	t_{RC}	80	-	ns
	Address Access Time	t_{AA}	-	80	ns
	Chip Select to Output	t_{CO}	-	80	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	80	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold from Address Change	t_{OH}	10	-	ns
Write	Write Cycle Time	t_{WC}	80	-	ns
	Chip Select to End of Write	t_{CW}	70	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	70	-	ns
	Write Pulse Width	t_{WP}	60	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	ns
	Data to Write Time Overlap	t_{DW}	35	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns

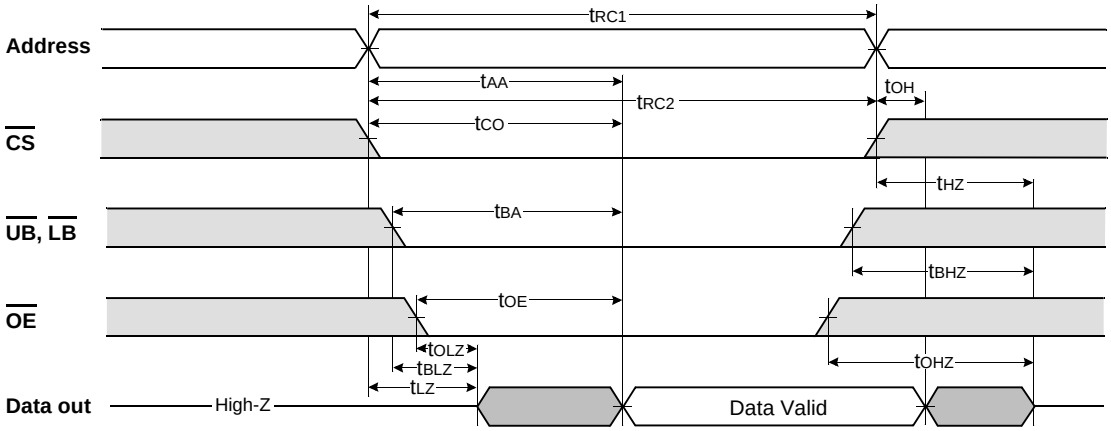
1. The limitation in continuous write operation is up to 50 times. If you want to write continuously over 50 times, please refer to the technical note.

U*t*RAM TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{PR}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



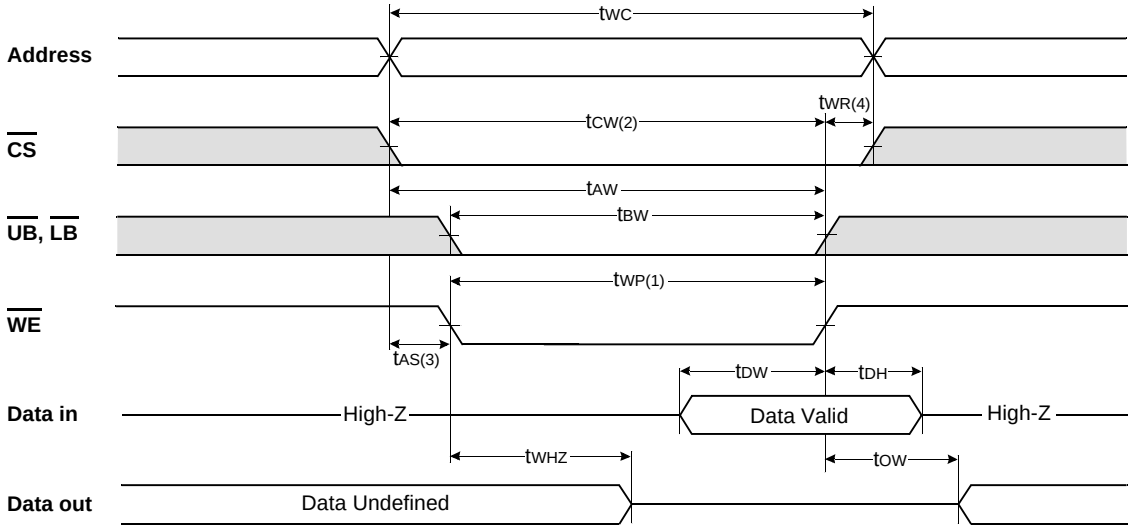
TIMING WAVEFORM OF READ CYCLE(2)($\overline{PR}$=$\overline{WE}$=V_{IH})



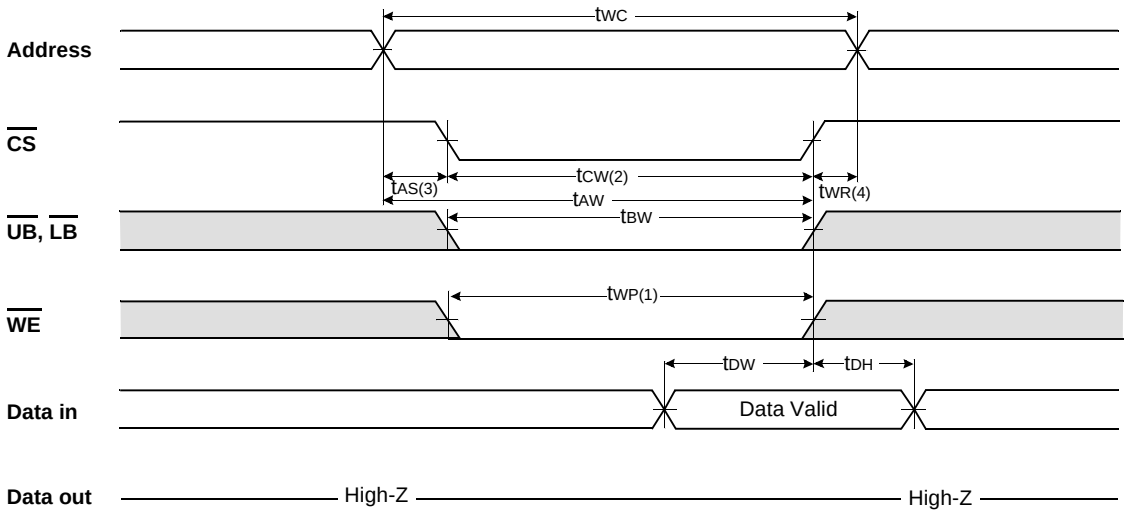
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined by longer one of t_{RC1} and t_{RC2}.
4. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).

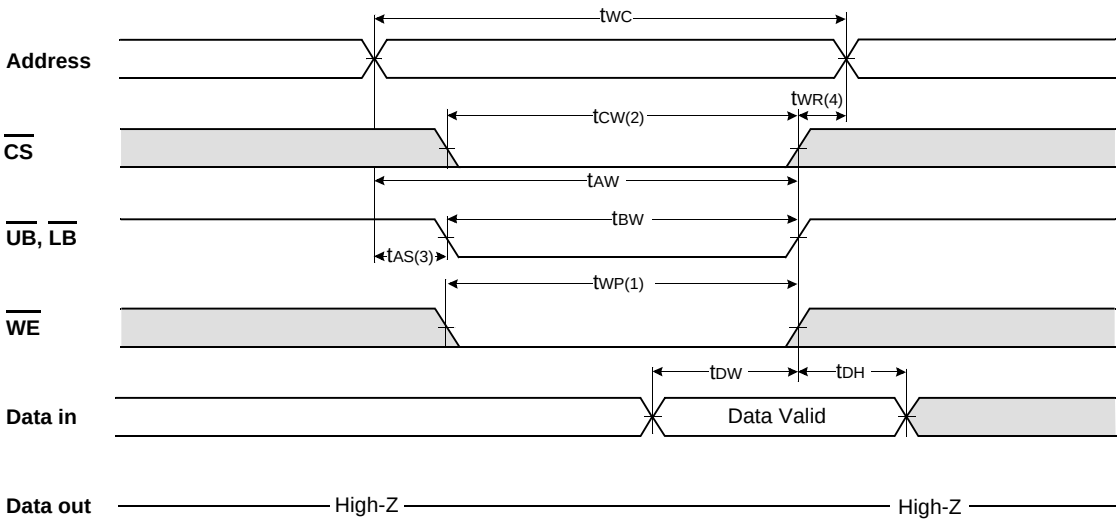
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{PR}$=V_{IH})



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled, $\overline{PR}$=V_{IH})



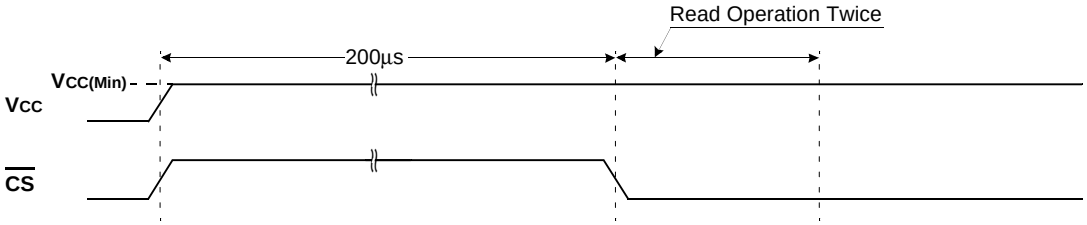
TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{PR}$=V_{IH})



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

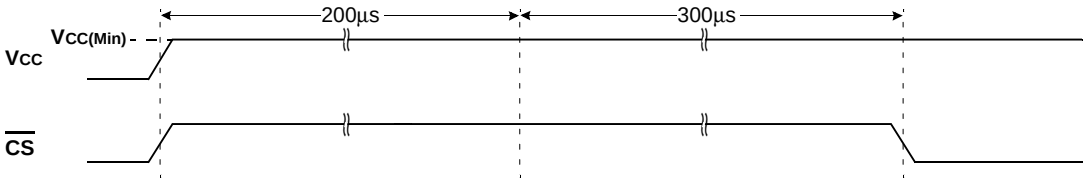
TIMING WAVEFORM OF POWER UP(1)



(POWER UP(1))

1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs with $\overline{CS}$ high and then toggle $\overline{CS}$ low and commit Read Operation at least twice. Then you get into the normal operation.
2. Read operation should be executed by toggling $\overline{CS}$ pin low.
3. The read operation must satisfy the specified t_{RC}.

TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle)



(POWER UP(2))

1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs and wait another 300µs with $\overline{CS}$ high if you don't want to commit dummy read cycle. After total 500µs wait, toggle $\overline{CS}$ low, then you get into the normal mode.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte(X8 device) or 1st & 6th word(X16 device) in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh(X8 device) or non-FFFFh(X16 device) data at the column address of 517(X8 device) or 256 and 261(X16 device). Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 11). Any intentional erasure of the original invalid block information is prohibited.

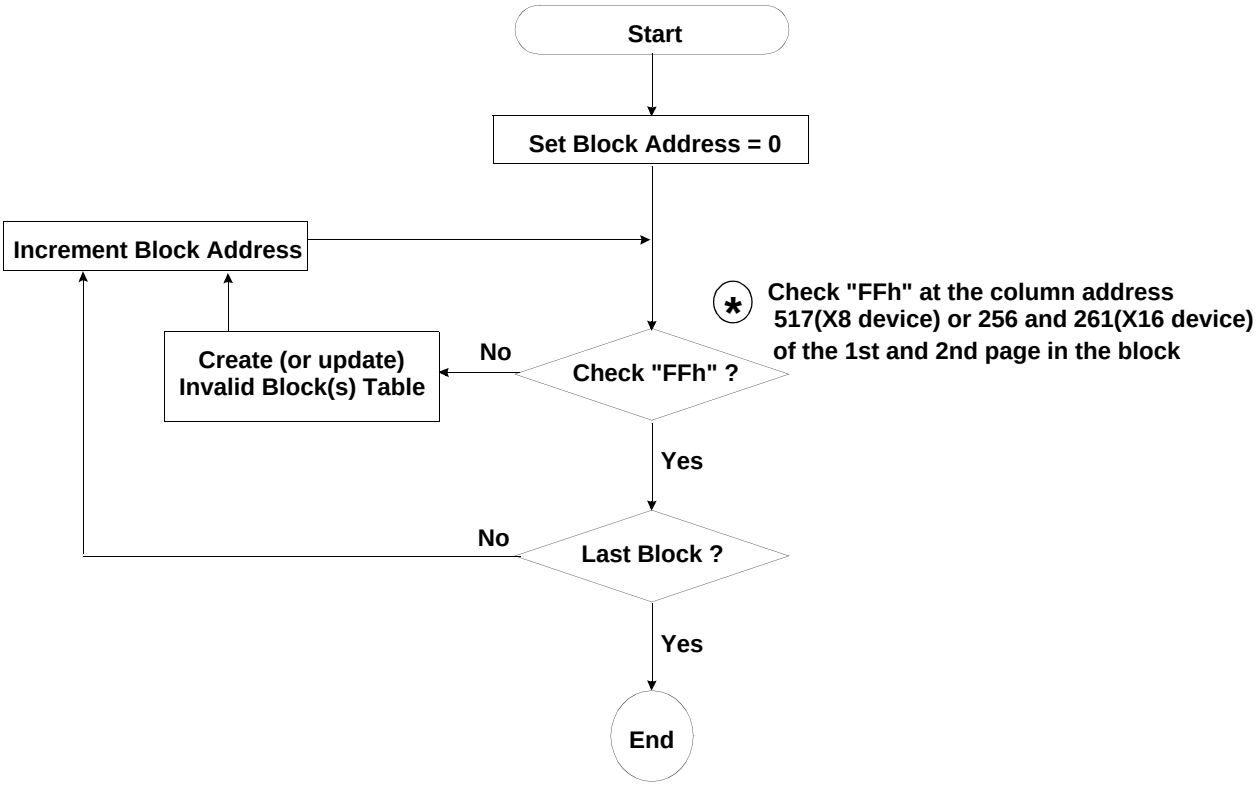


Figure 11. Flow chart to create invalid block table.

NAND Flash Technical Notes

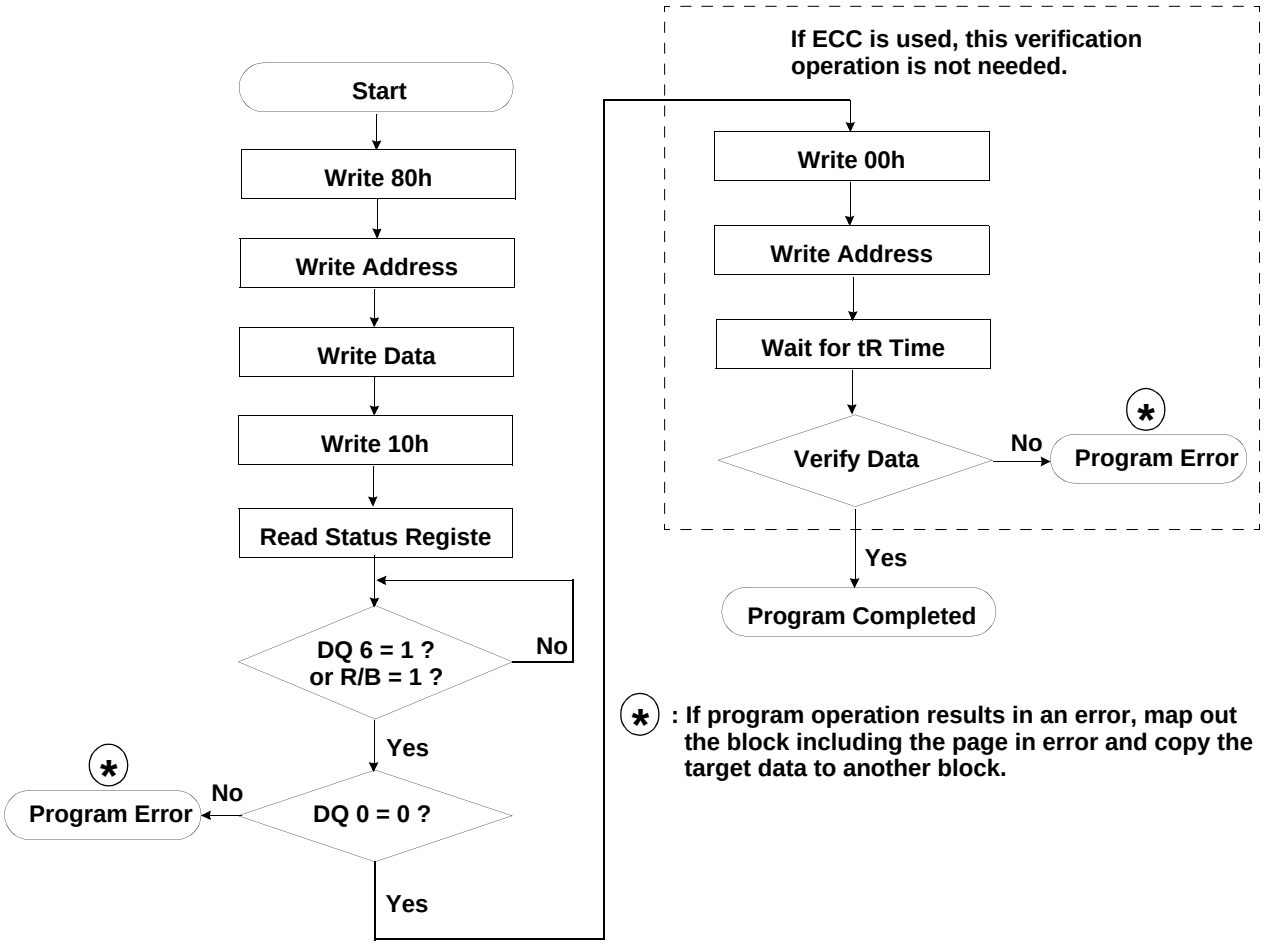
Error in write or read operation

Over its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, so you can execute block replacement on a page basis with a page sized buffer. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Figure 12. Flash Program flow chart



NAND Flash Technical Notes

Figure 13. Flash Erase Flow Chart

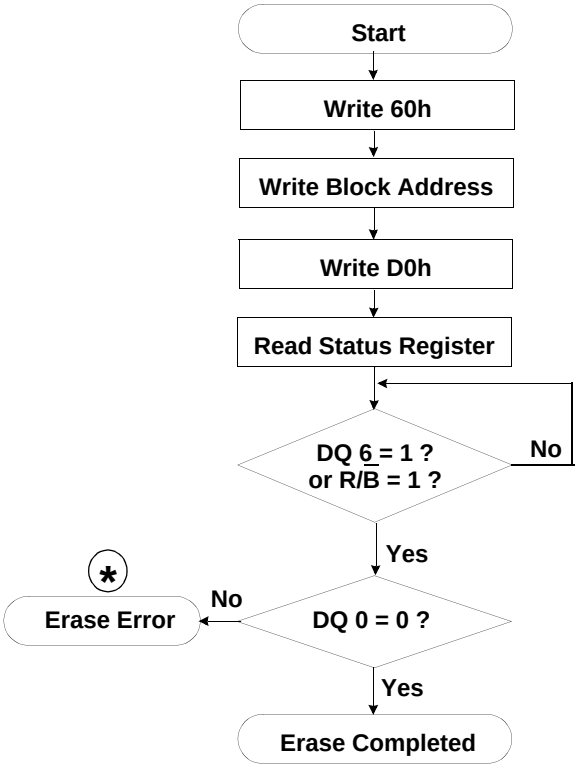
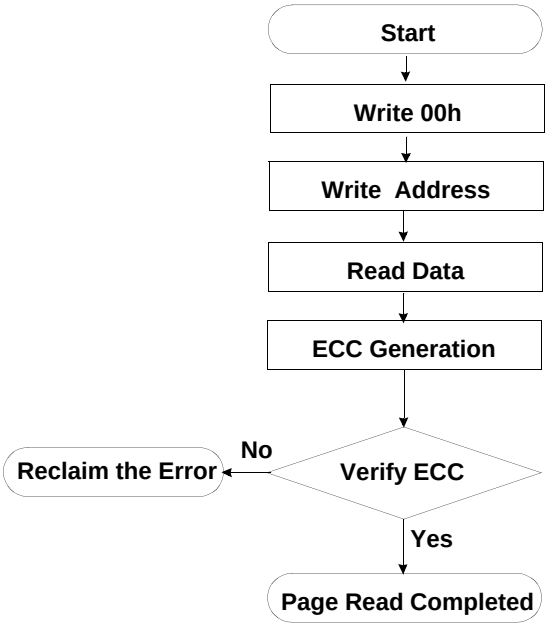
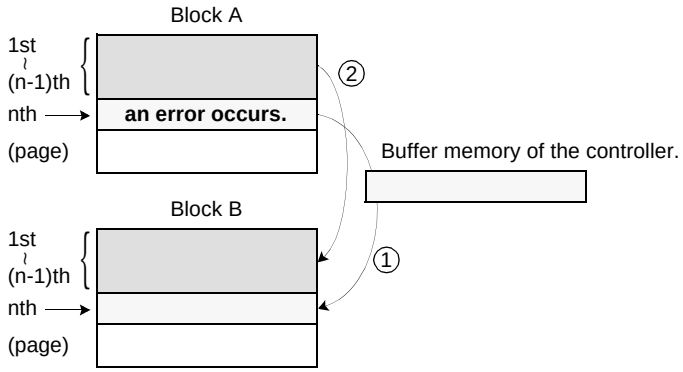


Figure 14. Flash Read Flow Chart



: If erase operation results in an error, map out the failing block and replace it with another block.

Figure 15. Flash Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

NAND Flash Technical Notes

Pointer Operation of NAND Flash

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

Table 6. Destination of the pointer

Command	Pointer position	Area
00h 01h 50h	0 ~ 255 byte 256 ~ 511 byte 512 ~ 527 byte	1st half array(A) 2nd half array(B) spare array(C)

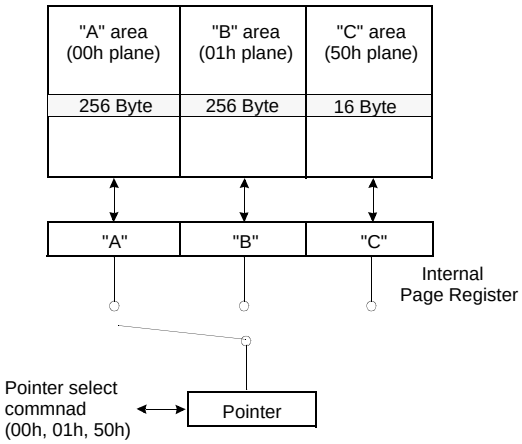
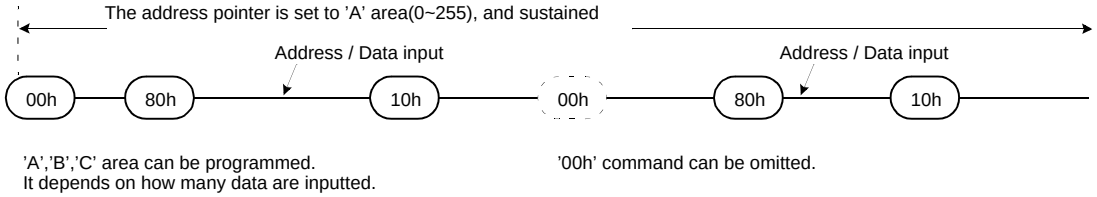
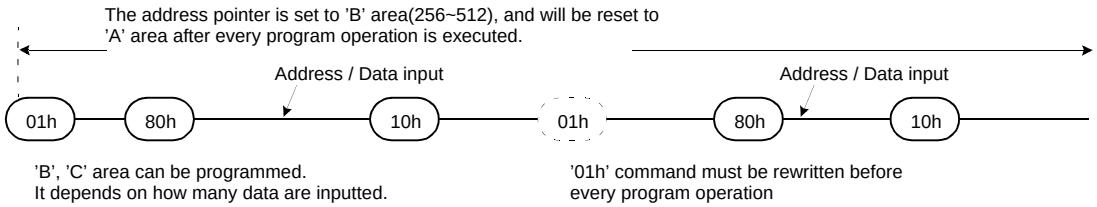


Figure 16. Block Diagram of Pointer Operation

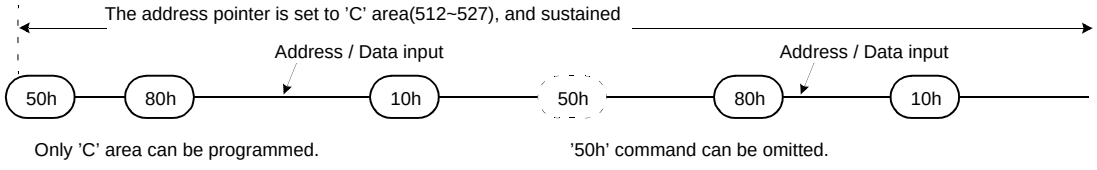
(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



(3) Command input sequence for programming 'C' area



NAND Flash Technical Notes

System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant saving in power consumption.

Figure 17. Program Operation with $\overline{CE}$ don't-care.

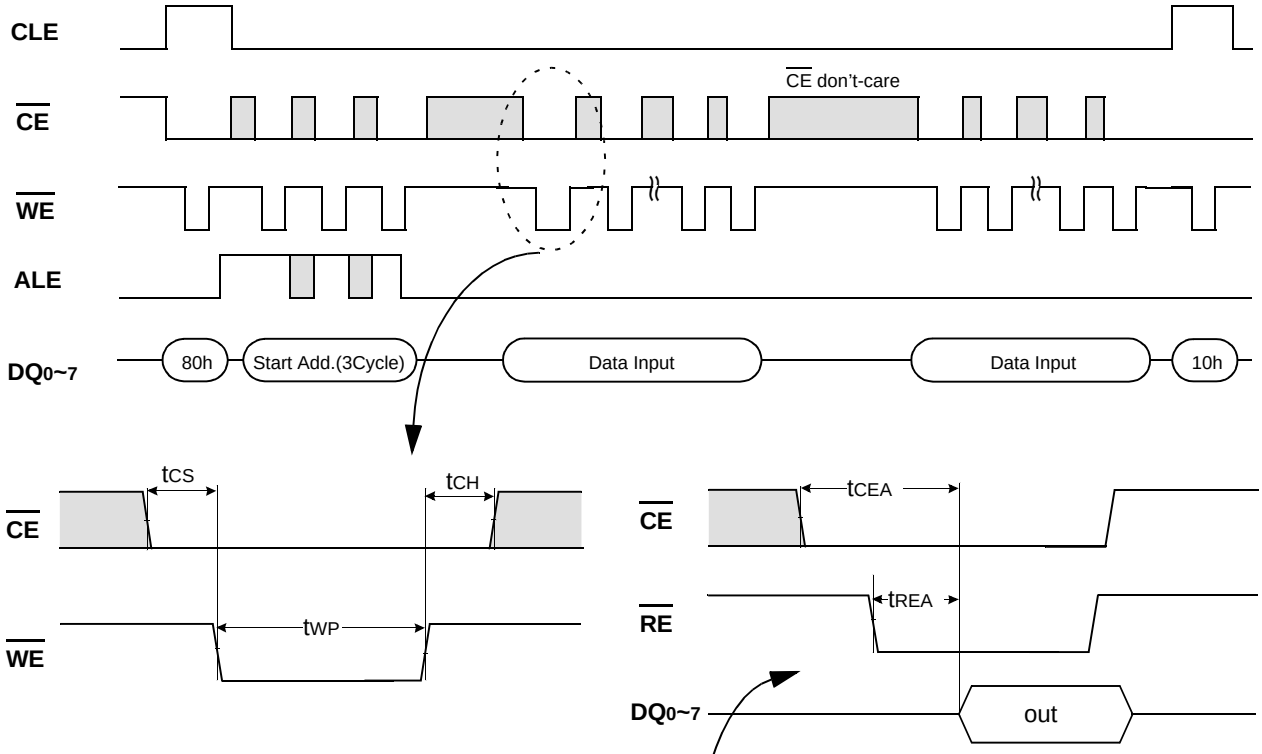
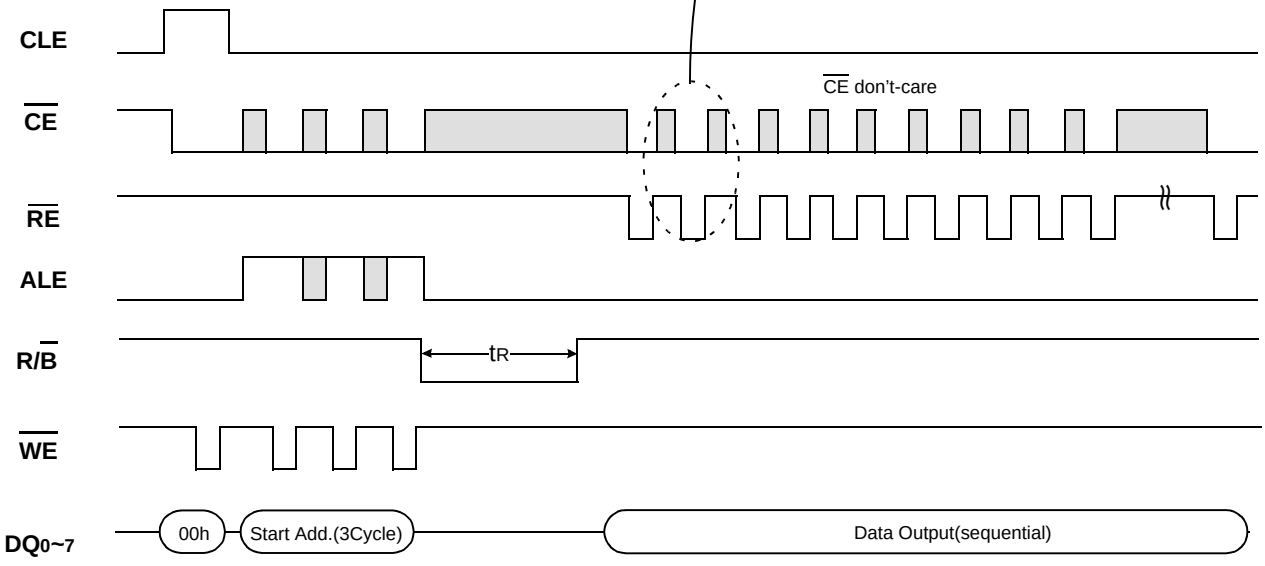


Figure 18. Read Operation with $\overline{CE}$ don't-care.



TECHNICAL NOTE

UtRAM USAGE AND TIMING

INTRODUCTION

UtRAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the UtRAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

START WITH A DRAM TECHNOLOGY

The key point of UtRAM is its high speed and low power. This high speed comes from the use of many small blocks such as 32Kbits each to create UtRAM arrays. The small blocks have short word lines thus with little capacitance eliminating a major factor of operating current dissipation in conventional DRAM blocks.

Each independent macro-cell on a UtRAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. UtRAM performs a complete read operation in every tRC, but UtRAM needs power up sequence like DRAM.

Power Up Sequence and Diagram
1. Apply power.
2. Maintain stable power for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least 2 times.

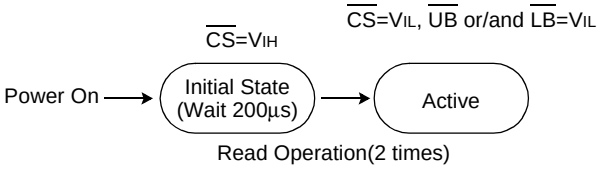


Figure 1.

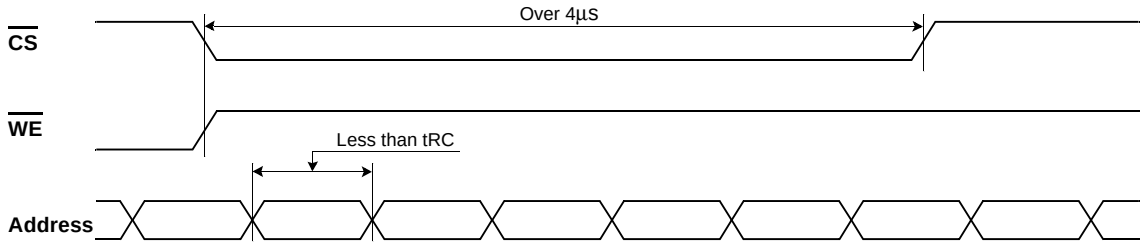
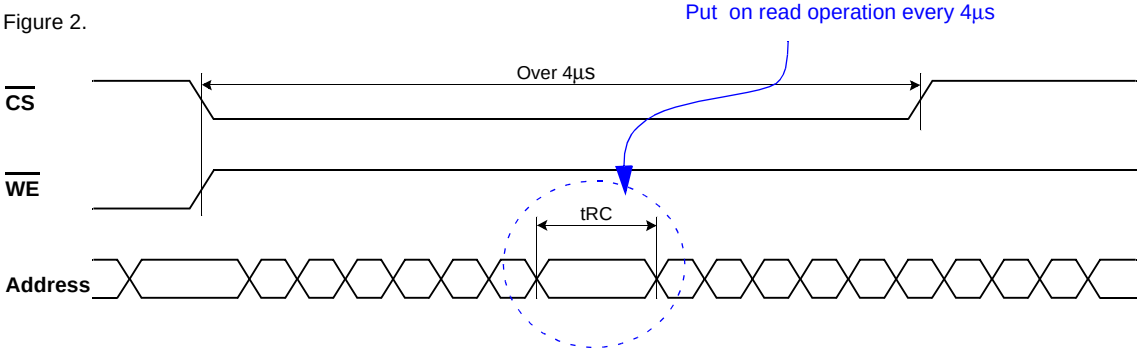


Figure 2.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The UtRAM was designed to work just like an SRAM - without any waits or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations inside with advanced design technology - those are not to be seen from outside. Precharging takes place during every access, overlapped between the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult. Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides an internal refresh controller for devices. When all accesses within refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM is sometimes used on these applications, which requires a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG's unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the UtRAM never need to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

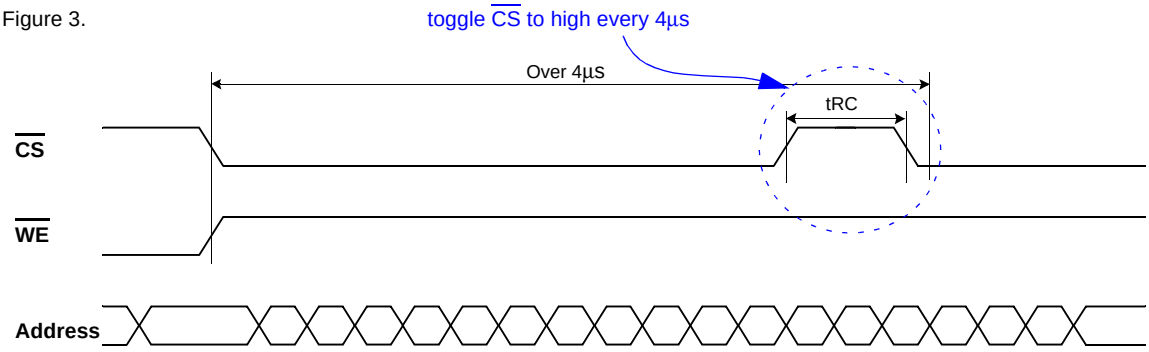
AVOID TIMING

Following figures show you an abnormal timing which is not supported on UtRAM and its solution.

If your system has a timing which sustains invalid states over 4µs at read mode like Figure 1, there are some guide lines for proper operation of UtRAM.

When your system has multiple invalid address signals shorter than tRC on the timing shown in Figure 1, UtRAM needs a normal read timing(tRC) during that cycle(Figure 2) or needs to toggle $\overline{CS}$ once to 'high' for about 'tRC'(Figure 3).

Figure 3.



Write operation has similar restriction to Read operation. If your system has a timing which sustains invalid states over 4µs at write mode and has continuous write signals with length of Min. tWC over 4µs like Figure 4, you must toggle WE once to high and make it stay high at least for tRC every 4µs or toggle CS once to high for about tRC.

Figure 4.

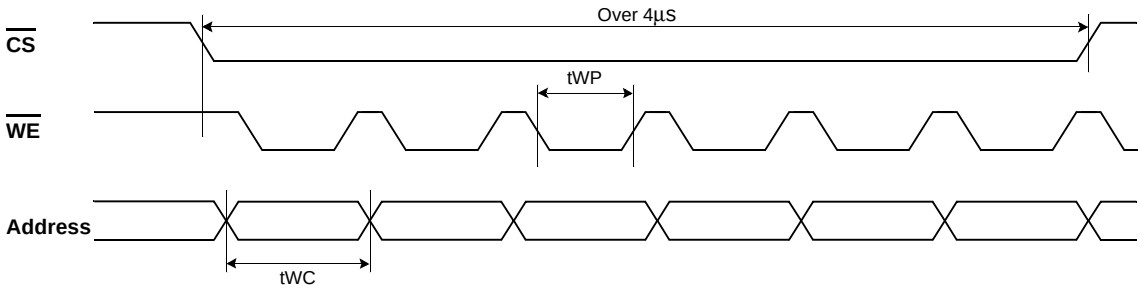


Figure 5.

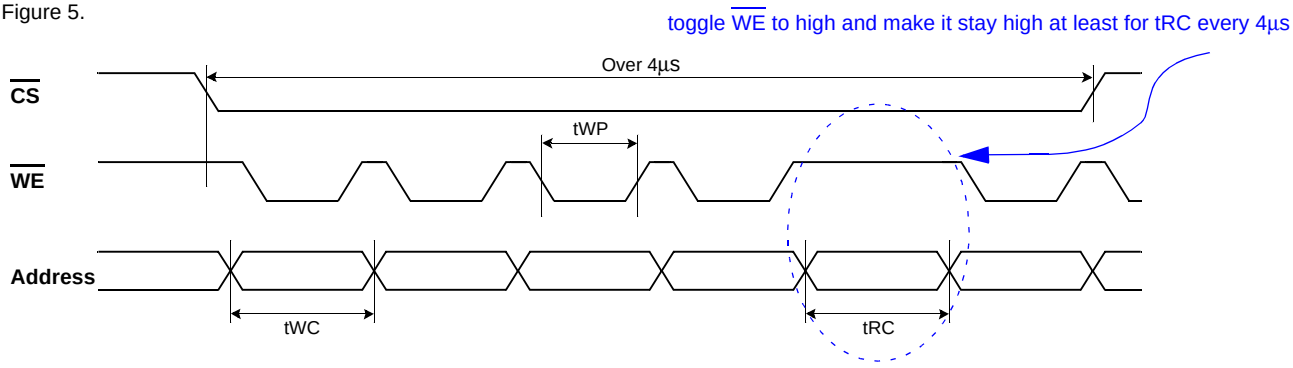
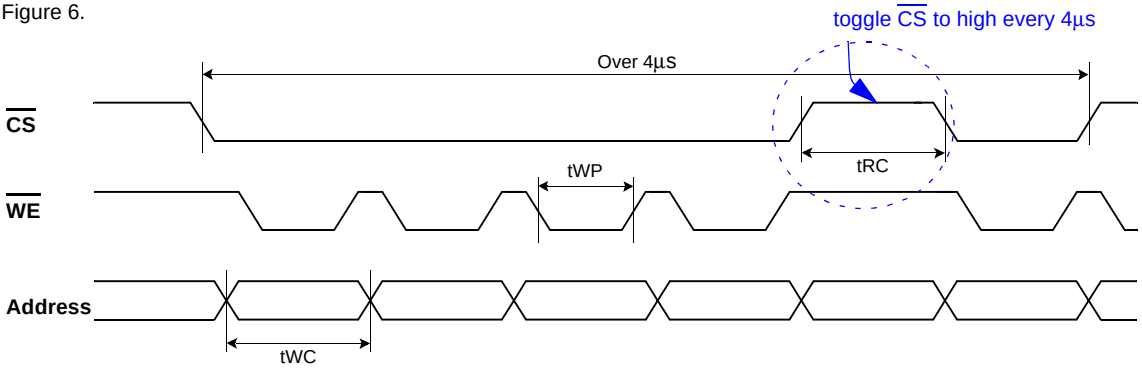


Figure 6.



PACKAGE DIMENSION

111-Ball Tape Ball Grid Array Package (measured in millimeters)