DRAM

4 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle

OPTIONS — MARKING

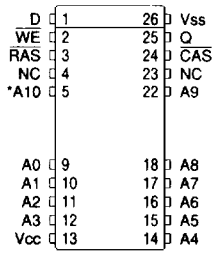
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil)** — TG
  - Plastic ZIP (350 mil) — Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book***.

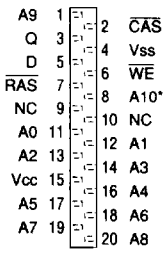
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
- Part Number Example: MT4C1004JDJ-6

PIN ASSIGNMENT (Top View)

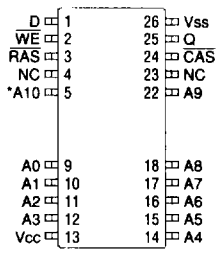
20-Pin SOJ (Q-1)



20-Pin ZIP (O-1)



20-Pin TSOP (R-1)



*Address not used for $\overline{RAS}$-ONLY REFRESH
**Consult factory on availability of reverse pinout TSOP packages

GENERAL DESCRIPTION

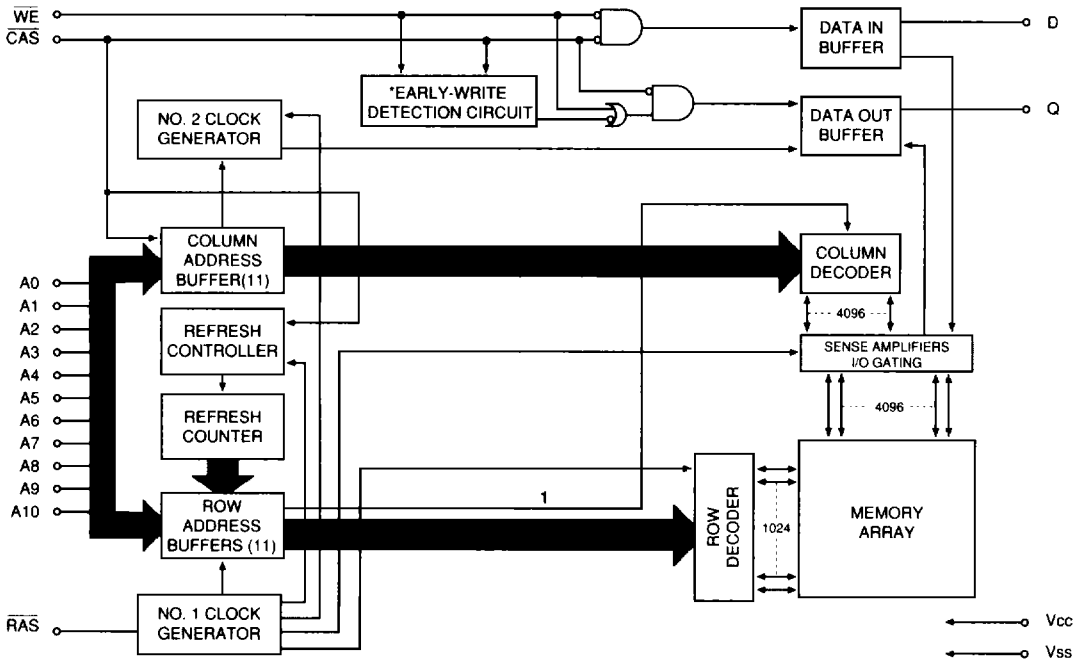
The MT4C1004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the

$\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC (MIN))	ICC3	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC (MIN))	ICC4	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: tRC = tRC (MIN))	ICC5	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC (MIN))	ICC6	110	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	60		65		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

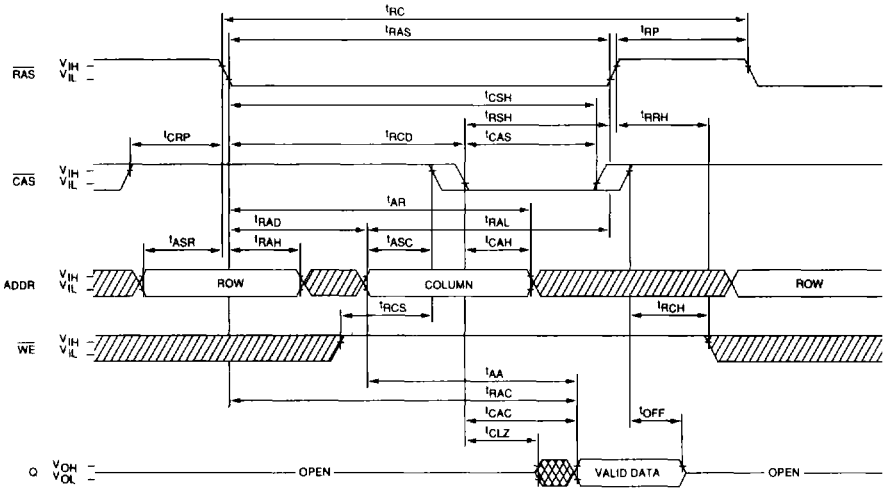
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	
Write command pulse width	^{t}WP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	15		15		20		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^{t}REF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRH	10		10		10		ns	24, 25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRP	10		10		10		ns	24, 25
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	10		10		10		ns	24, 25
$\overline{WE}$ setup time (WCBR test cycle)	^{t}WTS	10		10		10		ns	24, 25

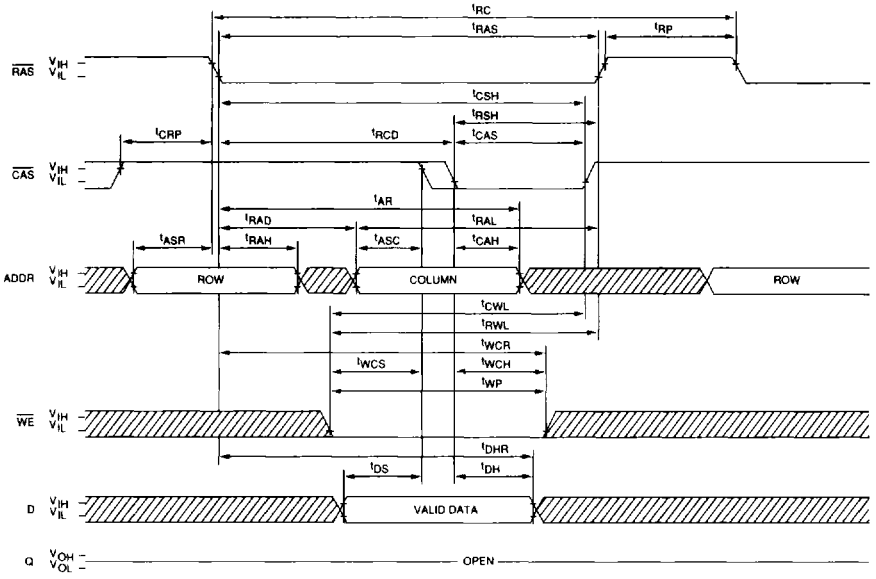
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
25. JEDEC test mode only.

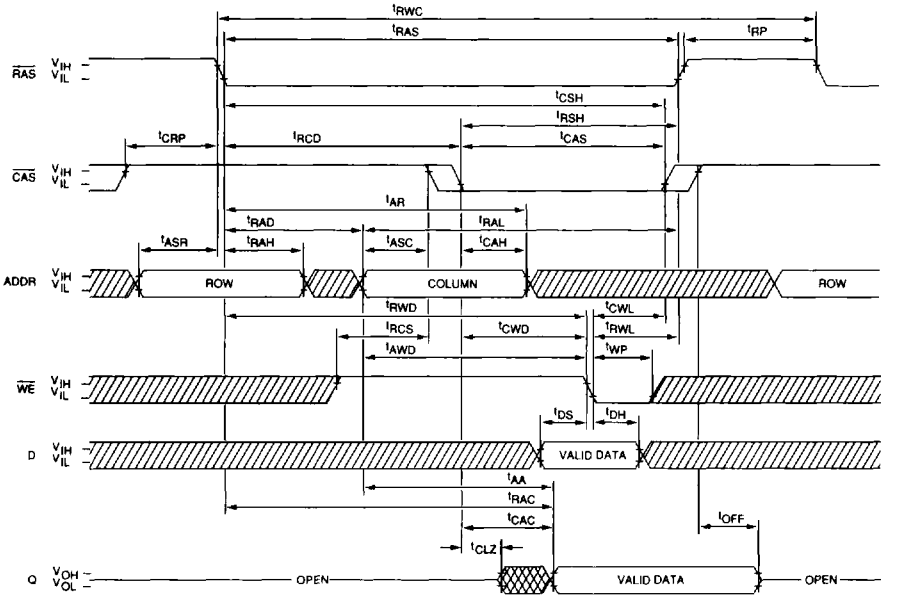
READ CYCLE



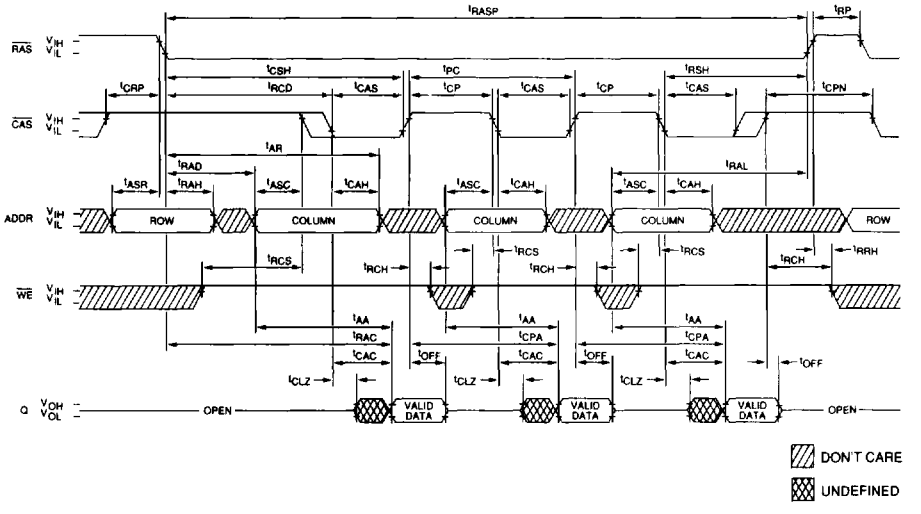
EARLY-WRITE CYCLE



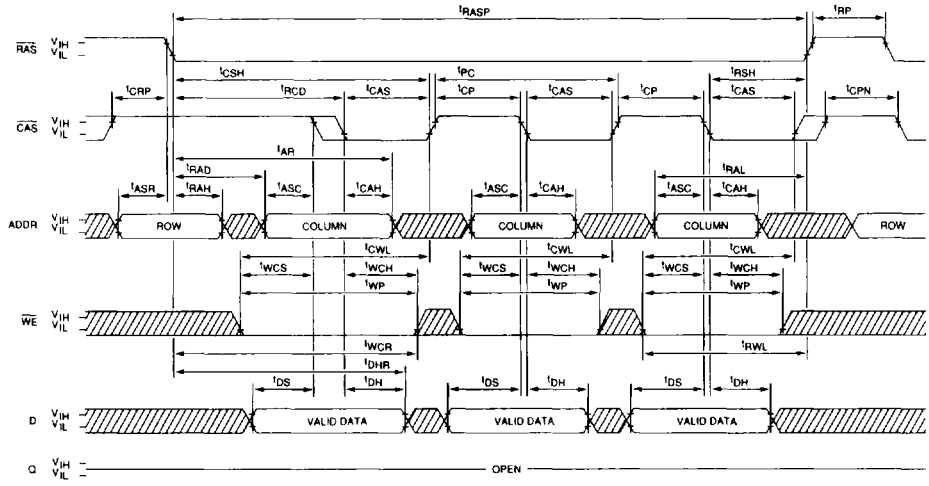
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



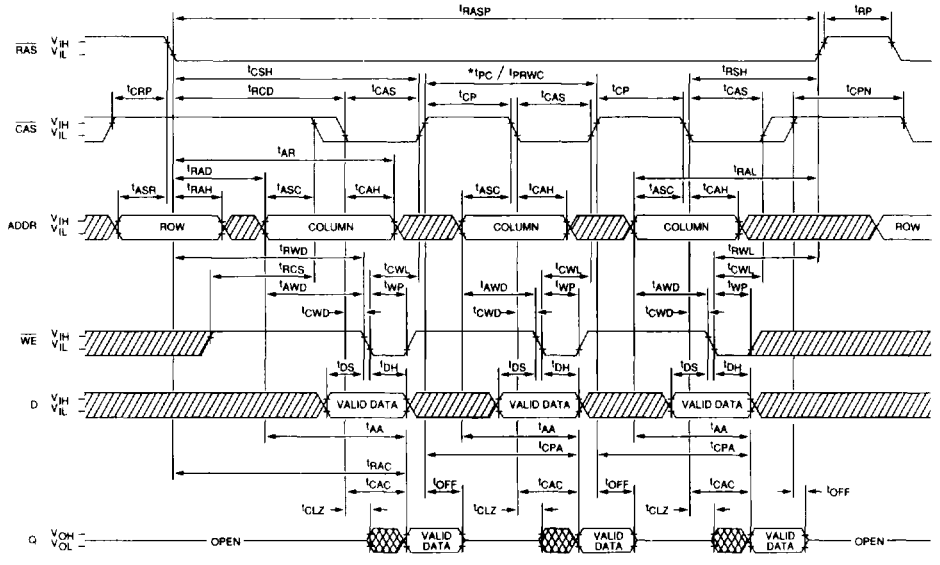
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

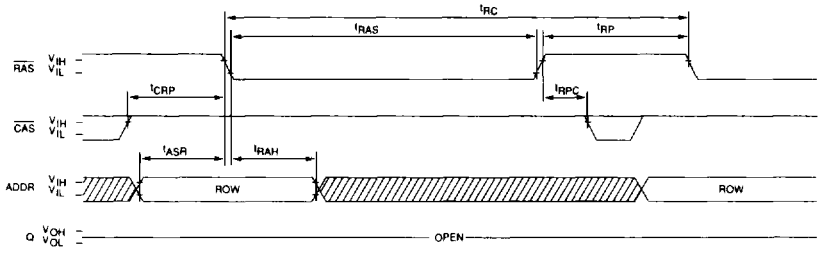


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

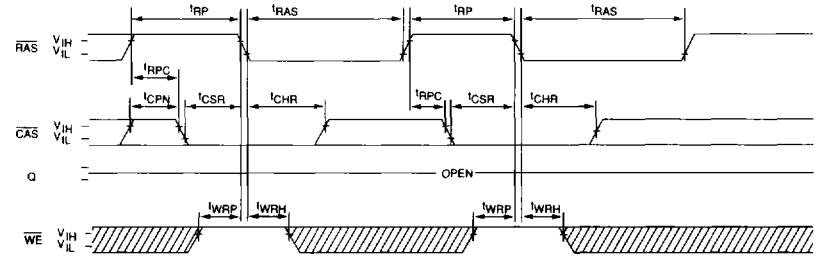


*tPC is for LATE-WRITE only.

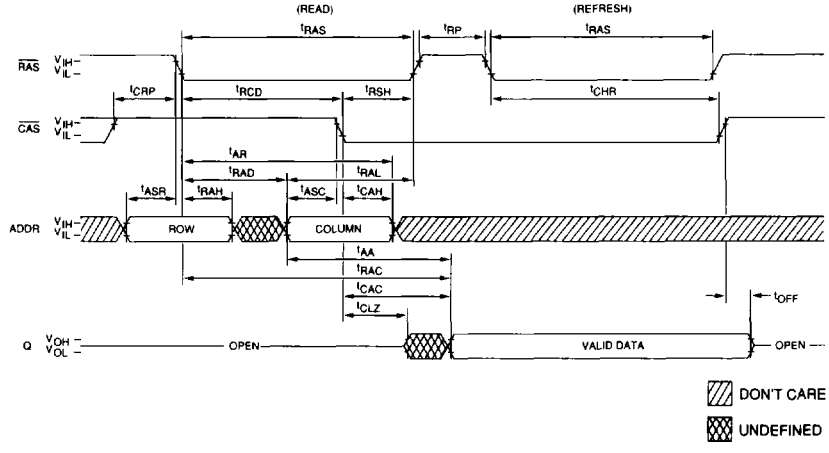
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{\text{WE}}$ = HIGH)



DRAM

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

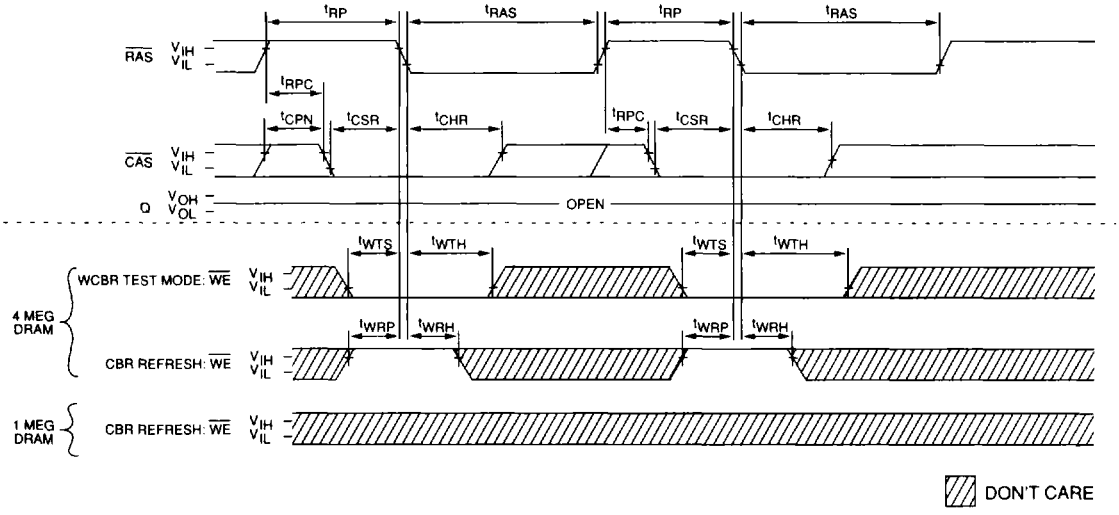
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR