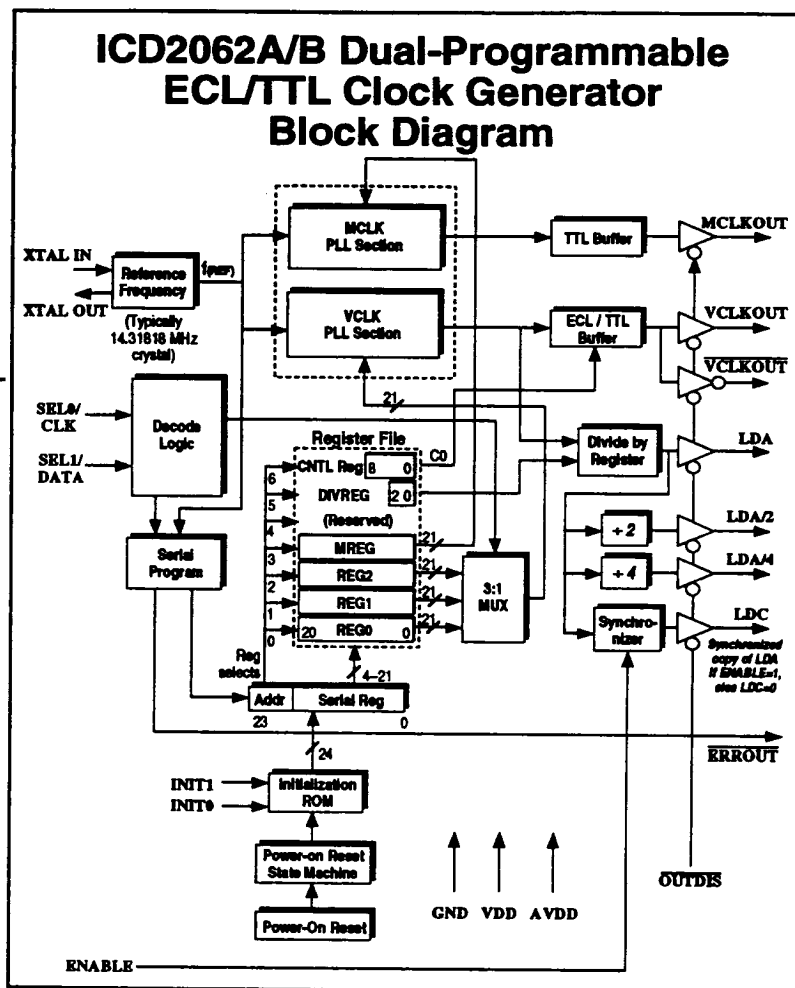


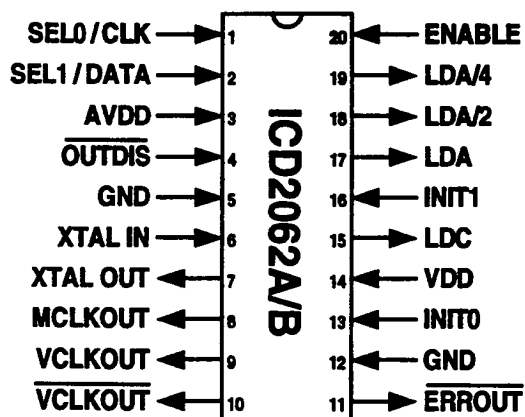
ICD2062A / ICD2062B

Dual Programmable ECL/TTL Clock Generator

Single-Chip Dual Programmable Oscillator Handles All Frequency Requirements of High-Performance Graphic Systems

- 2nd Generation Dual Oscillator Graphics Clock Generator
- 2 Independent Clock Outputs
ICD2062A: 510 KHz–135 MHz
ICD2062B: 510 KHz–185 MHz (Complementary ECL Video)
ICD2062A/B: 510 KHz–120 MHz (TTL Outputs)
- Individually Programmable Oscillators Using a Highly Reliable Manchester-Encoded 21-Bit Serial Data Word
- 2-Pin Serial Programming Interface Allows Direct Connection to Most Graphic Chip Sets with no External Hardware Required
- Programmable Video Clock Dividers Allow for Easy Interface to Most RAMDACs and VRAMs
- Tri-State Oscillator Control Disables Outputs for Test Purposes
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal Input
- Sophisticated Internal Loop-Filter Requires no External Components
- Low-Power, High-Speed, 5 Volt, 1.25 μ CMOS Technology
- Available in 20-Pin DIP or SOIC Package Configuration



Pin Descriptions

Signal Descriptions

| Signal | Pin # | Signal Function |
|-----------|-------|---|
| SEL0/CLK | 1 | Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down) |
| SEL1/DATA | 2 | Bit 1 (MSB) of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down) |
| AVDD | 3 | +5 volts to Analog Core |
| OUTDIS- | 4 | Output Disable (Tri-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if tri-state operation not required.) |
| GND | 5 | Ground |
| XTAL IN | 6 | Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available. |
| XTAL OUT | 7 | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD \approx 17 pf. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note <i>Crystal Oscillator Topics</i> (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |
| MCLKOUT | 8 | Memory Clock out |
| VCLKOUT | 9 | Differential clock outputs. Connect directly to RAMDAC CLOCK & CLOCK- inputs. Can drive 4 RAMDACs. |
| VCLKOUT- | 10 | Output levels equivalent to 10KH ECL circuit operating from single supply. VCLKOUT- is skew-free. |
| ERROUT- | 11 | Error Output: a low signals an error in the Serial Programming Word |
| GND | 12 | Ground |
| INIT0 | 13 | Select power-up initial conditions (LSB) (Internal pull-down) |
| VDD | 14 | +5 volts to I/O Ring |
| LDC | 15 | Load output (TTL compatible). When ENABLE is high, has same timing as LDA output. Can drive up to 4 capacitive loads without buffering. |
| INIT1 | 16 | Select power-up initial conditions (MSB) (Internal pull-down) |
| LDA | 17 | Skew-free Load Outputs (TTL compatible). Generated by dividing VCLKOUT by Div Register (1 or 2). Each output can drive up to 4 capacitive loads without buffering. |
| LDA/2 | 18 | Generated by dividing LDA by two |
| LDA/4 | 19 | Generated by dividing LDA by four. |
| ENABLE | 20 | Synchronous load enable input. Internally synched to LDA, used to start/stop LDC output synchronously. If ENABLE is low, LDC is held low; when high, LDC is free-running. |

Table of Contents

| | |
|---------------------------------------|----|
| • Introduction | 4 |
| • ICD2062A/B Changes from the ICD2062 | 5 |
| • Register Definitions | 6 |
| • Serial Programming Architecture | 9 |
| • Programming the ICD2062A/B | 12 |
| • RAMDAC/VRAM Interface | 16 |
| • Power Management Issues | 19 |
| • Circuit Operation | 20 |
| • PC Board Routing Issues | 22 |
| • Ordering Information | 23 |
| • Device Specifications | 24 |

Introduction

The ICD2062A/B is a clock generator for high-resolution video displays. It uses a low-frequency (and low-cost) reference crystal to produce the following: a 10KH compatible complementary ECL oscillator signal for high-speed video RAMDACs, a high-speed TTL oscillator signal for video RAMs and system logic operation, and the requisite load, control and clock signals to control the loading of data between the CRT controller, VRAM and RAMDACs.

The ICD2062A/B Dual Programmable Clock Generator offers 2 fully user-programmable phase-locked loops in a single package. The outputs may be changed “on the fly” to any desired frequency value in the range 510 KHz to either 135 MHz for the A version or 185 MHz for the B version (VCLKOUT) and 510 KHz to 120 MHz for both versions (MCLKOUT). The ICD2062A/B is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators, particularly where the application requires expensive complementary ECL oscillators.

The Video Clock output may be programmatically divided by 1 or 2 in order to generate the Load Signal, which is further divided by 2 and 4 for clocking video timing logic. A second Load Signal may be synchronously gated in order to enable starting and stopping the clocking of video RAMs. The ICD2062A/B can also configure the pipeline delay of certain RAMDACs (such as the Bt457/458) to a fixed pipeline delay.

Being able to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: $\pm 10\%$) allows worst case evaluations.

ICD2062A/B Changes from the ICD2062

The ICD2062A/B revision of the ICD2062 is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following major modifications have been implemented:

Changes Common to ICD2062A & ICD2062B

- **Enhanced VCO** — The redesigned VCOs generate 30% less jitter than those of previous versions.
- **Increased Frequency Resolution** — 3 additional bits have been added to the CNTL Register to allow an optional pre-divide by 2 on the P Counter. This in effect makes the P Counter 8 bits wide, and thus doubles the effective resolution of the Program Word. Full upward compatibility with existing software is maintained.
- **Glitch-Free Transitions** — Reprogramming the MCLK and the active VCLK registers is now glitch-free; the Reference Frequency is automatically multiplexed to the appropriate output pin during the transition period.
- **Extended Low-Frequency Range** — The lower frequency limit has been extended to 510 KHz as a result of the addition of a +128 value to the Post-VCO Divide Register.
- **New Index Table** — The new VCOs require a change in the Index Table values for the A and the B versions of the ICD2062A/B, due to the different high end frequency limits.

Changes to ICD2062B Only

- **New VCO** — The primary difference between the A and B versions is the design of the internal VCO. The ICD2062B video VCO has been redesigned to support frequencies up to 185 MHz.
- **New Register Initialization ROM** — A new ROM allows the ICD2062B to be initialized to higher default frequencies.

Register Definitions

Register File

The Register File consists of the following registers and their selection addresses:

Register Addressing

| Address | Register | Usage |
|---------|------------|----------------------------|
| 000 | REG0 | Video Clock Register 1 |
| 001 | REG1 | Video Clock Register 2 |
| 010 | REG2 | Video Clock Register 3 |
| 011 | MREG | Memory or I/O Timing Clock |
| 100 | (Reserved) | |
| 101 | DIVREG | Load Divisor Register |
| 110 | CNTL Reg | Control Register |

Register Selection

Video clock output is controlled not only by the SEL0 & SEL1 bits, but also by the OUTDIS $\bar{}$ signal, as follows:

VCLKOUT Selection

| OUTDIS $\bar{}$ | SEL1 | SEL0 | VCLKOUT |
|-----------------|------|------|---------|
| 0 | X | X | High-Z |
| 1 | 0 | 0 | REG0 |
| 1 | 0 | 1 | REG1 |
| 1 | 1 | X | REG2 |

The Memory Clock output is controlled by the OUTDIS $\bar{}$ signal as indicated below:

MCLKOUT Selection

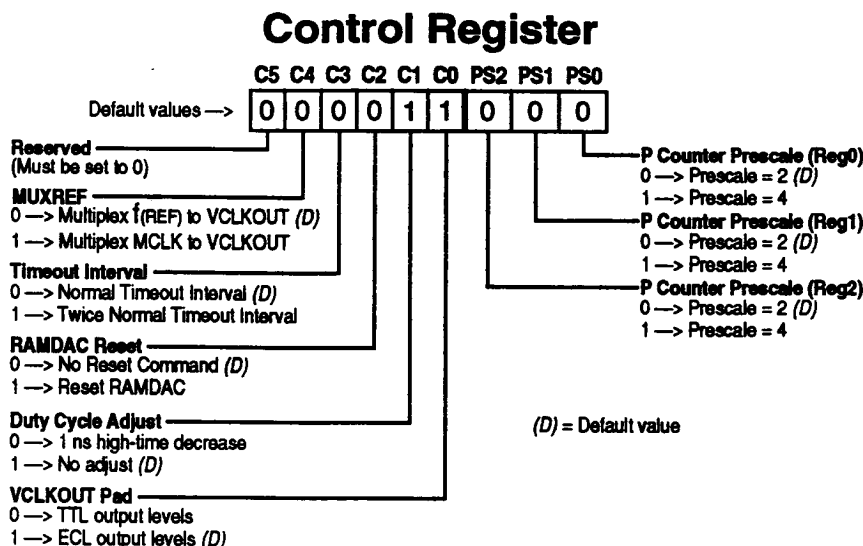
| OUTDIS $\bar{}$ | MCLKOUT |
|-----------------|---------|
| 0 | High-Z |
| 1 | MREG |

The Clock Select pins SEL0 & SEL1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins SEL0 & SEL1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f(\text{REF})$ for an additional timeout interval to give the VCO time to settle to its new value. [The timeout interval in both cases is approximately 5 msec — see the timeout interval spec in the AC Timing Section.]

When a new frequency is being set for MCLK, or if the active VCLK register is being programmed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent from the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See the AC Timing section for further details.).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined as follows:



MUXREF — This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Timeout Interval — The Timeout Interval is normally defined as in the AC Specifications. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, the timeout may be too short. If this control bit is set, the Timeout Interval is doubled.

RAMDAC Reset — This control bit, when set, will cause the ICD2062A/B to issue a RAMDAC reset sequence, which is required by some specific RAMDACs (such as the Bt457/458). For more specifics on this operation, see the paragraph titled *Internal Reset Sequence* in the section titled *RAMDAC/VRAM Interface*. NOTE: This operation will only take place the first time this bit is set.

Duty Cycle Adjust — This control bit causes a 1ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the Threshold Voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

VCLKOUT Pad — This control bit determines whether the VCLKOUT Pad is at ECL or TTL levels. The default is ECL levels. When in TTL mode, the VCLKOUT Pad is nonfunctional, and remains tri-stated.

P Counter Prescale (REG0, REG1, REG2) — These control bits determine whether or not to prescale the P Counter value, which allows "fine tuning" the output frequency of the respective register. Prescaling is explained in more detail in various sections of this Datasheet.

Divide Register Definition

The output signals LDA, LDA/2, LDA/4, and LDC are all a function of the VCLK VCO value divided by the division factor stored in the Divide Register (DIVREG).

DIVREG Division Factors

| D2 | D1 | D0 | Division Factor | Clock Low (cycles) | Clock High (cycles) |
|----|----|----|-----------------|--------------------|---------------------|
| 1 | 0 | X | +1 | 1/2 | 1/2 |
| 1 | 1 | X | +2 | 1 | 1 |
| 0 | X | X | • Reserved • | | |

Register Initialization

The ICD2062A/B Clock Synthesizer has several of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three pixel clock registers are initialized based on the state of the INIT1 and INIT0 pins at power-up. Also, the Memory Clock is initialized based on the INIT pins.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with VDD if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as follows:

Register Initialization — ICD2062A

| INIT1 | INIT0 | MREG | REG0 | REG1 | REG2 |
|-------|-------|--------|--------|--------|--------|
| 0 | 0 | 32.500 | 25.175 | 28.322 | 28.322 |
| 0 | 1 | 40.000 | 25.175 | 28.322 | 28.322 |
| 1 | 0 | 50.350 | 40.000 | 28.322 | 28.322 |
| 1 | 1 | 56.644 | 40.000 | 50.350 | 50.350 |

NOTE: Frequencies in MHz

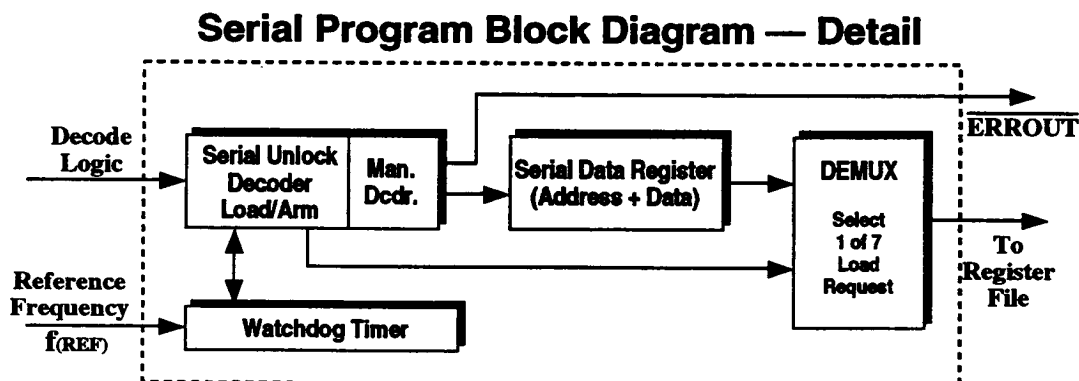
Register Initialization — ICD2062B

| INIT1 | INIT0 | MREG | REG0 | REG1 | REG2 |
|-------|-------|--------|--------|--------|--------|
| 0 | 0 | 32.500 | 25.175 | 28.322 | 28.322 |
| 0 | 1 | 40.000 | 25.175 | 28.322 | 28.322 |
| 1 | 0 | 50.350 | 110 | 135 | 165 |
| 1 | 1 | 56.644 | 110 | 135 | 185 |

NOTE: Frequencies in MHz

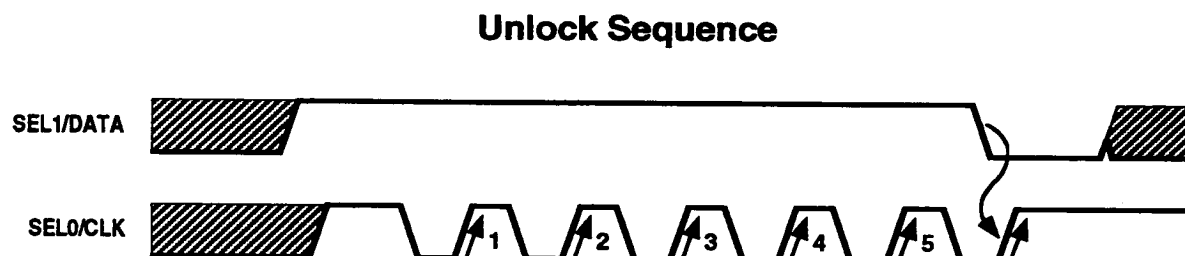
Serial Programming Architecture

The ICD2062A/B programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual function of clock selection and serial programming. The Serial Program Block (See diagram on the first page contains several components: a Serial Unlock Decoder (containing the Unlocking Mechanism and Manchester Decoder), a Watchdog Timer, the Serial Data Register (Serial Reg) and a Demultiplexer to the Register File.



Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence detailed in the following timing diagram:



The initial unlock sequence consists of at least five low-to-high transitions of CLK with DATA high, followed immediately by a single low-to-high transition of CLK with DATA low. Following this unlock sequence, the encoded serial data is clocked into the Serial Data Register.

Watchdog timer

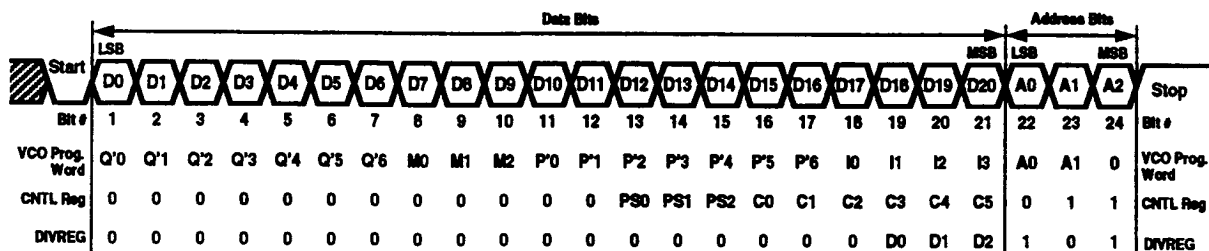
Following any transition of CLK or DATA, the Watchdog Timer is reset and begins counting. Throughout the entire programming process, the Watchdog Timer ensures that rising edges of CLK do not violate the timeout specification (of 2ms — see AC specs). If a timeout does occur, the Lock Mechanism is rearmed and the current data in the Serial Data Register is lost.

Since the VCLK registers are selected by the SEL0 or SEL1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. [Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.]

The Serial Data Register

Serial data is clocked into the Serial Data Register in the following order:

Serial Data Timing



The serial data is sent using a modified Manchester encoded data format. This is defined as follows:

- 1 — An individual data bit is sampled on the rising edge of CLK.
- 2 — The complement of the data bit must be sampled on the previous falling edge of CLK.
- 3 — The Setup and Hold Time requirements must be met on both CLK edges.
- 4 — The unlock sequence, start, and stop bits are not Manchester encoded.

For specifics on timing, see the timing diagram in the Device Specifications Section at the end of this Datasheet.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10] = P'; D[9:7] = Mux; D[6:0] = Q'. [See the section on *Programming the 2061* for more details on the VCO data word.] For the other registers having fewer than 21 bits (DIVREG, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should be set to zero to maintain software compatibility with future enhancements.

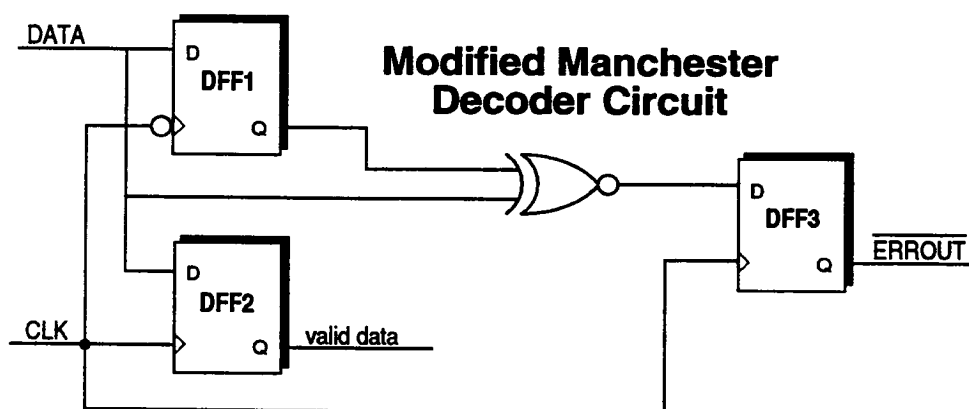
Following the entry of the last address bit, a stop bit or *Load* command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The Unlocking Mechanism then automatically rearms itself following the load. Only when the Watchdog Timer has timed out are the SEL0 & SEL1 pins permitted to return to their normal clock select function.

Note that the Serial Data Register (Serial Reg) which receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command which passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data Register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the Unlocking Mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the Serial Buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the Unlocking Mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the Unlocking Mechanism is rearmed, the Serial Counter reset, all received data ignored, and ERROUT- is asserted.

ERROUT- Operation

The ERROUT- signal is used to inform when a program error has been detected internally by the ICD2062A/B. The signal remains low until the next unlock sequence.

The following circuit shows the basic mechanism used to detect valid and erroneous serial data:



RULE: Must have different values on the rising and falling edges when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The ERROUT- signal is invoked for any of the following error conditions: incorrect start bit; incorrect Manchester encoding; incorrect length of data word; incorrect stop bit.

NOTE: If there is no input pin available on the target VGA controller chip to monitor ERROUT-, a software routine which counts VSYNC pulses to measure output frequency may be used as a determination of programming accuracy.

Programming the ICD2062A/B

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2062A/B has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

Programming Word Bit Fields

| Field | # of Bits | Notes |
|----------------------|-----------|------------------------------|
| Index (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Mux (M) | 3 | |
| Q Counter Value (Q') | 7 | LSB (Least Significant Bits) |

The frequency of the programmable oscillator f_{VCO} is determined by these fields as follows:

$$P' = P - 3 \quad Q' = Q - 2$$

$$f_{VCO} = (2 \cdot f_{REF}) \cdot \frac{P}{Q}$$

where f_{REF} = Reference frequency (between 1 MHz – 60 MHz; typically 14.31818 MHz). NOTE: If a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of f_{VCO} must remain between a minimum and maximum frequency. These limits vary depending on the device version (A or B) and the clock (MCLK or VCLK). See the table in the *Programming Constraints* section for the actual boundary frequencies in each case. For output frequencies below the minimum, f_{VCO} must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Post-VCO Divisor

| M | Divisor |
|-----|---------|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency, f_{VCO} , rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running. When the Index Field is programmed to 1111, VCLK is turned off and both channels run from the same MCLK VCO.

When the Index Field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one *does* want the clocks to run at 2^n multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency (MCLKOUT is thus at the same or a higher frequency than VCLKOUT). This will significantly reduce heterodyne jitter.

--- Index Field (I) Table ---
ICD2062A ICD2062B

| I | VCLK f_{VCO} | MCLK f_{VCO} | VCLK f_{VCO} | MCLK f_{VCO} |
|------|-----------------------|-----------------------|-----------------------|-----------------------|
| 0000 | • Reserved • | • Reserved • | 65.0 – 70.7 | • Reserved • |
| 0001 | 52.0 – 55.0 | 52.0 – 55.0 | 70.7 – 77.8 | 52.0 – 55.0 |
| 0010 | 55.0 – 60.0 | 55.0 – 60.0 | 77.8 – 85.6 | 55.0 – 60.0 |
| 0011 | 60.0 – 68.0 | 60.0 – 68.0 | 85.6 – 88.0 | 60.0 – 68.0 |
| 0100 | 68.0 – 70.0 | 68.0 – 70.0 | 88.0 – 94.2 | 68.0 – 70.0 |
| 0101 | 70.0 – 75.0 | 70.0 – 75.0 | 94.2 – 96.8 | 70.0 – 75.0 |
| 0110 | 75.0 – 80.0 | 75.0 – 80.0 | 96.8 – 106.5 | 75.0 – 80.0 |
| 0111 | 80.0 – 84.5 | 80.0 – 84.5 | 106.5 – 111.7 | 80.0 – 84.5 |
| 1000 | 84.5 – 90.0 | 84.5 – 90.0 | 111.7 – 117.2 | 84.5 – 90.0 |
| 1001 | 90.0 – 95.0 | 90.0 – 95.0 | 117.2 – 122.8 | 90.0 – 95.0 |
| 1010 | 95.0 – 100.0 | 95.0 – 100.0 | 122.8 – 135.1 | 95.0 – 100.0 |
| 1011 | 100.0 – 104.0 | 100.0 – 104.0 | 135.1 – 148.6 | 100.0 – 104.0 |
| 1100 | 104.0 – 110.0 | 104.0 – 110.0 | 148.6 – 160.0 | 104.0 – 110.0 |
| 1101 | 110.0 – 135.0 | 110.0 – 120.0 | 160.0 – 185.0 | 110.0 – 120.0 |
| 1110 | Turn off VCLK | 110.0 – 120.0 | Turn off VCLK | 110.0 – 120.0 |
| 1111 | Mux MCLK > VCLK | 110.0 – 120.0 | Mux MCLK > VCLK | 110.0 – 120.0 |

NOTE: Frequencies in MHz

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides the SERDATA program (Part #ICD/SDATA). SERDATA is a program for the IBM PC which automatically generates the appropriate programming word from the user's reference input and desired output frequencies. SERDATA is also available for the Apple Macintosh as a HyperCard 2.0 stack. Please specify the operating environment when ordering SERDATA.

Programming Constraints

There are five primary programming constraints the user must be aware of:

| ICD2062A | | | ICD2062B | |
|-----------------|------------------------------|--------------------------------|------------------------------|--------------------------------|
| Parameter | Minimum | Maximum | Minimum | Maximum |
| $f_{(REF)}$ | 1 MHz | 60 MHz | 1 MHz | 60 MHz |
| $f_{(REF)} / Q$ | 200 KHz | 1 MHz | 200 KHz | 1 MHz |
| $f_{(VCO)}$ | VCLK: 52 MHz MCLK: 52 MHz | VCLK: 135 MHz MCLK: 120 MHz | VCLK: 65 MHz MCLK: 52 MHz | VCLK: 185 MHz MCLK: 120 MHz |
| Q | 3 | 129 | 3 | 129 |
| P | 4 | 130 | 4 | 130 |

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the aforementioned SERDATA program, these constraints become transparent.

Programming Example — Prescaling = 2 (default)

The following is an example of the calculations SERDATA performs:

Derive the proper programming word for a 39.5 MHz VCLK output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 52 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0110. The result:

$$f_{(VCO)} = 79.0 = (2 \cdot 14.31818 \cdot \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7587$$

Several choices of P and Q are available:

| P | Q | $f_{(VCO)}$ | Error (PPM) |
|----|----|-------------|-------------|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |

Choose (P, Q) = (80,29) for best accuracy (40 PPM).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q - 2 = 29 - 2 = 27 = 0011011 \text{ (1bH)}$$

and the full programming word, W, is:

$$W = I, P', M, Q' = 0110,1001101,001,0011011 = 011010011010010011011$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate address bits and start & stop bits must also be included as defined in the *Serial Programming Scheme* section.

Programming Example — Prescaling = 4

Assume the desired VCLKOUT frequency is 25.174822 MHz. The table below compares the results of using the default prescaling value of 2 and the optional prescaling value of 4:

| Prescale | Actual Freq. | P | Q | Error (PPM) |
|----------|--------------|-----|----|-------------|
| 2 | 25.172286 | 109 | 62 | 101 |
| 4 | 25.174822 | 80 | 91 | 0 |

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2) — which involves loading a Control Word (taking care to preserve the current values of the other Control Bits) — before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency *without* prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

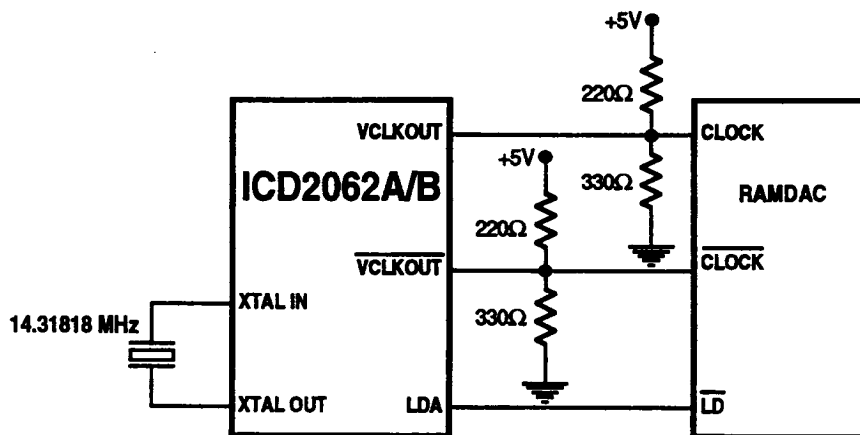
1. Set the Prescale Bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note: Care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

RAMDAC/VRAM Interface

Interfacing to the RAMDAC

The figure below shows how to interface the ICD2062A/B to a RAMDAC. The part should be located as close to the RAMDAC as possible. Termination resistors are needed on the VCLKOUT outputs, and should be located as close as possible to the RAMDAC. For specific information, please refer to the IC DESIGNS Application Note *ECL Outputs*.



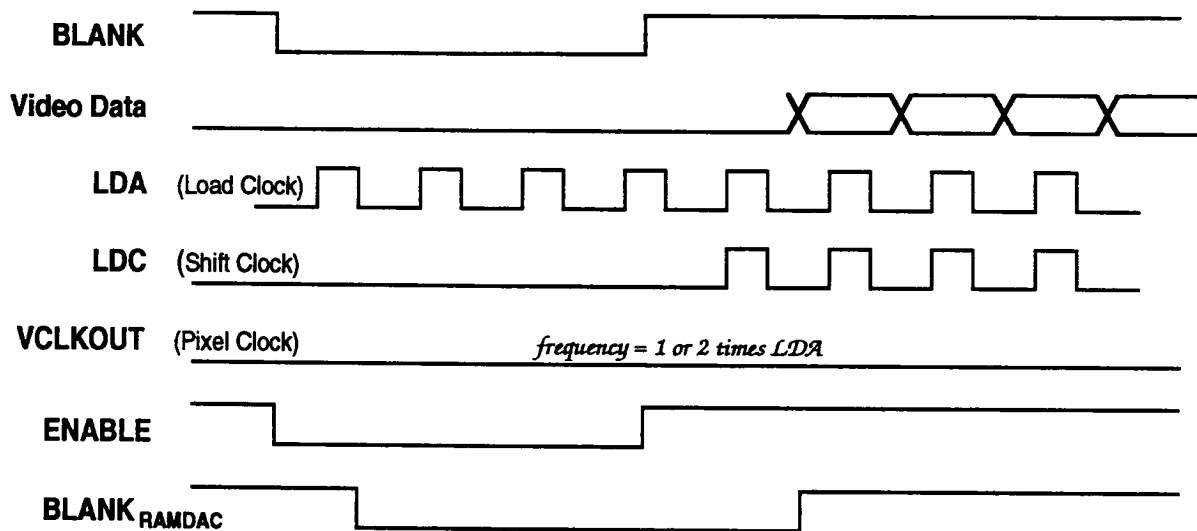
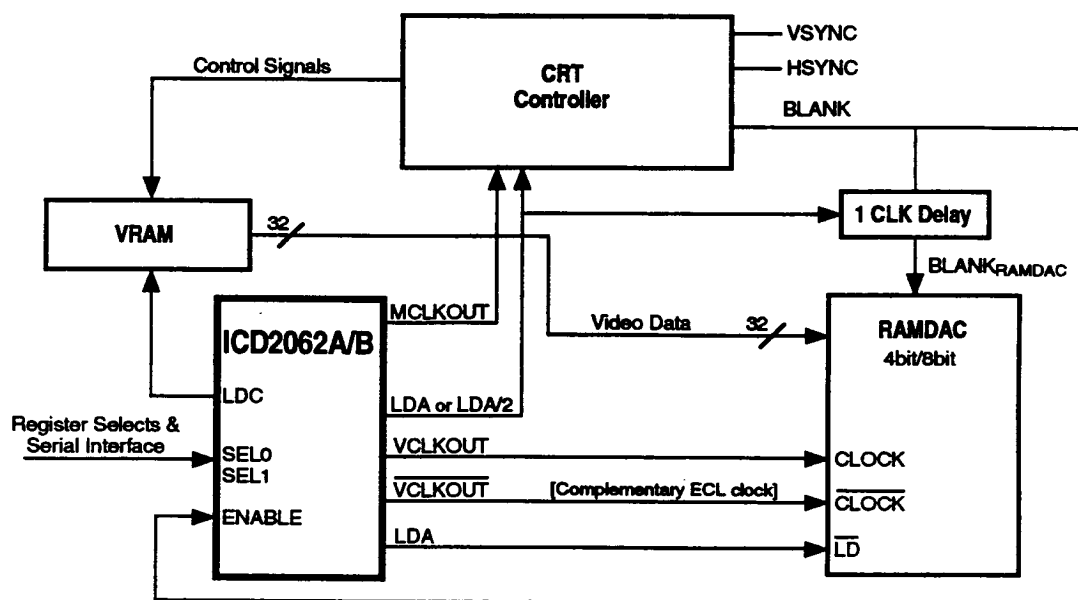
The ICD2062A/B may drive the CLOCK inputs of up to four RAMDACs, if they are located physically adjacent to each other. In this case, only 2 sets of termination resistors should be used, and these should be located nearest the farthest RAMDAC from the ICD2062A/B.

Typical ICD2062A/B Usage

The DIVREG Register holds the divisor, which can be 1 or 2, by which the pixel clock is divided to generate the load signals: LDA, LDA/2 and LDA/4.

The ENABLE input is synchronized internally to LDA; it may be used to start and stop the LDC output synchronously. When ENABLE is low, LDC is held low. When ENABLE is high, then LDC will be free-running and in phase with LDA. This allows the video DRAM shift registers to be non-clocked during the retrace intervals.

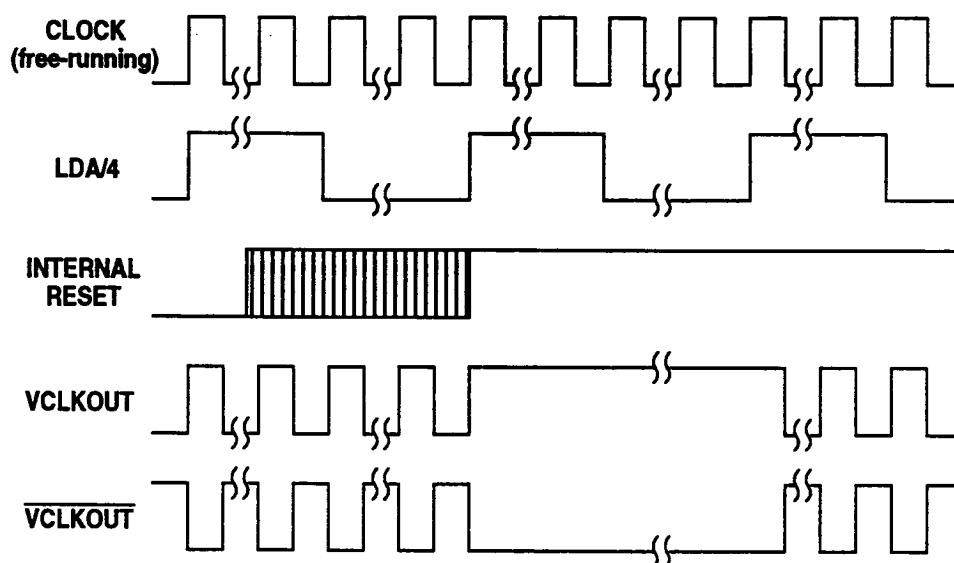
NOTE: For fanouts > 4, LDC needs to be buffered.



Internal RESET Sequence

The internal RESET signal allows the ICD2062A/B to set the RAMDAC pipeline delay to a specific cycle count, depending on the RAMDAC. Reset takes place the first time the CNTL Register's Reset Bit is set. Following the rising edge of LDA/4 after the Reset Bit is set, the VCLKOUT and VCLKOUT- outputs are stopped high and low, respectively; at the next rising edge of LDA/4, these outputs are again allowed to be free-running. The figure below shows the operation of the internal RESET signal:

Internal RESET Timing



Power Management Issues

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \cdot V \cdot f$, where:

I = current, C =load capacitance (max. 25pf),

V = output voltage (usually 5V for TTL pads, 1.5V for ECL pads), and

f = output frequency (MHz).

To calculate total operating current, sum the following:

| | | | |
|----------|---|--------------------------------------|---------------------------------|
| MCLKOUT | → | $C \cdot V \cdot f(\text{MCLKOUT})$ | |
| VCLKOUT | → | $C \cdot V \cdot f(\text{VCLKOUT})$ | ; (ECL pad, $V = 1.5\text{V}$) |
| VCLKOUT- | → | $C \cdot V \cdot f(\text{VCLKOUT-})$ | ; (ECL pad, $V = 1.5\text{V}$) |
| LDA | → | $C \cdot V \cdot f(\text{LDA})$ | |
| LDA/2 | → | $C \cdot V \cdot f(\text{LDA}/2)$ | |
| LDA/4 | → | $C \cdot V \cdot f(\text{LDA}/4)$ | |
| LDC | → | $C \cdot V \cdot f(\text{LDC})$ | |
| Internal | → | 12ma | |

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pf loading, depending on package type.

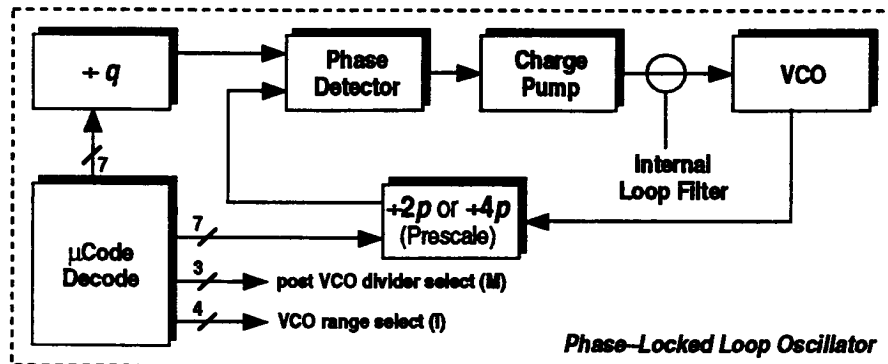
Typical values:

| Frequency | Capacitive | |
|-----------|------------|--------------|
| | Load | Current (ma) |
| low | low | 15 |
| high | low | 50 |
| high | high | 100 |

Circuit Operation

Circuit Description

The ICD2062A/B is designed to use an inexpensive TTL crystal and to generate the high-frequency ECL clock signals required by RAMDACs. The VCLKOUT and VCLKOUT- signals interface directly with the RAMDAC CLOCK and CLOCK- inputs. Output levels of the complementary ECL pads are compatible with 10KH ECL circuitry operating from a single +5V power supply.



Each oscillator block is a classical phase-locked loop connected as shown above. The external input frequency $f(\text{REF})$ goes into a divide-by- n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphic designs.

Frequency Range

The frequency ranges for the video and memory clock outputs are listed in the following table:

| | VCLKOUT | MCLKOUT |
|-----------------|-------------------|-------------------|
| ICD2062A | 510 KHz – 135 MHz | 510 KHz – 120 MHz |
| ICD2062B | 510 KHz – 185 MHz | 510 KHz – 120 MHz |

Output Disable

When the OUTDIS $\overline{}$ pin is asserted (active low), all the output pins except XTAL OUT and ERR $\overline{}$ OUT enter a high impedance mode, to support automated board testing.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. For optimum noise immunity, it is highly recommended that the ICD2062A/B be used with a voltage regulator or Zener diode attached to the AVDD line. A less expensive (and less effective) alternative is to utilize an RC power filter as follows: the analog power pin (AVDD) is bypassed to ground with a 0.1 μ f multi-layer ceramic capacitor and a 2.2 μ f/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22 Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Note, *Power Feed and Board Layout Issues*, for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2062A/B in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2062A/B closest to the device requiring the highest frequency.

FCC & Noise issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note: *Minimizing Radio Frequency Emissions*.

ECL Design Issues

Please refer to the IC DESIGNS Application Note: *ECL Outputs*.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on opposite sides of the die. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2062A/B is inherently stable over temperature, voltage and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2062A/B, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

Ordering Information

| Part Number | Package Type | Temperature Range | Speed Options |
|-----------------|---------------------------|---------------------------------|---------------|
| ICD2062A | P = 20-Pin Plastic DIP | C = Commercial (0°C - +70°C) | -1: 135 MHz |
| | C = 20-Pin Ceramic DIP | | |
| | S = 20-Pin SOIC | | |

| Part Number | Package Type | Temperature Range | Speed Options |
|-----------------|---------------------------|---------------------------------|---------------|
| ICD2062B | P = 20-Pin Plastic DIP | C = Commercial (0°C - +70°C) | -1: 135 MHz |
| | C = 20-Pin Ceramic DIP | | -2: 165 MHz |
| | S = 20-Pin SOIC | | -3: 185 MHz |

Example: order *ICD2062BSC-3* for the ICD2062B, 20-pin plastic SOIC, commercial temperature range device with a top Video Clock frequency range of 185 MHz.

Device Specifications

Electrical Data

Maximum Ratings

| Name | Description | Min | Max | Units |
|-------|------------------------------------|------|-----------|--------|
| VDD | Supply voltage relative to GND | -0.5 | 7.0 | Volts |
| VIN | Input Voltage with respect to GND | -0.5 | VDD + 0.5 | Volts |
| TOPER | Operating Temperature | 0 | +70 | °C |
| TSTOR | Storage Temperature | -65 | +150 | °C |
| TSOL | Max Soldering Temperature (10 sec) | | +260 | °C |
| TJ | Junction Temperature | | +125 | °C |
| PDISS | Package Power Dissipation | | 375 | mWatts |

DC Characteristics

VDD = +5V ±5%

0°C ≤ T_{CASE} ≤ +70°C

| Name | Description | Min | Typ | Max | Units | Conditions |
|-----------------------|------------------------------|---------|-----|---------|-------|-------------------------|
| V _{IH} | High-level input voltage | 2.0 | | | Volts | |
| V _{IL} | Low-level input voltage | | | 0.8 | Volts | |
| V _{OH(ECL)} | ECL High-level output * | VDD-1.0 | | VDD-0.8 | Volts | |
| V _{OL(ECL)} | ECL Low-level output * | VDD-2.0 | | VDD-1.6 | Volts | |
| V _{OH(TTL)} | TTL High-level output ‡ | 4.0 | | | Volts | I _{OH} = -4ma |
| V _{OL(TTL)} | TTL Low-level output ‡ | | | 0.4 | Volts | I _{OL} = 4ma |
| I _{IH} | Input high current | | | 100 | µa | V _{IH} = 5.25V |
| I _{IL} | Input low current | | | -250 | µa | V _{IL} = 0V |
| I _{OZ} | Output leakage current | | | 10 | µa | (tri-state) |
| I _{DD} | Power supply current | 15 | | 100 | ma | |
| I _{DD-TYP} | Power supply curr. (typical) | | 45 | | ma | @ 60 MHz |
| I _{ADD} | Analog power supply current | | | 10 | ma | |
| C _{IN} | Input Capacitance | | | 10 | pf | |
| C _{OUT(ECL)} | Output Capacitance | | 7 | | pf | |

* ECL outputs: VLKOUT, VCLKOUT-

‡ TTL outputs: MCLKOUT, LDA, LDA/2, LDA/4, LDC, ERRROUT-

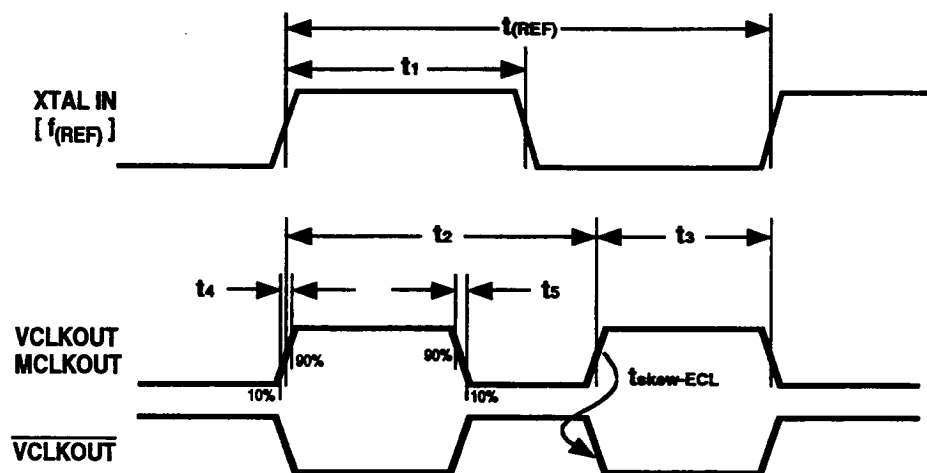
Electrical Data

AC Characteristics

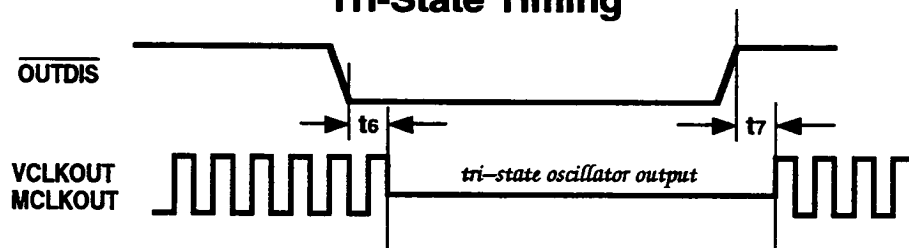
VDD = +5V $\pm 5\%$ 0°C $\leq T_{CASE} \leq +70^\circ\text{C}$

| Symbol | Name | Description | Min | Typ | Max | Units |
|------------------|------------------------|--|---------------------|----------|----------------------------------|-------|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value (Note: for references of other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.) | 1 | 14.31818 | 60 | MHz |
| $t_{(REF)}$ | reference clock period | $1/f_{(REF)}$ | 16.6 | | 1000 | ns |
| t_1 | input duty cycle | Duty cycle for the input oscillator defined as $t_1/t_{(REF)}$ | 25% | | 75% | |
| t_2 | output clock periods | Output oscillator values – ECL – ICD2062A: 7.4 (135 MHz) ICD2062B: 5.4 (185 MHz) – TTL – ICD2062A: 8.3 (120 MHz) ICD2062B: 8.3 (120 MHz) | | | 1960 (510 KHz) 1960 (510 KHz) | ns |
| t_3 | output duty cycle | Duty cycle for the output oscillators (NOTE: for non-ECL outputs, the duty cycle is measured at CMOS threshold levels. At 5 volts, $V_{TH} = 2.5$ Volts.) | 45% | | 55% | |
| t_4 | rise times | Rise time for the output oscillators into a 25 pF load | | | 3 | ns |
| t_5 | fall times | Fall time for the output oscillators into a 25 pF load | | | 3 | ns |
| $t_{skew-ECL}$ | | Skew between the VCLKOUT complementary outputs | | | 1 | ns |
| t_{freq1} | freq1 output | Old frequency output | | | | |
| t_{freq2} | freq2 output | New frequency output | | | | |
| t_A | $f_{(REF)}$ mux time | Time clock output remains high while output muxes to reference frequency | $1/2 t_{(REF)}$ | | $3/2 t_{(REF)}$ | |
| $t_{timeout}$ | timeout interval | Internal interval for serial programming and for VCO changes to settle. If the interval is too short, see the timeout interval section in the control register definition. | 2 | 5 | 10 | ms |
| t_B | t_{freq2} mux time | Time clock output remains high while output muxes to new frequency value | $1/2 t_{freq2}$ | | $3/2 t_{freq2}$ | |
| t_6 | tri-state | Time for the output oscillators to go into tri-state mode after OUTDIS– signal assertion | 0 | | 12 | ns |
| t_7 | clk valid | Time for the output oscillators to recover from tri-state mode after OUTDIS– signal goes high | 0 | | 12 | ns |
| $t_{SKEW-LDA}$ | | VCLKOUT to LDA output skew | 2 | | 6 | ns |
| $t_{SKEW-LDA/2}$ | | LDA to LDA/2 output skew | 0 | 1 | 2 | ns |
| $t_{SKEW-LDA/4}$ | | LDA to LDA/4 output skew | 0 | 1 | 2 | ns |
| $t_{SKEW-LDC}$ | | LDA to LDC output skew | 0 | 1 | 2 | ns |
| t_{EN-SU} | | ENABLE setup time to LDA | 12 | | | ns |
| t_{EN-HD} | | ENABLE hold time to LDA | 0 | | | ns |
| t_{serclk} | | Clock period of serial clock | $2 \cdot t_{(REF)}$ | | 2 | ms |
| t_{SU} | | Setup time | 20 | | | ns |
| t_{HD} | | Hold time | 10 | | | ns |
| t_{ldcmd} | | Load command | 0 | | $t_1 + 30$ | ns |

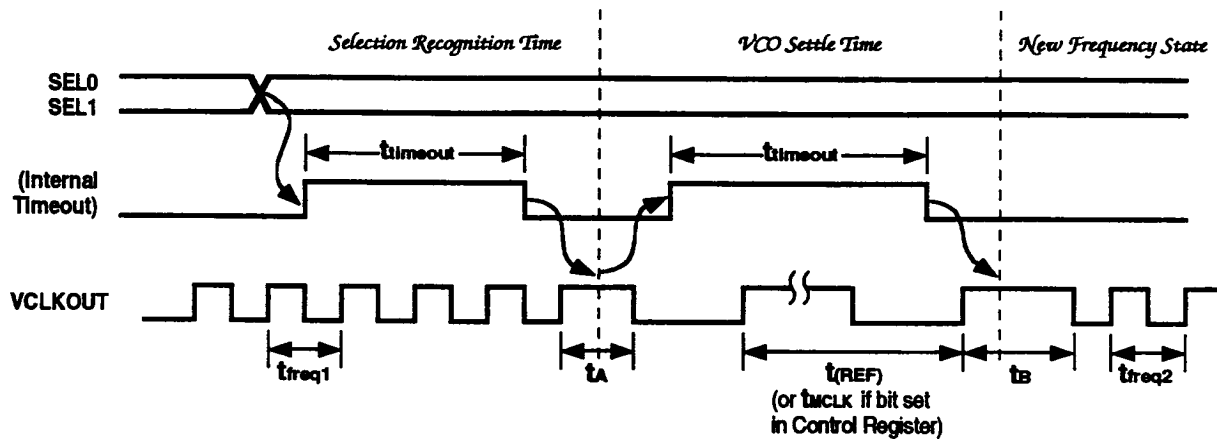
Rise and Fall Times



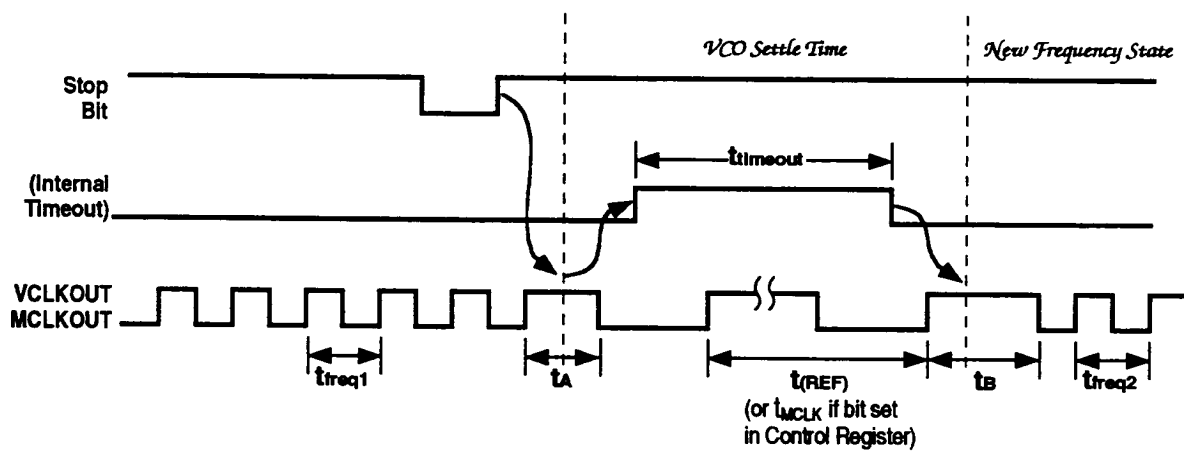
Tri-State Timing



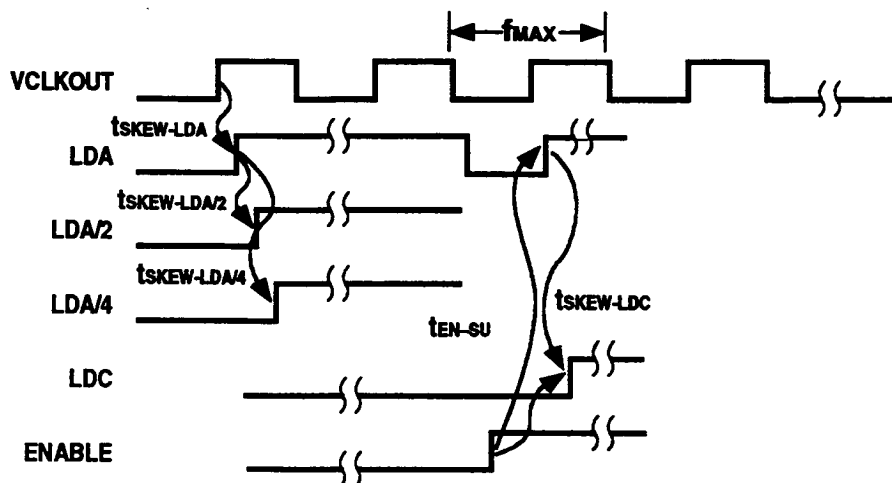
Selection Timing

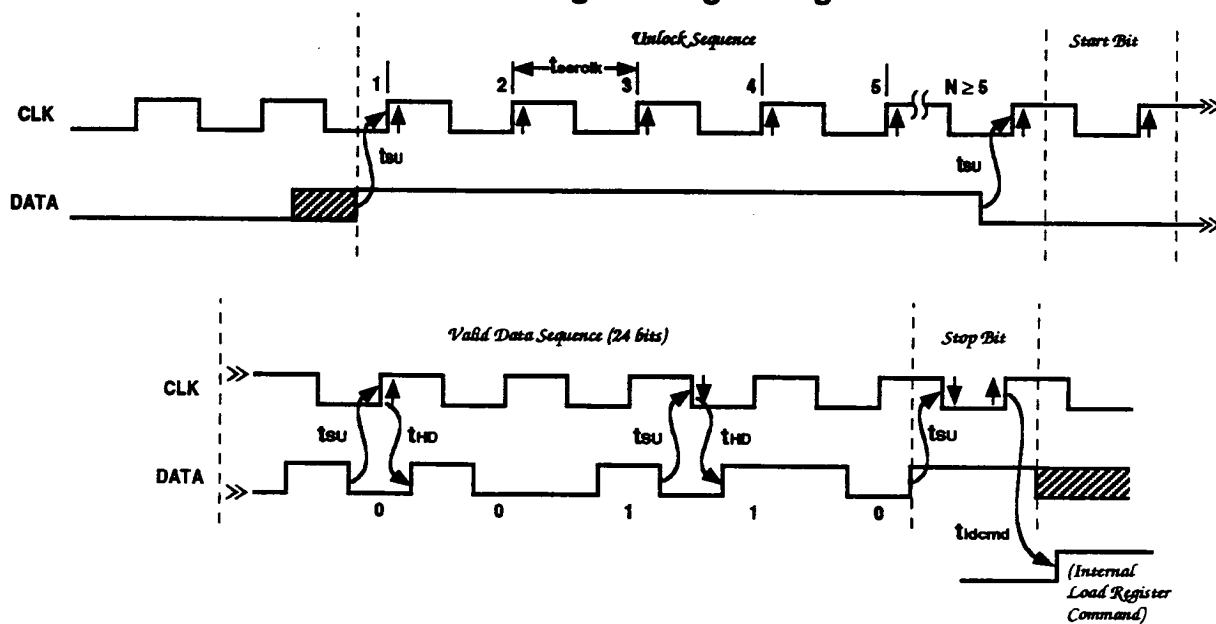


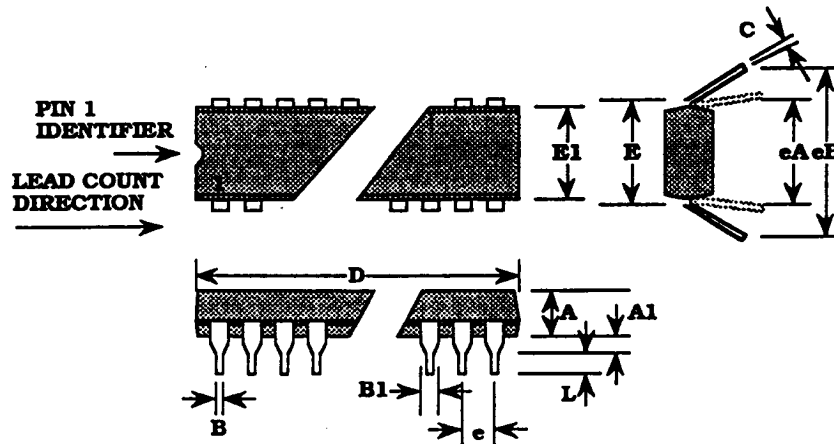
MCLK & Active VCLK Register Programming Timing



RAMDAC / VRAM Interface Timing

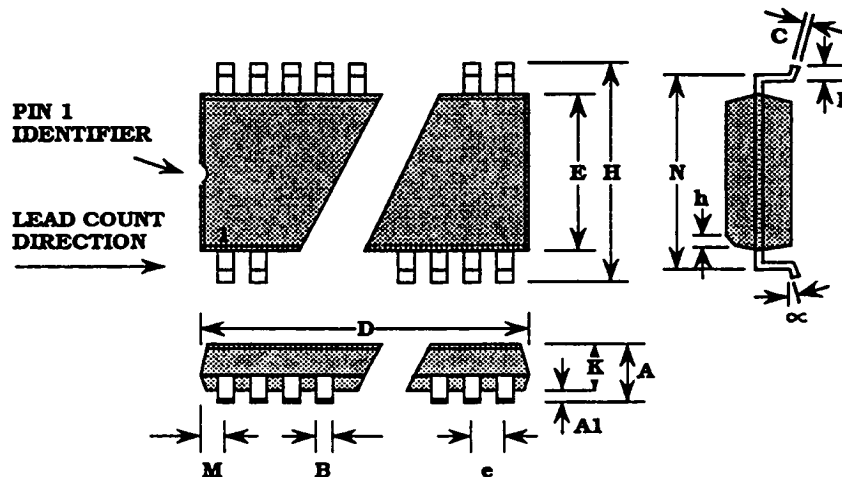


Serial Programming Timing

20-Pin Packages**PDIP Outline**

| Lead Count = 20 | | |
|-----------------|------|-------|
| SYMBOL | MIN | MAX |
| A | .195 | .200 |
| A1 | .015 | — |
| B | .015 | .020 |
| B1 | .050 | .070 |
| C | .008 | .012 |
| D | .925 | 1.030 |
| E | .290 | .310 |
| E1 | .230 | .280 |
| e | .100 | REF |
| eA | .290 | — |
| eB | — | .310 |
| L | .100 | — |

(Dimensions in Inches)

SOIC Outline

| Lead Count = 20 | | |
|-----------------|--------|------|
| SYMBOL | MIN | MAX |
| A | .099 | .104 |
| A1 | .004 | .009 |
| B | .014 | .019 |
| C | .010 | REF |
| D | .505 | .512 |
| E | .294 | .299 |
| e | .050 | TYP |
| H | .402 | .419 |
| h | .025 x | 45° |
| L | .030 | .040 |
| alpha | 0° | 8° |
| K | .088 | .098 |
| M | .020 | .030 |
| N | .335 | .351 |

(Dimensions in Inches)

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