N-Channel 30V (D-S) MOSFET

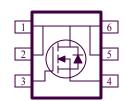
These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are power switch, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low r _{DS(on)} Provides Higher Efficiency and
	Extends Battery Life

- Low Gate Charge
- Fast Switch
- Miniature TSOP-6 Surface Mount Package Saves Board Space

PRODUCT SUMMARY			
V _{DS} (V)	$\mathbf{r}_{\mathrm{DS(on)}}\left(\Omega\right)$	$I_{D}(A)$	
30	0.032	6.3	
30	$0.044 @ V_{GS} = 4.5V$	5.4	





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter			Maximum	Units	
Drain-Source Voltage			30	V	
Gate-Source Voltage			±20	V	
Continuous Drain Current ^a	T _A =25°C	ī	6.3	_	
Continuous Drain Current	$T_A = 25^{\circ} \text{C}$ $T_A = 70^{\circ} \text{C}$	$\Box^{1}D$	5.1	A	
Pulsed Drain Current ^b		I_{DM}	±30		
Continuous Source Current (Diode Conduction) ^a			1.7	A	
D D	T _A =25°C	D	2.0	W	
Power Dissipation ^a	$T_A = 25^{\circ} \text{C}$ $T_A = 70^{\circ} \text{C}$	T ^I D	1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximum	Units		
Manipulation 4. April 1948	t <= 5 sec	R _{THJA}	62.5	°C/W	
Maximum Junction-to-Ambient ^a	Steady-State		110		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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Parameter	Carrala al	Took Conditions	Limits			Unit
rarameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \text{ uA}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \ V, \ V_{GS} = \pm 20 \ V$			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
Zero Gate Voltage Drain Current	1DSS	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α
Drain-Source On-Resistance ^A		$V_{GS} = 10 \text{ V}, I_D = 6.3 \text{ A}$		36	44	mΩ
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 5.4 \text{ A}$		46	64	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 6.3 \text{ A}$		45		S
Diode Forward Voltage	V_{SD}	$I_S = 1.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.80	1.2	V
Dynamic ^b						
Total Gate Charge	Q_g			4.7		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 6.3 \text{ A}$		1.7		пC
Gate-Drain Charge	Q_{gd}			1.4		
Turn-On Delay Time	$t_{d(on)}$			16		
Rise Time	$t_{\rm r}$	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega, I_D = 1 \text{ A},$		5		
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 10 \text{ V}$		23		ns
Fall-Time	t_{f}			3		
Source-Ddrain Reverse Recovery Time	t _{rr}	$I_F = 1.7 \text{ A}, \text{ di/dt} = 100 \text{ A/uS}$		41		

Notes

- a. Pulse test: $PW \le 300us duty cycle \le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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