PACE 1757M/ME
COMPLETE EMBEDDED CPU SUBSYSTEM

PRELIMINARY

FEATURES

Implements complete MIL-STD-1750A ISA including optional MMU, MFSR, and BPU functions.

- **Two throughput options:**
  P1757M 2.5MIPS USAF Dais Mix (Inc. Flt. Pt.) @40MHz
  P1757ME 3.6MIPS USAF Dais Mix (Inc. Flt. Pt.) @40MHz
- **All MIL-STD-1750A data formats and address types implemented.**
- **P1757ME includes additional matrix and vector instructions to enhance throughput in navigation, DSP transcendental, and other complex algorithms.**
- **Error detection and correction and parity bit provided.**
- **Separate high drive external address & data busses.**
- **10MHz data rate at 40MHz CPU clock**
- **System support functions included in P1757M:**
  - Arbitrator for use in tightly coupled multiprocessor design. Bus control provided to aid in implementation of multiprocessor systems.
  - MIL-STD- 1 750A timers A & B, programmable watch dog timer and programmable bus time-out function.
  - Start up ROM support per MIL-STD-1750A.
  - DMA support for logical and physical memory addresses.
  - Programmable memory and I/O data wait state genertion permits up to four different memory speeds in the same system.
  - Programmable address wait states.
  - Sixteen levels of interrupts are provided per MIL-STD-1750A. Interrupts can be either edge- or level-sensitive.
- **Fault detection and handling**
  - Programmable detection of unimplemented memory or illegal I/O addresses.
  - Full implementation of MIL-STD-1750A fault register.
  - External address error detection.
- **Testability and diagnostics.**
  - First failing address and data registers.
  - Built in test – runs automatically at power on and after each reset. All hardware blocks and external busses examined. Hardware pass/fail for catastrophic failures. Status register indicates failed test.
  - Console operating mode which allows operator to examine and change contents of registers within the CPU, any system memory location, or the I/O subsystems.
- **Single 144-pin Quad straight lead or Gullwing** 1.5 square inches of board surface.
- **Operating temperature range – 55 to +125°C; single 5V ± 10% Vcc power supply; power dissipation <1.9W (worst case at 40 MHz).**

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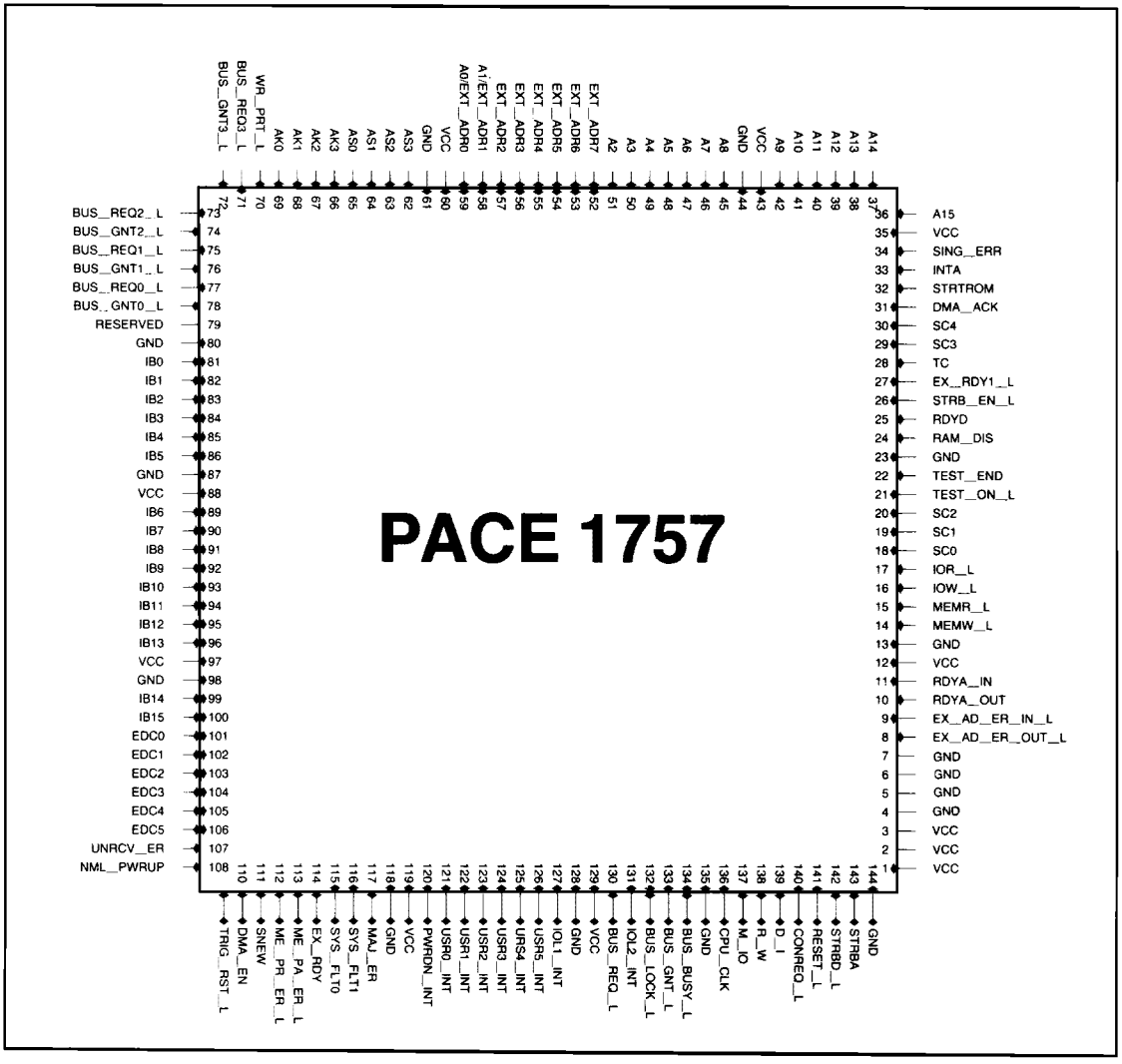
DESCRIPTION

All function srequired for a complete MIL-STD 1750A embedded CPU subsystem are in this single VLSI microcircuit occupying 1.5 square inches of board space with less than 1.9 watts of power dissipation at 40 MHz. Performance's PR1757M/ME is a complete, single package, 3.6 MIPS subsystem solution to embedded processor requirements.

The PACE 1757M uses the application-proven PACE 1750A microprocessor, the PACE1753, PACE1754, or the enhanced PACE1750AE microprocessor, which has additional instructions that provide high throughput for transcendental functions, navigational algorithms, and DSP functions. The PACE 1750AE is an architectural enhancement of the PACE 1750A.

PACE 1757 PINOUT



AC/DC ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

(Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power	-55°C to +125°C
Vcc Pin Potential to Ground Pin	-0.5V to 7.0V
Input Voltage	-0.5V to Vcc + 0.5V
Input Current	-30 mA to 5 mA
Voltage Applied to Inputs	-0.5V to Vcc + 0.5V
Current Applied to any Output	100 mA
Power Dissipation	2.5 Watts
ΘJA	35°C/W

RECOMMENDED OPERATING CONDITIONS

Grade	Case Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V+/- 10%
Commercial	0°C to +70°C	0V	5.0V+/- 10%

DC ELECTRICAL SPECIFICATIONS

(Over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	Input HIGH Level	2.0		V_{CC}+0.5	V	
V_{IL}	Input LOW Level[2]	-0.5		0.8	V	
V_{CD}	Input clamp diode voltage			-1.2	V	I_{IN} =-18mA V_{CC}= Min
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} =-8mA
		V_{CC}-0.2			V	I_{OH} =-300µA V_{CC}= Min
V_{OL}	Output LOW Voltage Except A_0-A_{15}, EXT ADR_0-EXT ADR_7			0.5	V	I_{OL}=8mA
				0.2	V	I_{OL} = 300µA V_{CC}= Min
	Output LOW Voltage A_0-A_{15}, EXT ADR_0-EXT ADR_7			0.5	V	I_{OL}=20mA
				0.2	V	I_{OL}=300µA V_{CC}= Min
I_{IH}	Input HIGH Current except IB_0-IB_{15}, EDC_0-EDC_5,$\overline{\text{BUS BUSY}}$, $\overline{\text{BUS LOCK}}$, EXT ADR_0-EXT ADR_7			10	µA	V_{IN}=Vcc V_{CC}=Max
	Input HIGH Current IB_0-IB_{15}, EDC_0-EDC_5,$\overline{\text{BUS BUSY}}$, $\overline{\text{BUS LOCK}}$, EXT ADR0-EXT ADR_7			50	µA	V_{IN}=Vcc V_{CC}=Max

DC ELECTRICAL SPECIFICATIONS (Continued)

(Over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
I_{IL}	Input LOW current except IB_0-IB_{15}, EDC_0-EDC_5, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$, EXT ADR_0-EXT ADR_7, TEST ON			-10	µA	V_{IN}=GND V_{CC}=Max
	Input LOW current TEST ON			-500	µA	$V_{IN}=V_{CC}$ Vcc=Max
	Input LOW current IB_0-IB_{15}, EDC_0-EDC_5, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$, EXT ADR_0-EXT ADR_7			-50		
I_{OZH}	Output 3-state current Except SINGERR, STRBA			50	µA	V_{OUT}=2.4V V_{CC}=Max
	Output 3-state current SINGERR, STRBA			500		
I_{OZL}	Output 3-state current Except $\overline{STRBD}$			-50	µA	V_{OUT}=0.5V V_{CC}=Max
	Output 3-state current $\overline{STRBD}$			-500		
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels)			80	mA	V_{IN}<0.2V or >V_{CC}-0.2V,f=0Hz Outputs open V_{CC}=Max
I_{CCQT}	Quiescent Power Supply Current (TTL Levels)			210	mA	V_{IN}=3.4V, All inputs, f=0Hz Outputs open V_{CC}=Max
I_{CCD} TTL	Dynamic Power Supply Current f = 20 MHz			280	mA	V_{IN}<0.8V or >3.4V, Outputs open, V_{CC}=Max
	f = 30 MHz			310		
	f = 35 MHz			325		
	f = 40 MHz			340		
I_{CCD}	Dynamic Power Supply Current f = 20 MHz			150	mA	V_{IN}<0.2V or >V_{CC} -0.2V Outputs open, V_{CC}=Max
	f = 30 MHz			180		
	f = 35 MHz			195		
	f = 40 MHz			210		
I_{OS}	Output Short Circuit Current (one output shorted at a time)	-25			mA	V_{OUT}=GND V_{CC}=MAX[1]
C_{IN}	Input Capacitance[3]		5		pF	Inputs Only
C_{OUT}	Output Capacitance[3]		9		pF	Outputs(includes I/O Buffers)

Note 1: Duration of the short should not exceed one second.
Note 2: VIL=-3.0V for pulse widths less than or equal to 20ns.
Note 3: This parameter is set by design and not tested.

TIMING GENERATOR STATE DIAGRAMS

Two separate and almost independent state diagrams may be used to describe the PACE1757M machine cycle.

The Execution Unit performs according to a cycle of three states represented by Diagram A (the A machine) and the External Bus Unit follows a minimum cycle of four states, indicated in Diagram B (the B machine).

Referring to Diagram A, the paths are defined as follows for the Execution Unit:

(0) External Reset true

(1) External Reset false

(2) ALU wait or Bus wait.

(3) ALU Branch false

(4) ALU Branch true

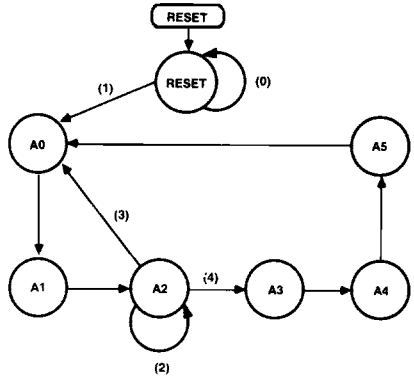


Diagram A

Diagram B defines the paths for the External Bus as follows:

(0) External Reset false

(8) Bus Req. false

(9) Bus Req. true and Bus Av. true

(10) Bus Req. true and Bus Av. false

(11) Bus Av. false

(12) Bus Av. true

(13) RDYA false

(14) RDYA true

(16) RDYD false

(17) RDYD true and Bus Req. true and Bus Av true

(18) RDYD true and Bus Req. false

(19) RDYD true and Bus Req. true and Bus Av false

(20) Bus Req. true and Bus Av. true

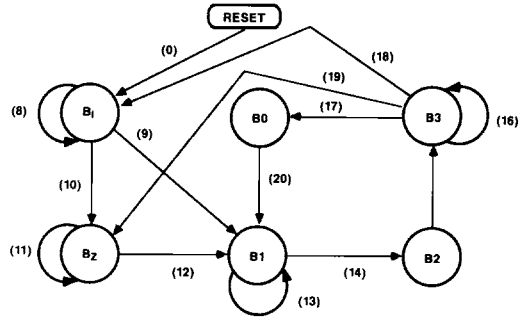


Diagram B

NOTE:
Bus Av = Bus grant and Bus not busy and Bus not locked.

DIFFERENCES BETWEEN THE PACE1757M AND PACE1757ME

The PACE1757ME, which uses the P1750AE CPU, achieves a 41% boost in performance (in clock cycles) over the PACE1757M, which uses the P1750A CPU. This reduction in clocks per instruction is because of three architectural enhancements:

1. The inclusion of a 24 x 24 Multiply Accumulate (MAC) array.
2. A reduction in non-bus cycles to 2 clocks (bus cycles remain at 4 clocks to maintain full compatibility with CPU's peripheral chips).
3. Branch calculation logic.

The table below shows how the MAC improves all multiply operations — both integer and floating point — by 477% to 760%.

Instruction	PACE1750AE		PACE1750A		Gain # Clks (%)
	Clocks	Execution Time (40 MHz)	Clocks	Execution Time (40 MHz)	
Integer Add/Sub	4	100ns	4	100ns	—
Double Precision Integer Add/Sub	6	150ns	9	225ns	50
Integer Multiply	4	100ns	23	575ns	575
Double Precision Integer Add/Sub	9	225ns	69	1725ns	760
Floating Add/Sub	18	450ns	28	700ns	55
Extended Floating Add/Sub	34	850ns	51	1225ns	50
Floating Multiply	9	225ns	43	1075ns	477
Extended Floating Point Multiply	17	425ns	96	2400ns	564
Branch (Taken)	8	200ns	12	300ns	50
Branch (Not Taken)	4	100ns	4	100ns	—
Flt'g' Point Polynomial Step (Mul+Add/Sub)	27	675ns	71	1775ns	263
Ext Flt'g' Point Polynomial Step (Mul/Sub)	51	1275ns	147	3675ns	2400
DAIS Mix (MIPS)	—	3.56	—	2.52	41/59

PACE1757ME BUILT IN FUNCTIONS

A core set of additional instructions have been included in the PACE1757ME. These instructions use the Built- In Function (BIF) opcode space. The objective of these new opcodes is to enhance the performance of the PACE in critical application areas such as navigation, DSP, transcendentals and other LINPAK and matrix type instructions. Below is a list of the BIFs and their execution times (N = the number of elements in the vector being processed).

Instruction	Mnemonic	Address Mode	Number of Clocks	Notes
Memory Parametric Dot Product—Single	VDPS	4F3(RA)	10 + 8 • N	Interruptable
Memory Parametric Dot Product—Double	VDPD	4F1(RA)	10+16 • N	Interruptable
3 x 3 Register Dot Product	R3DP	4F03	6	
Double Precision Multiply Accumulate	MACD	4F02	8	
Polynomial POLY	4F06	7 • N - 2		
Clear AccumulatorCLAC	4F00	4		
Store Accumulator (32-Bit)	STA	4F08	7	
Store Accumulator (48-Bit)	STAL	4F04	11	
Load Accumulator (32-Bit)	LAC	4F05	9	
Load Accumulator Long (48-Bit)	LACL	4F07	9	
Move MMU Page Block	MMPG	4F0F	16+8 • N	Privileged
Load Timer A Reset Register	LTAR	4F0D	4	
Load Timer B Reset Register	LTBR	4F0E	4	

TIMING GENERATOR STATE DIAGRAMS

Two separate and almost independent state diagrams may be used to describe the PACE1757ME machine cycle.

The Execution Unit performs according to a cycle of three states represented by Diagram A (the A machine) and the External Bus Unit follows a minimum cycle of four states, indicated in Diagram B (the B machine).

Referring to Diagram A, the paths are defined as follows for the Execution Unit:

(0) External Reset true

(1) External Reset false

(2) ALU wait or Bus wait.

(3) ALU Branch false

(4) ALU Branch true

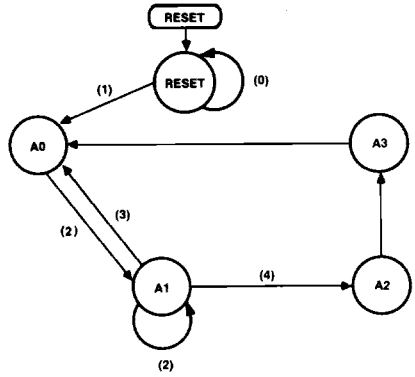


Diagram A

Diagram B defines the paths for the External Bus as follows:

(0) External Reset false

(1) No Internal Bus Req.

(2) Internal Bus Req.

(3) Bus Busy or No Bus Grant

(4) Bus Grant and Not Busy or Bus Locked by CPU

(5) RDYA false

(6) RDYA true

(7) RDYD false

(8) RDYD true, and no Internal Bus Request

(9) RDYD true, Internal Bus Request pending

(10) Bus Locked by CPU and No Internal Request

(11) Bus Locked by CPU Internal Req.

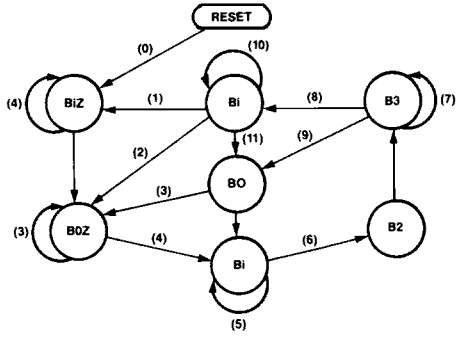


Diagram B

NOTE:
Bus Av = Bus grant and Bus not busy and Bus not locked.

SIGNAL PROPAGATION DELAYS

Symbol	Description	20MHz		30MHz		35MHZ		40MHZ	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$TC(BR)_L$	$\overline{BUS\ REQUEST}$		33		25		22		22
$TC(BR)_H$			33		25		22		22
TBG_V (C)	$\overline{BUSGRANT}$ - Setup	5		5		5		5	
$TC(BG)_X$	$\overline{BUSGRANT}$ - Hold	5		5		5		5	
$TC(BB)_L$	$\overline{BUS\ BUSY}$		25		24		22		20
$TC(BB)_H$			25		20		18		17
TBB_V (C)	$\overline{BUS\ BUSY}$ - Setup	5		5		5		5	
$TC(BB)_X$	$\overline{BUS\ BUSY}$ - Hold	5		5		5		5	
$TC(BL)_L$	$\overline{BUS\ LOCK}$		30		25		23		21
$TC(BL)_H$			30		20		19		17
TBL_V (C)	$\overline{BUS\ LOCK}$ - Setup	5		5		5		5	
$TC(BL)_X$ (IN)	$\overline{BUS\ LOCK}$ - Hold	5		5		5		5	
$TC(ST)_V$	M/$\overline{IO}$		30		25		23		20
	R/$\overline{W}$		30		25		23		20
	AS0:AS3, AK0:AK3, D/$\overline{I}$		25		20		20		20
$TC(ST)_X$	M/$\overline{IO}$, R/$\overline{W}$, AS0:AS3, AK0:AK3, D/$\overline{I}$	0		0		0		0	
$TC(SA)_H$	STRBA		22		17		16		16
$TC(SA)_L$			22		17		16		16
$TSA_L(IBA)_X$	Address Hold from STRBA(L)	5		5		5		5	
TRA_V(C)	RDYA – Setup	5		5		5		5	
$TC(RA)_X$	RDYA – Hold	5		5		5		5	
$TC(SDW)_L$	$\overline{STRBD}$		22		17		16		14
$TC(SD)_H$			22		17		16		14
$TFC(SDR)_L$			22		17		16		14
$TIBD_X(SDR)_H$		0		0		0		0	
$TSDW_H(IBD)_X$		30		25		21		17	
$TSD_L(SD)_H$(Write)		40		26		23		20	
$TRD(RD)_X$	RDYD – Setup	5		5		5		5	
$TC(RD)_X$	RDYD – Hold	5		5		5		5	
$TC(IBA)_V$	IB0:IB15		30		25		23		20
$TFC(IBA)_X$		0		0		0		0	
$TIBDR_V$(C)	– Setup	5		5		5		5	
$TC(IBD)_X$(Read)	– Hold	5		5		5		5	
$TC(IBD)_X$(Write)	DATAVALID (OUT)	0		0		0		0	
$TFC(IBD)_V$			30		25		23		20
TC(SNW)	SNEW		30		26		24		22
TFC(TGO)	$\overline{TRIGO\ RST}$		30		26		24		22
$TRST_L(DMA\ EN)_L$	DMA ENABLE		40		35		33		30
TC(DME)			40		35		33		30
TFC(NPU)	NORMAL POWER-UP		40		35		33		30
TC(ER)	CLK TO MAJER (UNRCV ER)		60		50		47		45
$TRST_L$(NPU)	RESET		50		40		35		30
$TREQ_V$(C)	$\overline{CON\ REQ}$	0		0		0		0	
$TC(REQ)_X$		10		10		10		10	
$TF_V(BB)_H$	LEVEL SENSITIVE FAULTS	5		5		5		5	
$TBB_H(F)_X$		5		5		5		5	
TIR_V(C)	IOL 1/2 INT. USR $\overline{INT}$ (0:5) - Setup	0		0		0		0	
$TC(IR)_X$	PWRDN INT. LEVEL SENSITIVE – HOLD	10		10		10		10	
$TRST_L(TRST_H)$	RESET PULSE WIDTH	25		20		18		15	
$TC(XX)_Z$	CLK TO TRI-STATE		22		17		15		13

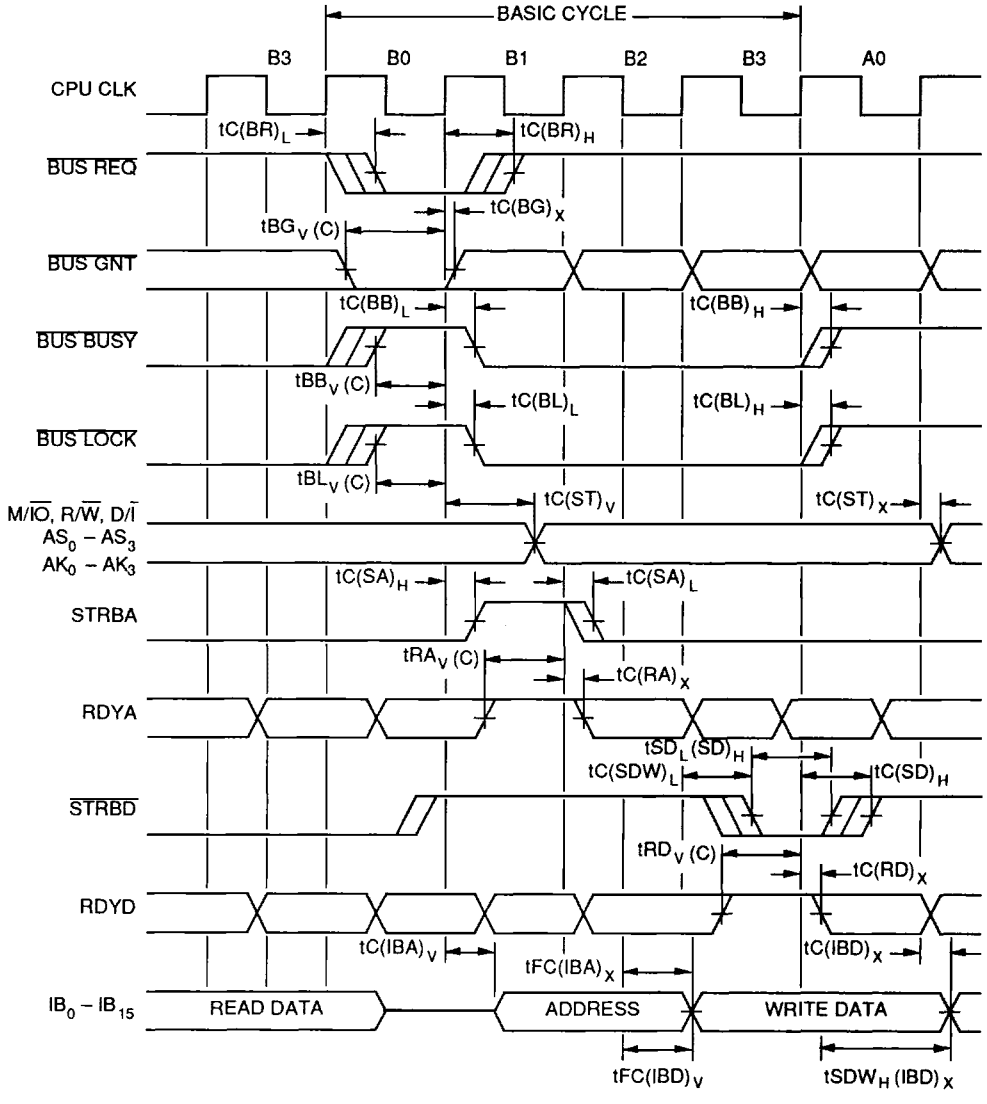
Note 1: Units = ns

SIGNAL PROPAGATION DELAYS (cont'd)

		20MHz		30MHz		35MHZ		40MHZ	
Symbol	**Description**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
TD/I(EXT ADR)$_V$	MMU Cache Hit		25		23		23		23
TSTRBD(EXT ADR ER)	External Address Error		25		20		18		16
TIBD$_V$(EDC GEN)$_V$	Error Connection Write Cycle		30		25		24		23
TC(GNT)	Arbiter Priority Transition		35		25		22		18
TC(RDYA)	Address Ready		30		25		21		17
TIBDIN(MEM PAR ER)	Parity Mode		34		30		28		25
TC(MEM PRT ER)	Memory Protect Error		50		45		43		40
$\overline{\text{TSTRBD (WR PROT)}}$	Write Protect Cache Hit		25		20		18		16
TC(WR PROT)I	Write Protect Cache Miss		25		22		20		18
TD/I(PROT FLAG)	Cache Hit (BPU Protection Error)		40		45		42		40
TD/I(PROT FLAG)	Cache Hit (MMU Key-Lock Error)		40		35		33		30
TC(PROT FLAG)	Cache Hit (BPU Protection Error)		25		35		33		30
TC(PROT FLAG)	Cache Hit (MMU Key-Lock Error)		25		20		20		20
TC(EXT ADR)$_V$	Clock to EXT Address Valid (Miss)		32		30		27		23
TFC(IB OUT)$_V$	Clock to EXT Address Valid (Miss)		30		25		25		25
$\overline{\text{TEX RDY1}}$(RDYD)	Ready Data		28		24		23		21
$\overline{\text{TEX RDY}}$(RDYD)	Ready Data		16		13		12.5		11.5
TC (RDYD)$_V$	Ready Data		28		22		19		16
TSTRBAh(A)$_V$	Address Valid		29		21		20		19
TIBA$_V$(A)$_V$	Address Valid		31		22		21		20
TFC (R)$_L$	Read Strobes		24		18		15		12
TSTRBD$_H$(R)$_H$	Read Strobes		24		18		15		12
TSTRBD$_H$(W)$_L$	Write Strobes		26		20		18		15
TSTRBD$_L$(W)$_H$	Write Strobes		26		20		18		15
TSTRBD(STRTROM)	Start-Up ROM		26		20		18		15
TC(TIM CLK)	Timer Clock		30		25		23		20
TEXT AD(FC B3)	Extended Address Set-Up	10		10		10		10	
TF(F), TI(I)	Edge Sensitive Pulse Width	5		5		5		5	
t_r, t_f	Clock Rise and Fall Time		5		5		5		5

Units = ns

MINIMUM WRITE BUS CYCLE TIMING DIAGRAM



Note: All measurements of delay times on active signals relate to the 1.5 Volt level.
All timing parameters are composed of three elements as follows:

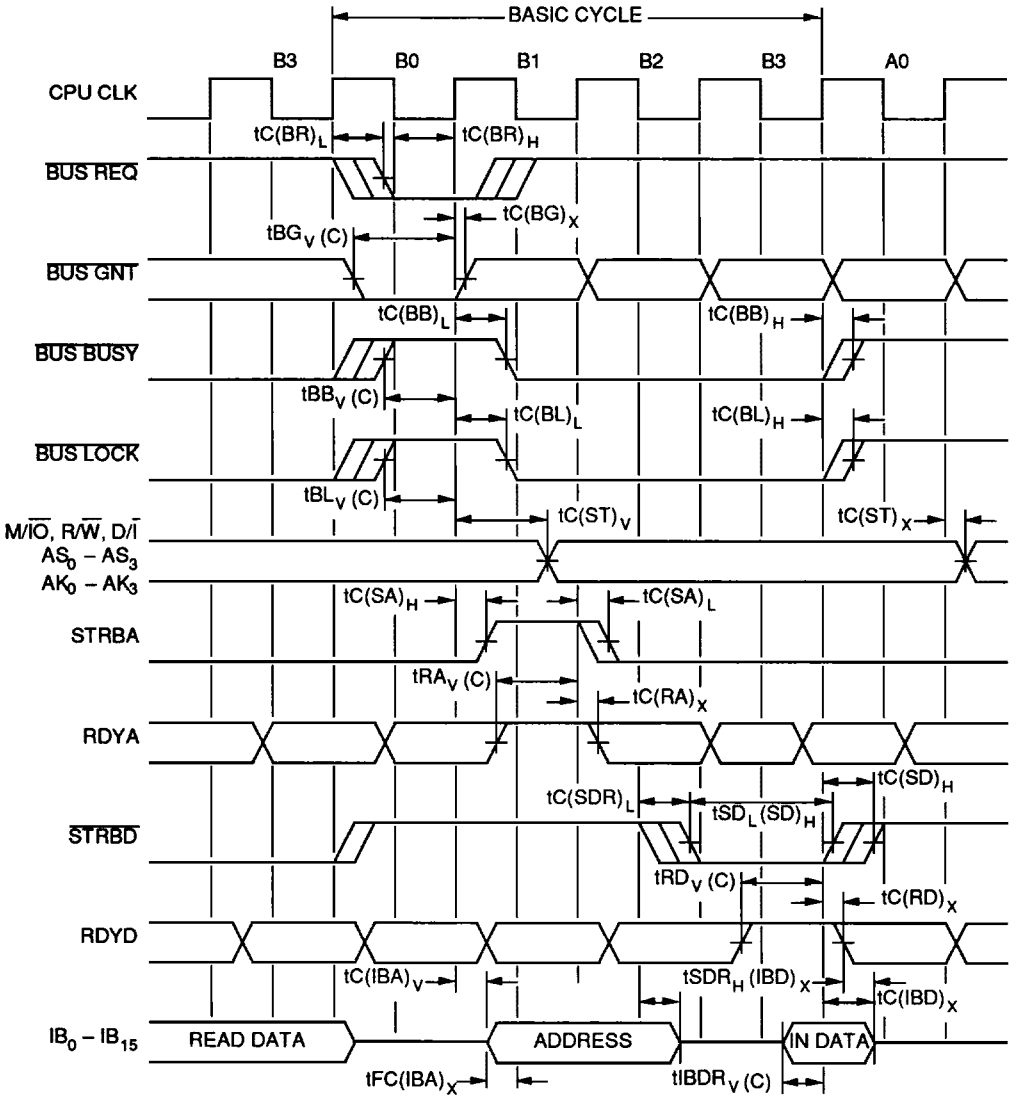
- the first, the letter T, stands for Timing,
- the second element represents the "from" signal, and
- the third element (in parenthesis) indicates the "to" signal.

When the CPU clock is one of the signal elements, either the rising edge "E" or the falling edge "FC" is referenced. When other signals are used as elements, an additional lower case suffix follows to indicate the *final* logical level of the signal. Suffixes are defined as follows:

L = LOW, H = HIGH, v = valid, z = Tri-State, x = Don't Care, zH = Tri-State to High, LH = Low to HIgh.

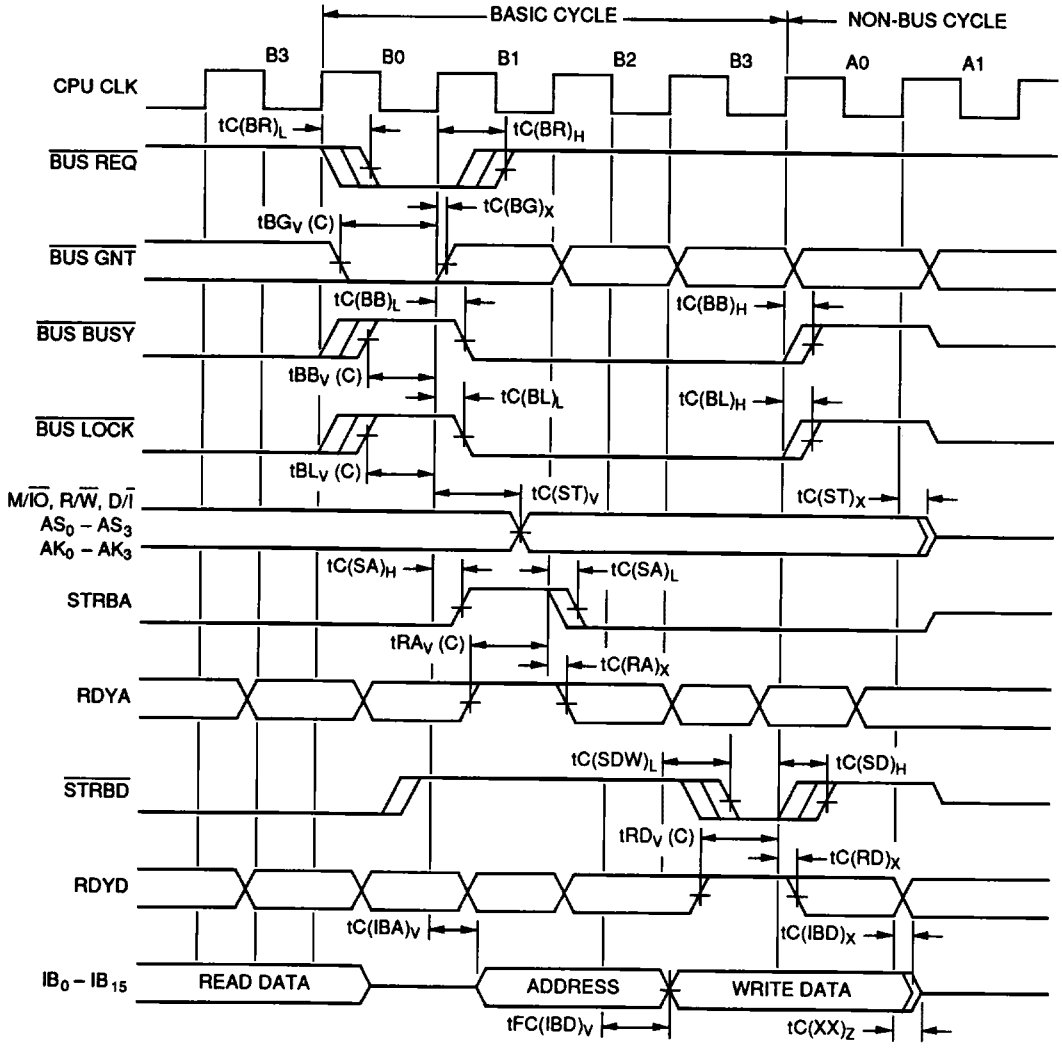
Signal names associated with only the Read Cycle end with a "R", whereas the ones associated with only the write cycle end with a "W."

MINIMUM READ BUS CYCLE TIMING DIAGRAM



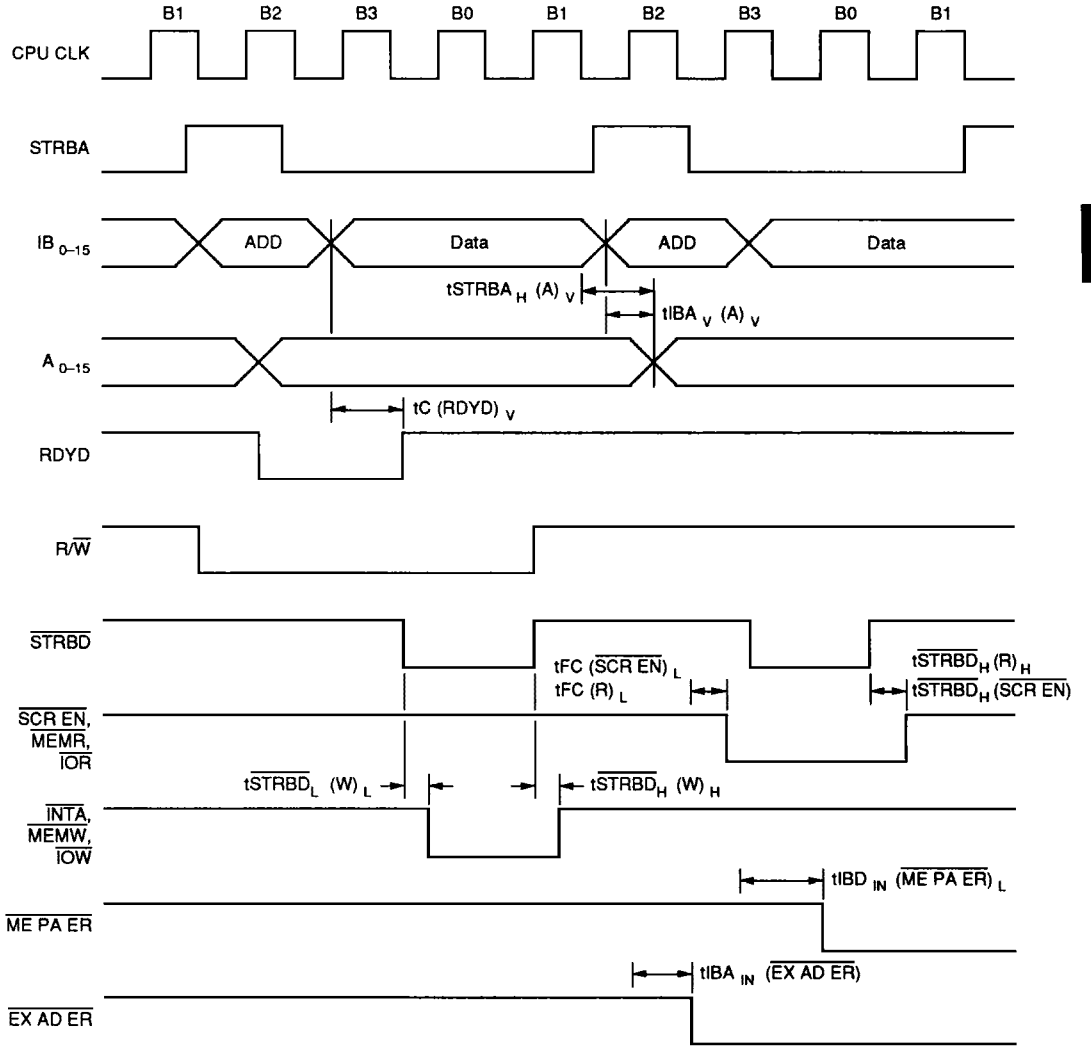
Note: All measurements of delay times on active signals relate to the 1.5 Volt level.

MINIMUM WRITE BUS CYCLE, FOLLOWED BY A NON-BUS CYCLE, TIMING DIAGRAM



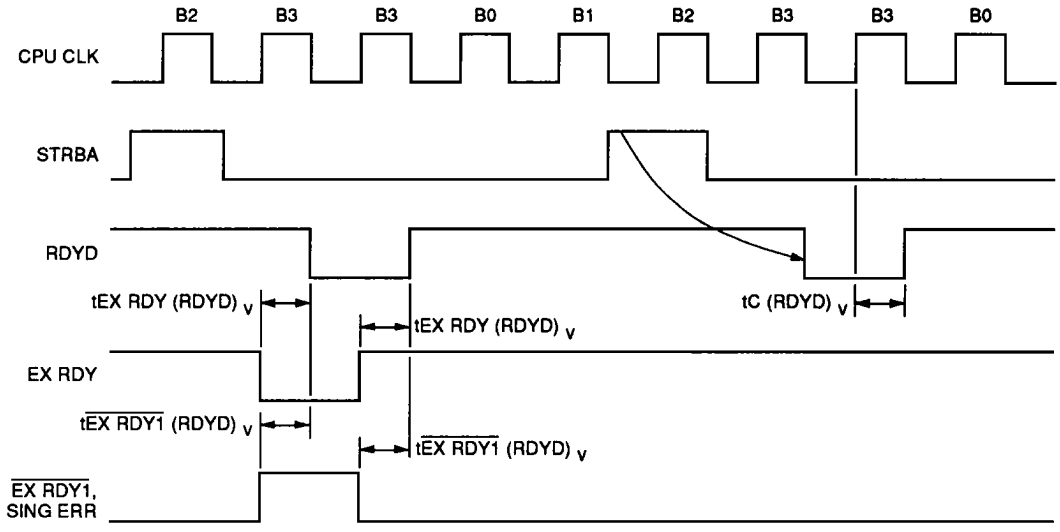
Note:
All time measurements on active signals relate to the 1.5 volt level.

Address Bus and Strobes

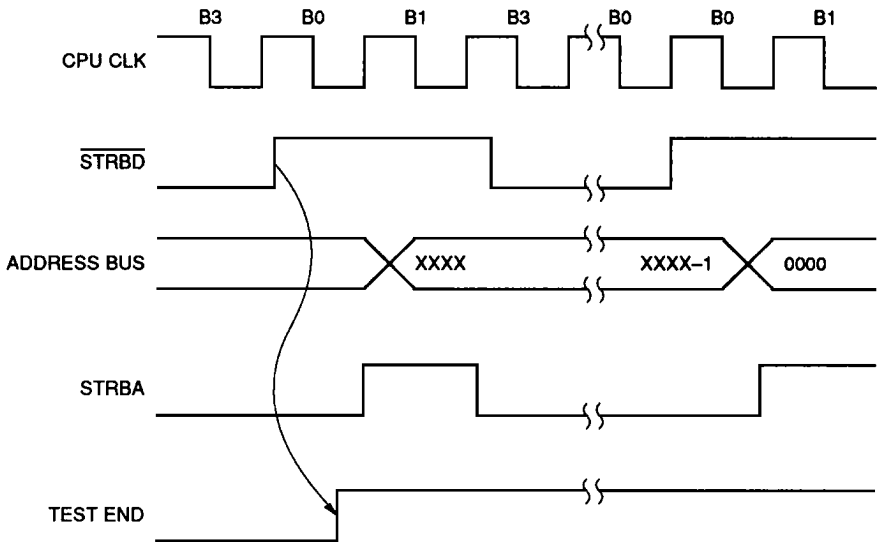


Note:
All time measurements on active signals relate to 1.5V levels.

RDYD TIMING



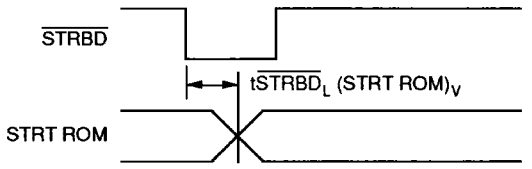
TEST END TIMING[1]



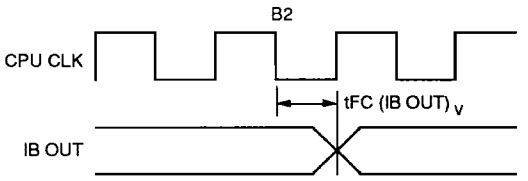
Notes:

1. The last two instructions executed during system test are: XIO RA, 1F44, 0 and JC 7, 0000 hex, 0. After execution of the IOW bus cycle, the XIO proceeds by filling the instruction pipe with two memory read bus cycles where the opcode 7070 hex and 0000 hex are entered to the processor. As from the end of STRBD in the second cycle, TEST END is asserted. At this point, the execution of IC starts by first issuing two fetch cycles from the "old PC" (from addresses XXXX & XXXX+1). The data will be taken from system memory (because TEST END is asserted) but both the address and data are irrelevent. Following that, IC will start filling the pipe from address 0000 hex and 0001 hex, now from the system memory to start user's program execution.
2. All time measurements on active signals relate to 1.5V levels.

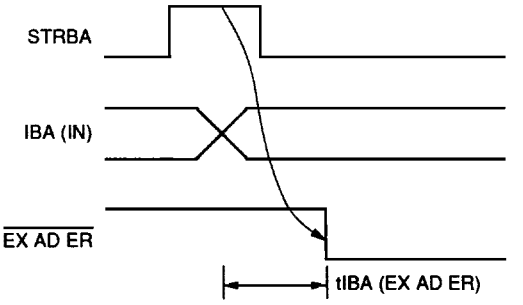
STRT ROM



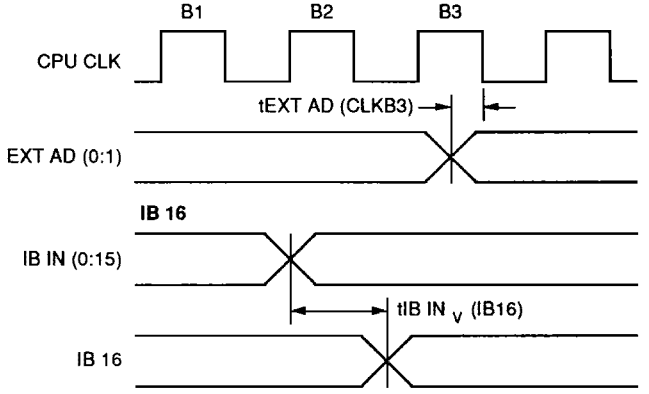
IB BUS OUTPUT (0:15)



EX AD ER

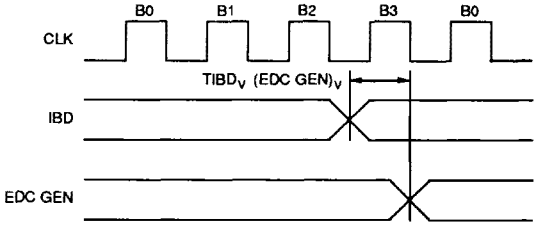


EXTENDED ADDRESSES (0:1)

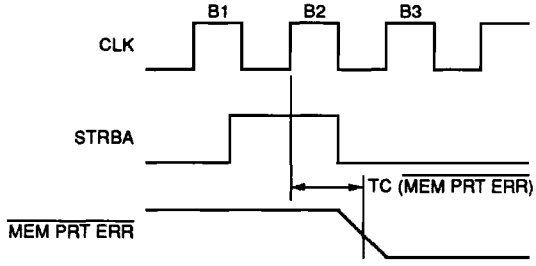


Note: All time measurements on active signals relate to 1.5V levels.

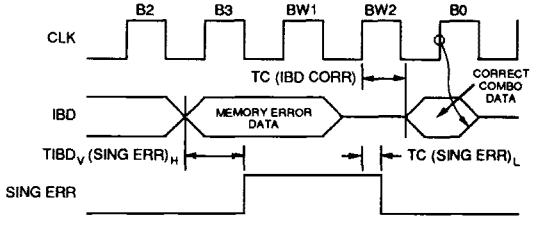
Error Correction (Write Cycle)



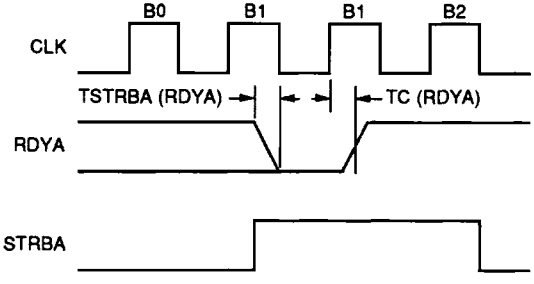
Memory Protect Error



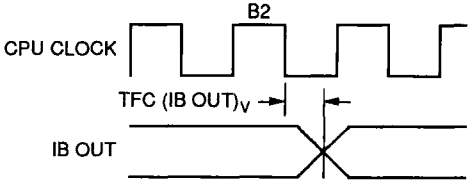
Error Correction (Read Cycle)



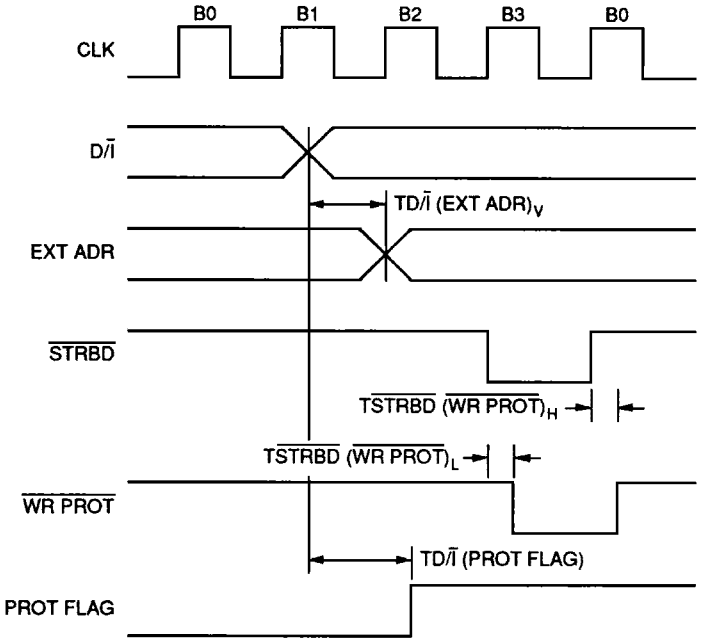
Ready Address



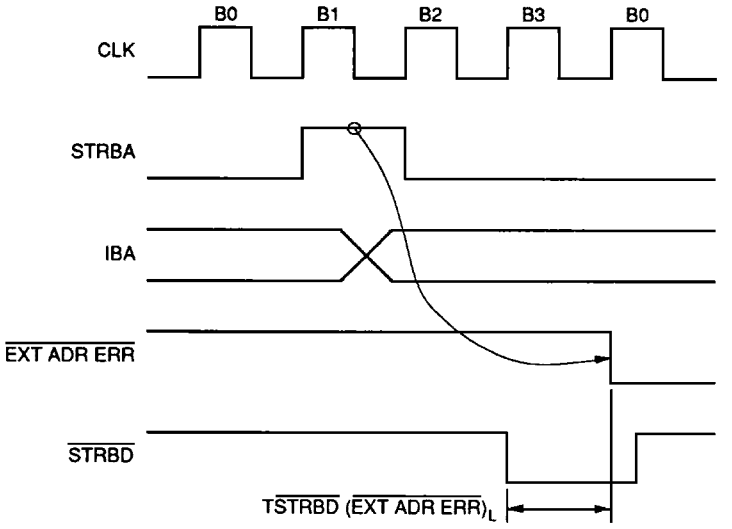
IB Bus Output (0:15)



MMU Cache Hit

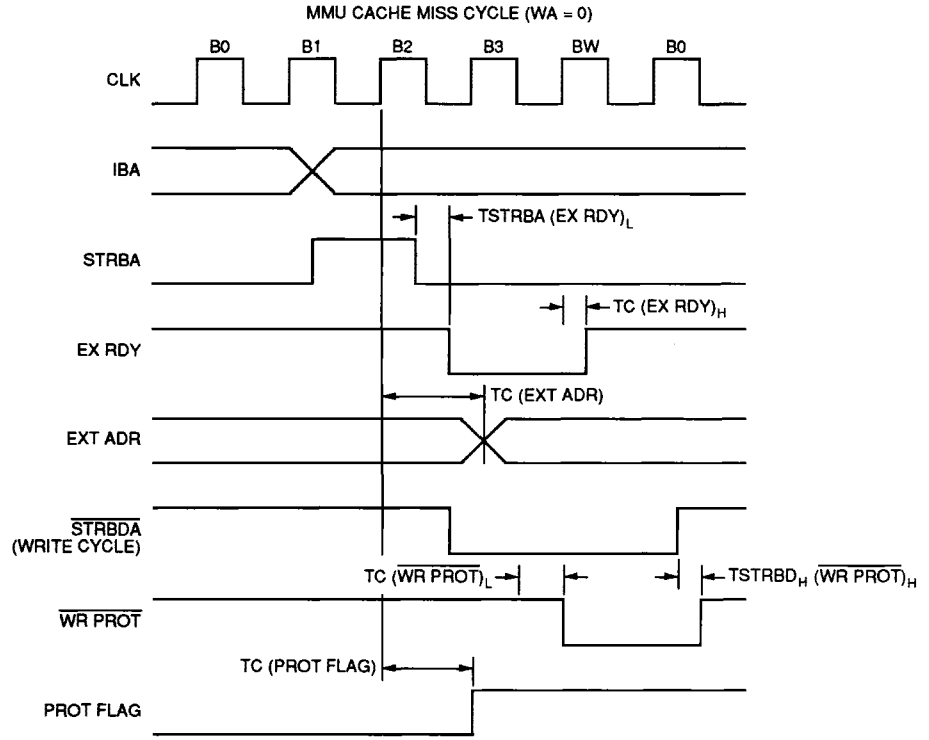


External Address Error

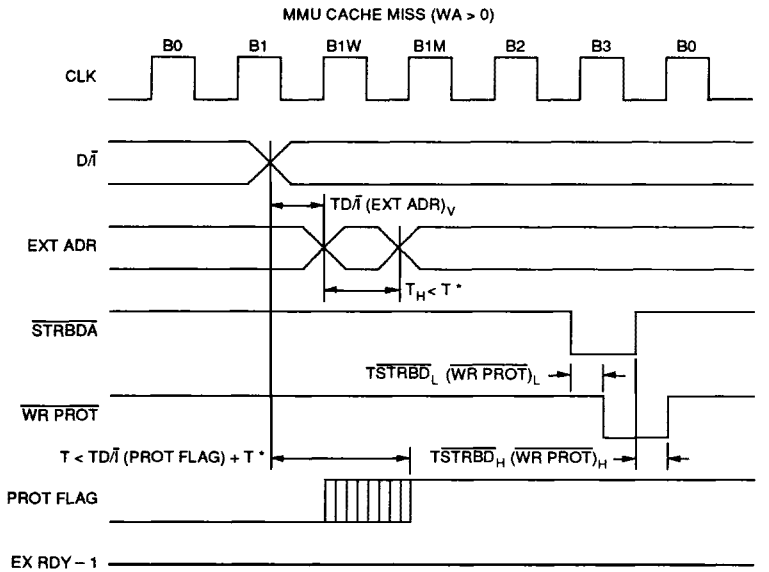


Note:
All time measurements on active signals relate to 1.5V levels.

MMU Cache Miss Cycle (WA = 0)

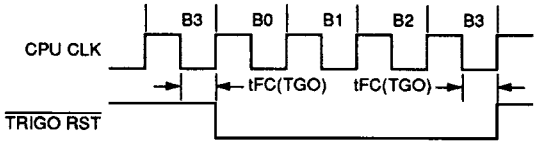


MMU Cache Miss Cycle (WA > 0)

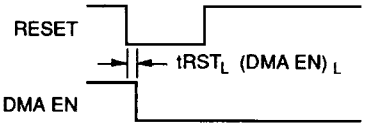


* The WR PROT/PROT FLAG signal is programmed as WR PROT or PROT FLAG. (See BPU Description), T = 1 Clock Period.
Note: All time measurements on active signals relate to 1.5V levels.

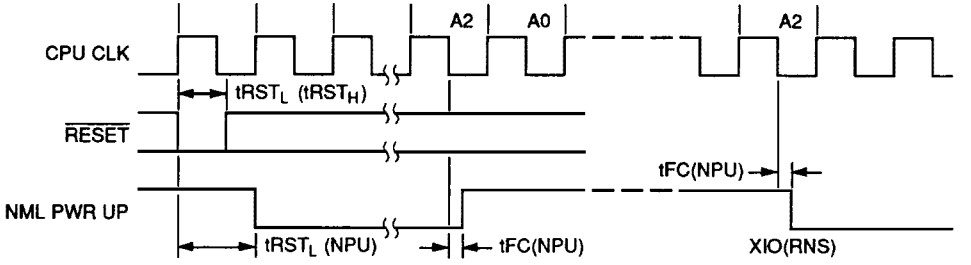
TRIGO RST Discrete Timing



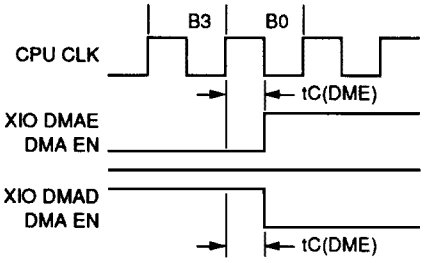
DMA EN Discrete Timing



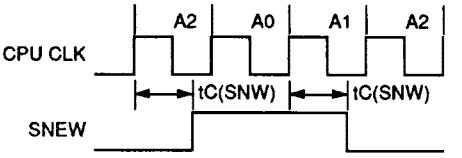
Normal Power Up Discrete Timing



XIO Operations

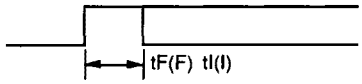


SNEW Discrete Timing

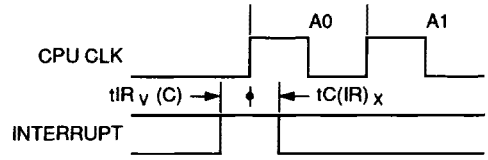


External Faults and Interrupts Timing

Edge-sensitive interrupts and faults ($SYSFLT_0$, $SYSFLT_1$) min. pulse width

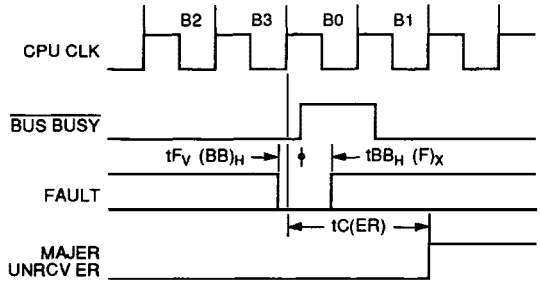


Level-sensitive interrupts

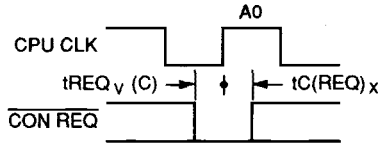


Note: $tC(IR)_X$ max = 35 clocks

Level-sensitive faults

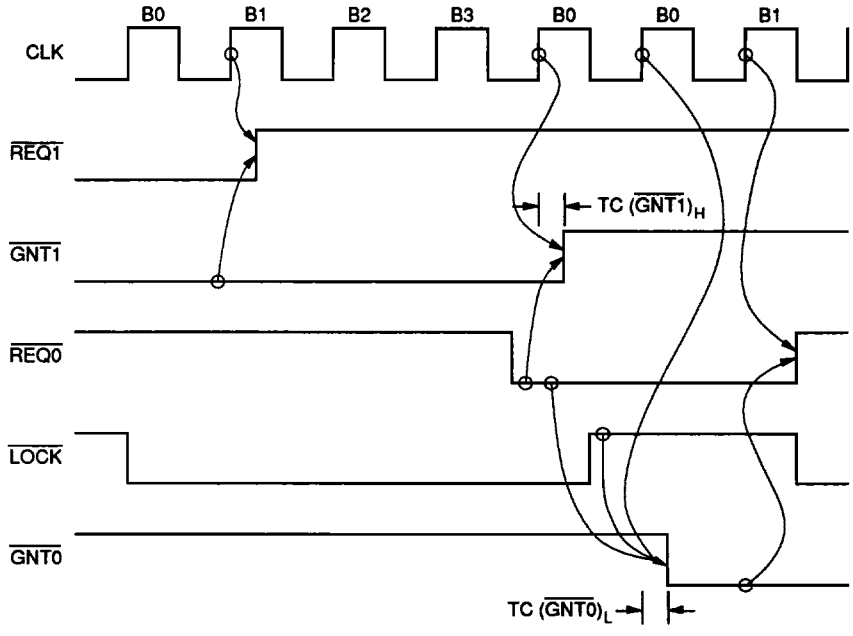


$\overline{\text{CON REQ}}$

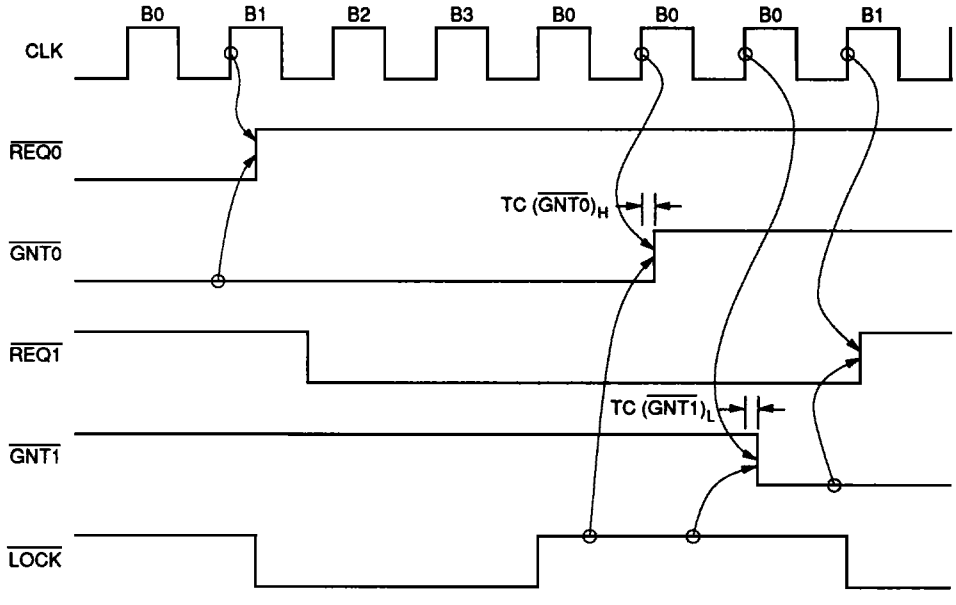


Note: All time measurements on active signals relate to the 1.5 volt level.

Low Priority to High Priority Transition

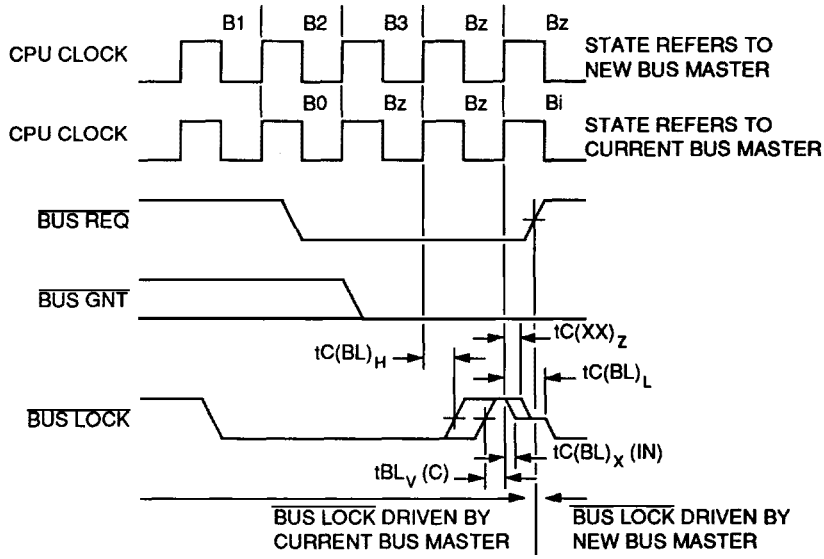


Bus Arbitrator High Priority to Low Priority Transition



Note: All time measurements on active signals relate to 1.5V levels.

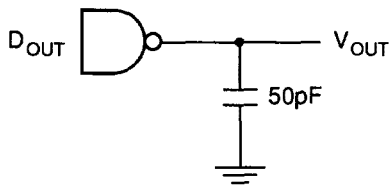
BUS ACQUISITION



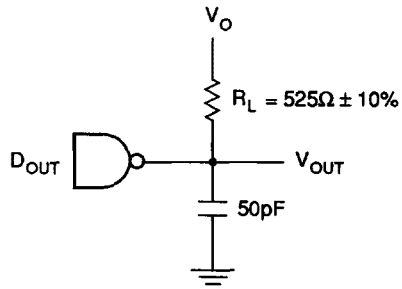
Note:
A CPU contending for the BUS, will assert the $\overline{\text{BUS REQ}}$ line, and will acquire it when $\overline{\text{BUS GNT}}$ is assserted and the BUS is not locked ($\overline{\text{BUS LOCK}}$ is HIGH).

SWITCHING TIME TEST CIRCUITS

Standard Output (Non-Three-State)



Three-State



Note: All time measurements on active signals relate to the 1.5 volt level.

Parameter	V0	VMEA
t_{PLZ}	≥ 3V	0.5V
t_{PHZ}	0V	$V_{CC} - 0.5V$
t_{PXL}	$V_{CC}/2$	1.5V
t_{PXH}	$V_{CC}/2$	1.5V

SIGNAL DESCRIPTIONS

CLOCKS AND EXTERNAL REQUESTS

Mnemonic	Name	Description
CPU CLK	CPU Clock	A single phase input clock signal (0-40 MHz, 40% to 60% duty cycle). This is a common input to all 3 devices.
$\overline{\text{RESET}}$	Reset	An active-low input which initializes the PACE1757M. Input to the P1750A/AE, P1753 and P1754.
$\overline{\text{CON REQ}}$	Console Request	An active-low input that initiates console operations after the completion of the current instruction. Input to the CPU.

INTERRUPT INPUTS

Mnemonic	Name	Description
PWRDN INT	Power Down Interrupt	An interrupt request that cannot be masked or disabled. This signal is active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register of the P1750A/AE.
USR_0INT-USR_5INT	User Interrupt	Interrupt request input signals that are active on the positive going edge or the high level, according to the interrupt mode bit set in the P1750A/AE configuration register.
IOL_1INT-IOL_2INT	I/O Level Interrupts	Active high interrupt requests that can be used to expand the number of user interrupts. Inputs to the P1750A/AE interrupt register.

ERROR CONTROL

Mnemonic	Name	Description
UNRCV ER	Unrecoverable Error	An active-high output that indicates the occurrence of an error classified as unrecoverable. A signal from the CPU
MAJ ER	Major Error	An active-high output that indicates the occurrence of an error classified as major. Again, from the CPU.

DISCRETE CONTROL

Mnemonic	Name	Description
NML PWRUP	Normal Power Up	An active-high output that is set by the CPU when it has successfully completed the built-in self-test in the initialiazation sequence. It can be reset by the I/O command RNS.
SNEW	Start New	An active high output that indicates a new instruction is about to start executing in the next cycle. This signal is issued by the CPU.
$\overline{\text{TRIGO RST}}$	Trigger-Go Reset	An active-low discrete output. This signal can be pulsed low under program control [I/O address 400B(Hex)] and is automatically pulsed by the processor during it's initialization.
STRT ROM	Start Up Rom	An output follow the execution of the ESUR and DSUR, I/O commands as defined in MIL-STD-1750A. It will be at the logical level "1" after executing ESUR and at the logical "0" level after executing DSUR. Initially, it defaults to a "1" on the P1754.
DMA EN	Direct Memory Access Enable	An active high output that indicates the DMA is enabled. It is enabled when the P1750A/AE is initialized (reset). It can be enabled or disabled under program control (I/O commands DMAE, DMAD) by the CPU.

STATUS AND QUALIFIERS

Mnemonic	Name	Description
$\overline{\text{TEST ON}}$	System Test Enable	An active-low input, used to enable the execution of the System Test built into the P1754, immediately after completion of the PACE 1750A/AE initialization and before fetching any instructions from the user's program.
TEST END	System Test End	An active-high output indicating whether the Pace 1754 SystemTest has been completed. Whenever the System Test is disabled by the $\overline{\text{TEST ON}}$ signal, the TEST END output will be at a logical "1" immediately after reset is removed.
SC_0-SC_4	System Configuration Inputs	Inputs which are buffered onto IB0-IB4 when executing an I/O Read from I/O address 8410(hex).
D/$\overline{\text{I}}$	Data or Instruction	A P1750A/AE output signal that indicates whether the current bus cycle access is for Data (high) or Instruction (low). It is tristate during bus cycles not assigned to this CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
R/$\overline{\text{W}}$	Read or Write	A CPU output signal that indicates the direction of data flow with respect to the current bus master. A high idicates a read or input operation. A low indicates a write or output operation. This signal is tri-state during bus cycles not assigned to this CPU.
M/$\overline{\text{IO}}$	Memory or I/O	An output signal from the CPU that indicates whether the current bus cycle is memory (high) or I/O (low). This signal is tri-state during bus cycles not assigned to this CPU.
RDYA_IN	Address Ready In	An active-high input to the CPU that can be used to extend the address phase of a bus cycle. When RDYA_IN is not active, wait states are inserted by the P1750A/AE to accommodate slower memory or I/O devices. This line is usually connected to RDYA_OUT unless the memory interface logic requires the two RDYA signals remain discrete as an input and output.
RDYA_OUT	Address Ready Out	An active high output from the COMBO that indicates that there are no wait states requested when STRBA is active. Wait states are inserted when this signal becomes inactive during STRBA. Up to 3 wait states can be inserted by programming an internal register. Three wait states are inserted after reset (default).
RDYD	Data Ready	An active-high signal to the CPU from the PIC that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the P1750A/AE to acommodate slower memory or I/O devices.

BUS ARBITRATION

Mnemonic	Name	Description
$\overline{\text{BUS REQ}}$	Bus Request	An active-low output that indicates the CPU requires the bus. It becomes inactive when the CPU has acquired the bus and started the bus cycle.
$\overline{\text{BUS GNT}}$	Bus Grant	An active-low input from an external arbiter that indicates this CPU currently has the highest priority bus request. If the bus is not used and not locked, the CPU may begin a bus cycle, commencing with the next CPU clock. A high level will hold the the CPU in Hi Z state (Bz), tri-stating the IB bus status lines (D/$\overline{\text{I}}$, $\overline{\text{R/W}}$, M/$\overline{\text{IO}}$), strobes($\overline{\text{STRBA}}$,$\overline{\text{STRBD}}$), and all the other lines that go tri-state when this CPU does not have the bus.
$\overline{\text{BUS BUSY}}$	Bus Busy	An active-low, bi-directional signal used to establish the beginning and end of a cycle. The trailing edge (low to high transition) is used for sampling bits into the P1750A Fault Register. It is tri-state in bus cycles not assigned to this CPU. However, the CPU monitors the $\overline{\text{BUS BUSY}}$ line for latching non-CPU bus cycle faults into the Fault Register.
$\overline{\text{BUS LOCK}}$	Bus Lock	An active low, bi-directional signal used to lock the bus for successive bus cycles. During non-locked bus cycles,the $\overline{\text{BUS LOCK}}$ signal mimics the $\overline{\text{BUS BUSY}}$ signal. A new master will receive a $\overline{\text{BUS GRANT}}$ only after this signal becomes inactive.It is tri-stated during bus cycles not assigned to this CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB and STLB.
$\overline{\text{BUS GNT}}_0$-$\overline{\text{BUS GNT}}_3$	Bus Grant	Active-low outputs from the PIC indicating which master was granted the BUS. It remains active during $\overline{\text{BUS LOCK}}$ unless a higher master request occurs, which resets it. However, the higher master will be granted the BUS only after the current master's $\overline{\text{BUS LOCK}}$ releases the BUS.
BUS REQ_0-BUS REQ_3	Bus Request	Active low inputs to the PIC that indicate a requirement for the BUS from the 4 masters on the bus. The master assigned to pin $\overline{\text{BUS REQ}}_0$ has the highest priority. The master assigned to pin $\overline{\text{BUS REQ}}_3$ has the lowest priority.

FAULTS AND FLAGS

Mnemonic	Name	Description
$\overline{\text{MEM PRT ER}}$	Memory Protect Error	An active-low input generated by the MMU or BPU, or both, during attempted writes to protected memory. It is sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault Register (bit 0 CPU bus cycle, bit 1 if non-CPU bus cycle). The error is generated in one of the following conditions: a.mismatch in the access keys in the MMU page, an access to an execution protected page during instruction cycles, an access to a write protected page during data cycles or an access to a page write protected by the BPU.
$\overline{\text{MEM PAR ER}}$	Memory Parity Error	An active low signal which is sampled by the $\overline{\text{BUS BUSY}}$ signal into bit 2 of the CPU's Fault Register. It signals an error on the Data Bus during a memory cycle.Two detection modes can be selected by programming the control register of the MMU/ COMBO: EDAC mode(6 Hamming code parity bits) or single bit parity mode (even or odd parity). The signal is inactive when none of the above modes are selected (default after reset).
$\overline{\text{EXT ADR ER IN}}$	External Address Error In	An active-low input sampled by the $\overline{\text{BUS BUSY}}$ signal into the CPU Fault Register (bit 5 or 8), depending on the cycle(memory or I/O).
$\overline{\text{EXT ADR ER OUT}}$	External Address Error Out	An active low output which signals to the CPU and memory interface logic that an unimplemented memory or illegal I/O access has taken place.
$SYSFLT_0$- $SYSFLT_1$	System Fault 0, System Fault 1	Asychronous, positive edge sensitive inputs that set bit 7 ($SYSFLT_0$) or bits 13 and 15 (SYSFLT1) in the P1750A/AE Fault Register.
$\overline{\text{EX AD ER}}$/SING ERR	Illegal Address Error/Single Error	An active low output from the PIC indicating an illegal address error when referencing memory or I/O. It becomes an active high input called SINGLE ERROR for handshaking with the P1753 when the PIC is programmed to support EDAC. Default state after reset is high impedance.
WR PROT/PROT FLAG	Write Protected /Protection Flag	Either an active low output ($\overline{\text{WR PROT}}$, following $\overline{\text{STRBD}}$ timing) during legal memory write cycles when no protection occurs, or an active high (PROT FLAG) signal indicating a protection error in a write cycle. Either mode can be selected by programming the COMBO control register.Default mode after reset is Write Protected.
$\overline{\text{ME PA ER}}$/RAMDIS	Memory Parity Error	An active low output indicating a Parity error when reading from memory. It becomes an active high output calles RAM DISABLE for handshaking with the P1753 when the PIC is programmed to support EDAC.
TC	Terminal Count	An active high output from the PIC indicating a bus time out or a watchdog trigger.

STATUS BUS

Mnemonic	Name	Description
AK0-AK3	Access Key	Active high outputs corresponding to the AK field of the processor status word used to match the Access Lock in the MMU for memory accesses (a mismatch will cause the MMU to pull the $\overline{\text{MEM PRT ER}}$ signal LOW), and also indicate the processor state (PS). Priviledged instructions can be executed with PS=0 only. These signals are tri-state for bus cycles not assigned to this CPU.
AS0-AS3	Address State	Active high outputs corresponding to the AS field of the processor status word that selects the page register group in the MMU. In the DMA physical demultiplexed mode, AS(0:1) will receive the 9th and 10th most significant bits of the physical address for use in the BPU function. These signals are tri-state in bus cycles not assigned to this CPU.

INFORMATION BUS

Mnemonic	Name	Description
IB_0-IB_{15}	Information Bus	A bi-directional time multiplexed address/data BUS. IB0 is the most significant bit
EDC_0-EDC_5	Error Detection/ Correction Bus	An active high bi-directional BUS used for detection of errors on the data BUS (IB_0-IB_{15}) and correction of single errors. When working in parity mode EDC0 is the parity bit. EDC1-EDC5 are undefined in this case.
A(0:1)/EXT ADR(0:1) A(2:15)	Address Bus	An active high output Bus from the PIC. Contains the address of the current bus cycle as latched by the end of STRBA. In system configurations including the MMU function, the only active lines during memory cycles are A(4:15). In this example, A(2:3) are high impedance (don't care) and A(0:1) turn into inputs called Extended Addresses, EXT AD (0:1). In this situation, these two lines, supplied by the MMU, will be used to operate the programmable ready generation during bus cycles.
EXT ADR_0-EXT ADR_7	Extended Address Bus	An bi-directional active high BUS. In CPU cycles, it is an output BUS that is used to select one of 256 pages, 4K words each, expanding the direct addressing space to 1M word. In DMA cycles, indicated by DMA-ACK being active, it is also an output BUS except when programmed for the physical demultiplexed DMA mode. In this example, it becomes an input to receive the eight most significant bits of the DMA physical address for use in the BPU function.

BUS STROBES AND QUALIFIERS

Mnemonic	Name	Description
STRBA (note 1)	Address Strobe	An active-high output that can be used to externally latch the contents of IB(0:15) into the address latches of the PIC and MMU at the high to low transition of the strobe. The signal is tristate during bus cycles not assigned to this CPU. It is issued by the CPU and input to the MMU and PIC.
$\overline{\text{STRBD}}$ (note 2)	Data Strobe	An active-low output used to read or write data from the PIC as well as to strobe data in memory and XIO cycles. This signal is tri-state during bus cycles not assigned to this CPU.It is intercon nected in the same manner as STRBA.
$\overline{\text{MEMW}}$	Memory Write Strobe	An active-low output produced in memory write cycles by the PIC.
$\overline{\text{MEMR}}$	Memory Read Strobe	An active-low output produced by the P1754 in memory read cycles.
$\overline{\text{IOW}}$	I/O Write Strobe	An active-low output produced by the P1754 in output write cycles.
$\overline{\text{IOR}}$	I/O Read Strobe	An active-low output produced by the P1754 during input read cycles.
$\overline{\text{STRB EN}}$	Strobe Enable	An active-low input, enabling the active state of the address outputs of the P1754 and the $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ outputs. When a logic "1" (if enabled by bits EST and EAD of the control register) it will correspondingly tri-state the above signals.
$\overline{\text{INTA}}$	Interrupt Acknowledge Strobe	An active-low output produced during any interrupt sequence corresponding to an output write to address 1000(Hex).
DMA ACK	DMA Acknowledge	An active-high input from the DMA controller to the P1753 which indicates a DMA cycle. Used to select the DMA table in the BPU memory for protection. For example, this could allow the DMA channel to update the program which could be write protected from the processor. In the physical DMA mode, it will cause the Extended Address Lines (EXT ADR_{0-7}) to become inputs providing BPU protection of the DMA transfers.
EX RDY	External Data Ready	An active-high output from the MMU that indicates no wait states are requested. It becomes inactive for one clock (inserting one wait state) whenever a memory page different than the current one is accessed (e.g. a cache miss).
$\overline{\text{EX RDY1}}$	External Ready Data1	An active low input to the PIC from the memory interface logic which at a logical "1" overrides the internal RDYD generation and forces it to a logical "0".

Note 1: One internal pulldown resistor is provided at the STRBA input. The nominal value is 40KOhm and the maximum range is 20KOhm to 80KOhm. In designs with TTL devices loading STRBA, an additional external resistor may be required.

Note 2: One internal pullup is provided at the $\overline{\text{STRBD}}$ input. The nominal value is 40KOhms and the maximum range is 20K-80KOhms.

COMBO REGISTER MAP

CONTROL REGISTER (1F50/9F50)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
QR1	QR2	QR3	QR4	ODD	EEI	EED	EPR	SPD	WPT	EB1	EB2	EIO	GPT	DMX	DLP

CONTROL REGISTER 1 (1F51/9F51)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WA0	WA1	SPI	RES*	PEG	IDL	RESERVED									

UNIMPLEMENTED MEMORY REGISTER 1 (1F55/9F55)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BL1 LO								BL1 HI							

UNIMPLEMENTED MEMORY REGISTER 2 (1F56/9F56)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BL2 LO								BL2 HI							

FIRST UNIMPLEMENTED OUTPUT COMMAND (1F57/9F57)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	LAST SEQUENTIAL PIO OUTPUT COMMAND									

FIRST UNIMPLEMENTED INPUT COMMAND (1F58/9F58)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	LAST SEQUENTIAL PIO INPUT COMMAND									

FIRST FAILING ADDRESS REGISTER (9F59)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIRST FAILING PHYSICAL ADDRESS—PADR (4:19)															

FIRST FAILING DATA REGISTER (9F5A)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIRST FAILING DATA WORD															

MEMORY FAULT STATUS REGISTER (A00D)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LPA				RESERVED							ID	AS			

*Reserved

COMBO REGISTER MAP DEFINITIONS

CONTROL REGISTER (1F50/9F50)
(Default = 00C6H)

QR1	Enable error detection/correction or parity checking/generation for memory addresses 00000H-3FFFFH.
QR2	Enable error detection/correction or parity checking/generation for memory addresses 40000H-7FFFFH.
QR3	Enable error detection/correction or parity checking/generation for memory addresses 80000H-BFFFFH.
QR4	Enable error detection/correction or parity checking/generation for memory addresses C0000H-FFFFFH.
ODD	Enable odd parity, 1 = ODD, 0 = EVEN
EEI	Enable error detection/correction (EDAC) on instruction fetch only.
EED	Enable error detection/correction (EDAC) on operand (data) fetch only.
EPR	Enable parity detection function. (If both EPR and either EEI or EED are enabled, EEI or EED will take preference.)
SPD	Enable 1 wait state on MMU cache miss cycle (1 = 1 WAIT, 0 = NO WAIT).
WPT	Enable protected write strobe (WR PROT PIN). 1: WR PROT = write protected strobe 0: WR PROT = write protect level (1 = write protect memory)
EB1	Enable block 1 of unimplemented memory (as defined in unimplemented memory register 1).
EB2	Enable block 2 of unimplemented memory (as defined in unimplemented memory register 2.)
EIO	Enable illegal PIO detection (as defined in last implemented input and output registers, and Mil-Std-1750A reserved I/O space).
GPT	Enable global memory protect (Set by RESET, and reset by I/O command 4003).
DMX	Demultiplexed Address/data Bus in DMA cycles.
DLP	Logical/Physical DMA (1 = LOGICAL, 0 = Physical).

CONTROL REGISTER 1 (1F51)
(DEFAULT = C3FFH)

WA0/ WA1	Number of WAIT STATES on RDYA.
SPI	Enable illegal PIO detection for MIL-STD-1750A spare I/O spaces.
PEG	Determines what is generated when both EDAC and parity checks are disabled.
IDL	Enables/disables the generation of an idle cycle between BUS REQ and BUS GNT, during read cycles, allowing for one additional clock cycle to release the IB.

UNIMPLEMENTED MEMORY REGISTER1 (1F55)

BL1 LO	Low boundary of unimplemented block 1 of memory.
BL1 HI	High boundary of unimplemented block 1 of memory.

UNIMPLEMENTED MEMORY REGISTER2 (1F56)

BL2 LO	Low boundary of unimplemented block 2 of memory.
BL2 HI	High boundary of unimplemented block 2 of memory.

FIRST UNIMPLEMENTED OUTPUT COMMAND REGISTER (1F57)

BITS 0:5	Not used.
BITS 6:15	First unused sequential PIO output command.

FIRST UNIMPLEMENTED INPUT COMMAND REGISTER (1F58)

BITS 0:5	Not used.
BITS 0:6	First unused sequential PIO input command.

FIRST FAILING ADDRESS REGISTER (1F59)

PADR (4:19):	16 LSB of the physical address of the first failure.

FIRST FAILING DATA REGISTER (1F5B)

BIT 0:15	"1" indicates the position of the wrong/corrected bit in the data word.

MEMORY FAULT STATUS REGISTER (A00D)

LPA	Page address within the group.
ID	Instruction/data.
AS	Group address.

PIC REGISTER MAP

CONTROL REGISTER (1F40, 9F40)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PR1	PR2	PR3	PR4	ODD	EST	EAD	EXR	SPI	CNF	EB1	EB2	EIO	LIO	LME	0

STATUS REGISTER (9F41)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CPU	CMB	PIC	RESERVED		STB	ADR	TWD	TBT	RESERVED						IFL

MEMORY READY PROGRAM REGISTER (1F42, 9F42)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MEM Q1				MEM Q2				MEM Q3				MEM Q4			

I/O READY PROGRAM REGISTER (1F43, 9F43)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IO Q1				IO Q2				IO Q3				IO Q4			

PROGRAM REGISTER (1F44, 9F44)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLOCK FREQUENCY (MHZ)						EBT	SBT	EWD	SWD	RESERVED					

WATCH DOG TIMER (1F45, 9F45)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
WATCHDOG SETUP COUNT															

UNIMPLEMENTED MEMORY REGISTER (1F46, 9F46)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BL1 LO				BL1 HI				BL2 LO				BL2 LO			

FIRST UNIMPLEMENTED OUTPUT COMMAND (1F47, 9F47)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	FIRST UNIMPLEMENTED OUTPUT COMMAND									

FIRST UNIMPLEMENTED INPUT COMMAND (1F48, 9F48)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X	X	X	X	X	X	FIRST UNIMPLEMENTED INPUT COMMAND									

FIRST FAILING ADDRESS REGISTER (9F49)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIRST FAILING ADDRESS															

PIC REGISTER MAP DEFINITIONS

CONTROL REGISTER Default = (0000)

PR1	Enable Parity Checking/Generation for Memory Addresses 0000-3FFF.
PR2	Enable Parity Checking/Generation for Memory Addresses 4000-7FFF.
PR3	Enable Parity Checking/Generation for Memory Addresses 8000-BFFF.
PR4	Enable Parity Checking/Generation for Memory Addresses C000-FFFF.
ODD	Enable ODD Parity.
EST	Enable Three State Control on PIC Generated Strobes; IOR, IOW, MEMR, MEMW.
EAD	Enable Three State Control on PIC Generated Address; A_0-A_{15}.
EXR	Extends ready generation over the full I/O space when = 1. (Default = 0)
SPI	Enables ILLEGAL PIO detection for MIL-STD-1750A spare I/O spaces. 1 = Spare I/O legal, 0 = Default = spare I/O illegal.
CNF	EDAC Function on MMU/COMBO; 1 = used, 0 = not used.
EB1	Enable Block 1 of Unimplemented Memory, as Defined in the Unimplemented Memory Register.
EB2	Enable Block 2 of Unimplemented Memory, as Defined in the Unimplemented Memory Register.
EIO	Enable illegal PIO Detection, as Defined in Last Implemented Input and Output Registers.
LIO	Enable Long I/O Ready Generation, 1ms to 15ms, I/O Addresses 0000-00FF, 8000-80FF.
LME	Enable Long Memory Ready Generation, 1ms to 15ms, Addresses 0000-3FFF.

STATUS REGISTER Default = (0000)

CPU	CPU Passed PIC System Test.
CMB	COMBO Chip Passed PIC System Test.
PIC	PIC Chip Passed PIC System Test.
STB	Reserved
ADR	Reserved
TWD	Watch Dog reached terminal count.
TBT	Bus Time-out reached terminal count.
IFL	Interrupt Flag—Shows the last interrupt I/O command implemented in the software.

MEMORY READY PROGRAM REGISTER
Default = (FFFF)

MEM Q1	Lower Block number of wait states
MEM Q2	Second Block number of wait states
MEM Q3	Third Block number of wait states
MEM Q4	Upper Block number of wait states

I/O READY PROGRAM REGISTER
Default = Undefined

IO Q1	Lower section number of wait states
IO Q2	Second section number of wait states
IO Q3	Third section number of wait states
IO Q4	Upper section number of wait states

PROGRAM REGISTER Default = (0000)

CFB	0:5, Clock Frequency Bits (MHz).
EBT	Enable Bus Time-out Function.
SBT	Select Bus Time-out Limit; 1 = 128 Cycles, 0 = 64 Cycles.
EWD	Enable Watch Dog Function.
SWD	Select Watch Dog Clock, 1 = 1KHz, 0 = 1MHz.

WATCH DOG TIMER REGISTER Default = (0000)

BITS	0:15, Watch Dog set-up Count.

UNIMPLEMENTED MEMORY REGISTER
Default = (Undefined)

BL1 LO	Low boundary of unimplemented block 1 of memory.
BL1 HI	High boundary of unimplemented block 1 of memory.
BL2 LO	Low boundary of unimplemented block 2 of memory.
BL2 HI	High boundary of unimplemented block 2 of memory.

FIRST UNIMPLEMENTED OUTPUT COMMAND REGISTER Default = (Undefined)

BITS 0:5	Not used.
BITS 6:15	First unused sequential PIO output command.

FIRST UNIMPLEMENTER INPUT COMMAND REGISTER

Default = (Undefined)

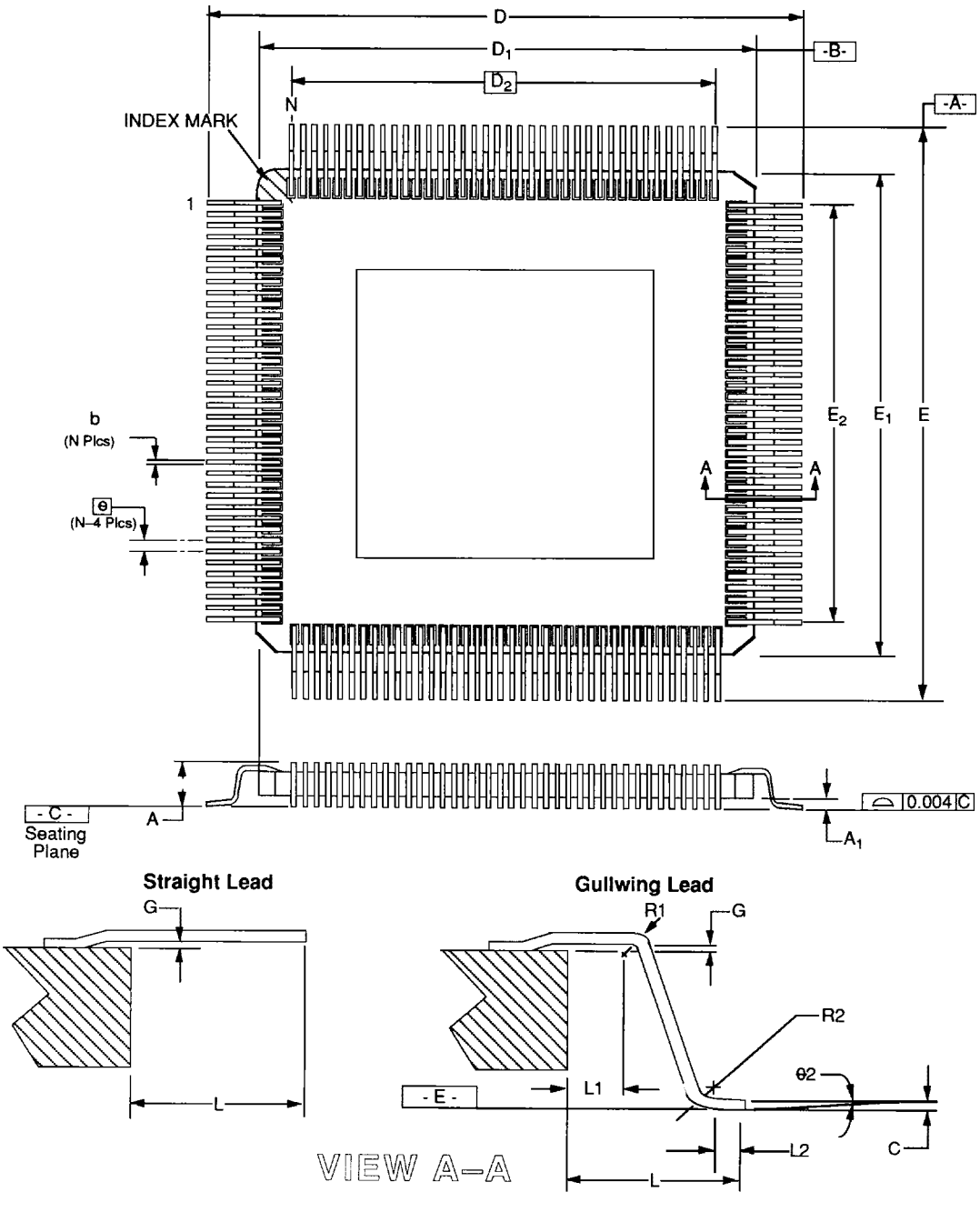
BITS 0:5	Not used.
BITS 6:15	First unused sequential PIO input command.

FIRST FAILING REGISTER

Default = (Undefined)

BITS 0:15	16 LSB of the physical address of the first failure.

PACKAGE OUTLINE



1757M/ME 144-LEAD QUAD FLATPACK OUTLINE

	Straight Leads	Gullwing Leads
A	130 ±10	175 ±20
A1	N/A	25 ±5
b	8 ±2	8 ±2
c	6 ±2	6 ±1
D	1750 ±15	1450 ±10
D1	1150 ±12	1150 ±12
D2	875 REF	875 REF
E	1750 ±5	1450 ±10
E1	1150 ±12	1150 ±12
E2	875 REF	875 REF
L1	N/A	75 ±15
L2	N/A	25 ±5
L	300 ±5	150 ±10
R1	N/A	25 ±2
R2	N/A	25 ±2
O1	N/A	0° 7°
O2	N/A	0° 7°
G	8 ±4	8 ±4
N	144	144

Units: Mils

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ORDERING INFORMATION

PACE1754 – XX YY Z *

- B — Compliant MIL-STD-883C Par 1.2.1 Class B
- C — Commercial Temperature Range 0 to 70°C
- M — Military Temperature Range -55 to +125°C
- C — 64-Pin Dual In-Line
- G — 64-Pin Dual In-Line with Gull Wing leads
- PG — 68-Pin Pin Grid Array (PGA)
- QG — 68-Lead Gull Wing Leaded Quad Pack (Leaded Chip Carrier)
- QL — 68-Lead Quad Flat Pack
- 20 — 20 MHz Clock
- 30 — 30 MHz Clock
- 40 — 40 MHz Clock