



HV04
HV06

64-Channel Serial To Parallel Converter With High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{pp} Max	Package Options				
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die	80-Lead Quad Cerpak Gullwing (MIL-STD-883 Processed*)
HV04	60V	HV0406DG	HV0406PG	HV0406T	HV0406X	—
	80V	HV0408DG	HV0408PG	HV0408T	HV0408X	RBHV0408DG
HV06	60V	HV0606DG	HV0606PG	HV0606T	HV0606X	—
	80V	HV0608DG	HV0608PG	HV0608T	HV0608X	RBHV0608DG

* For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- HVC MOS® technology
- Output voltages up to 90V using a ramped supply
- Low power level shifting
- Shift register speed 8 MHz
- Latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

Absolute Maximum Ratings¹

Supply voltage, V_{DD}	-0.5V to +15V	
Supply voltage, V_{pp} ²	-0.5V to +90V	
Logic input levels	-0.5V to V_{DD} +0.5V	
Ground current ³	3.0A	
High voltage supply current ³	2.6A	
Continuous total power dissipation ⁴	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range	-65°C to +150°C	

Notes:

1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{pp} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

Not recommended for new designs. Please use HV577, with improved performance.

The HV04 and HV06 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04 shifts in the counterclockwise direction when viewed from the top of the package and the HV06 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the LE (latch enable), BL (blinking), or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored when LE is low.

The HV04 and HV06 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics SUPERTEX INC

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	$f_{CLK} = 8MHz, f_{DATA} = 4MHz$ $LE = LOW$
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All $V_{IN} = 0V$
I_{PP}	High Voltage Supply Current				0.50	mA	$V_{PP} = 80V$ All outputs high
					0.50	mA	$V_{PP} = 80V$ All outputs low
I_{IH}	High-Level Logic Input Current				10	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	μA	$V_I = 0V$
V_{OH}	High-Level Output	HV_{OUT}	74			V	$V_{PP} = 80V, IHV_{OUT} = -20mA$
		Data Out	$V_{DD} - 1V$			V	$ID_{OUT} = -100\mu A$
V_{OL}	Low-Level Output	HV_{OUT}			6	V	$V_{PP} = 80V, IHV_{OUT} = +10mA$
		Data Out			1	V	$ID_{OUT} = +100\mu A$
V_{OC}	HV _{OUT} Clamp Voltage				$V_{PP} + 1.5$	V	$I_{OL} = +10mA$
					-1.5	V	$I_{OL} = -20mA$

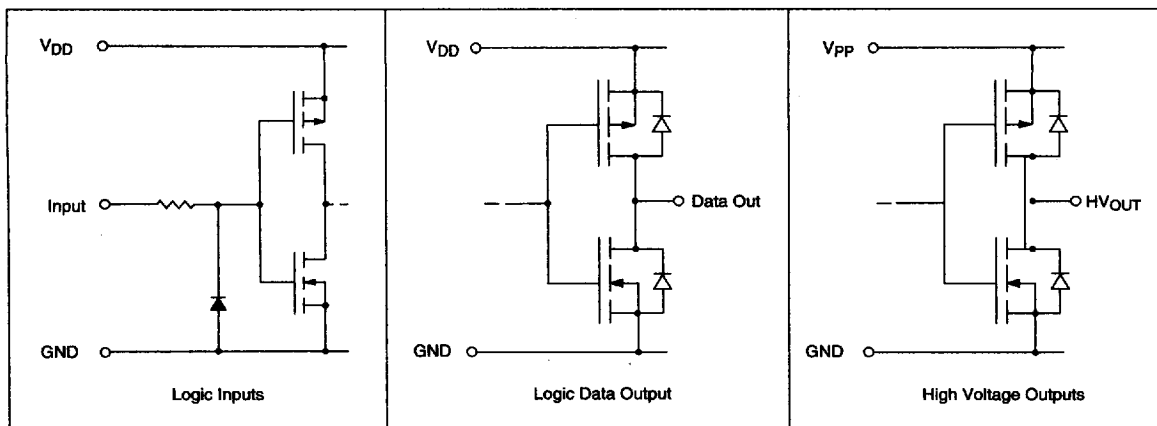
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	LE Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	LE Setup Time Before Rising Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in LE, POL, BL Is Allowed	100			ns	
t_{SL}	Setup Time from LE Rise to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from BL Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from POL Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

Recommended Operating Conditions

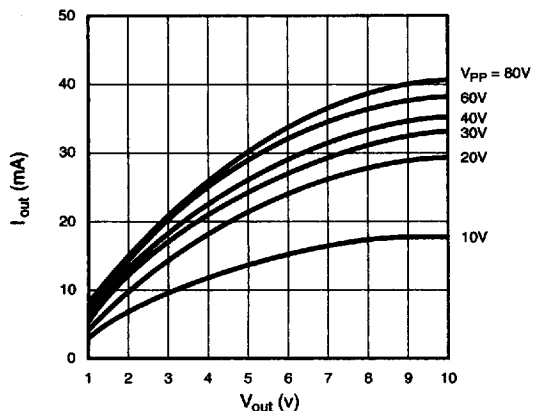
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	$V_{DD} - 2V$		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
dV/dt	V_{PP} ramp rate			80	V/ μs
T_A	Operating free-air temperature	-40		+85	$^{\circ}C$

Input and Output Equivalent Circuits SUPERTEX INC

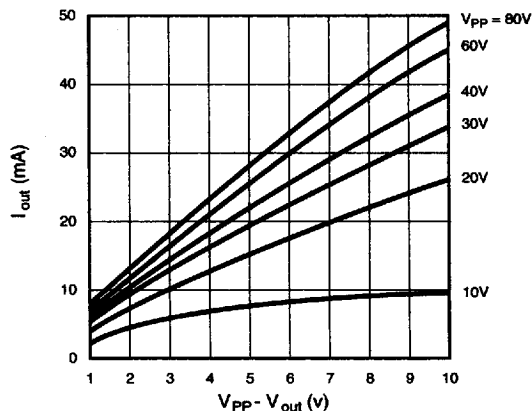


Typical Performance Curves

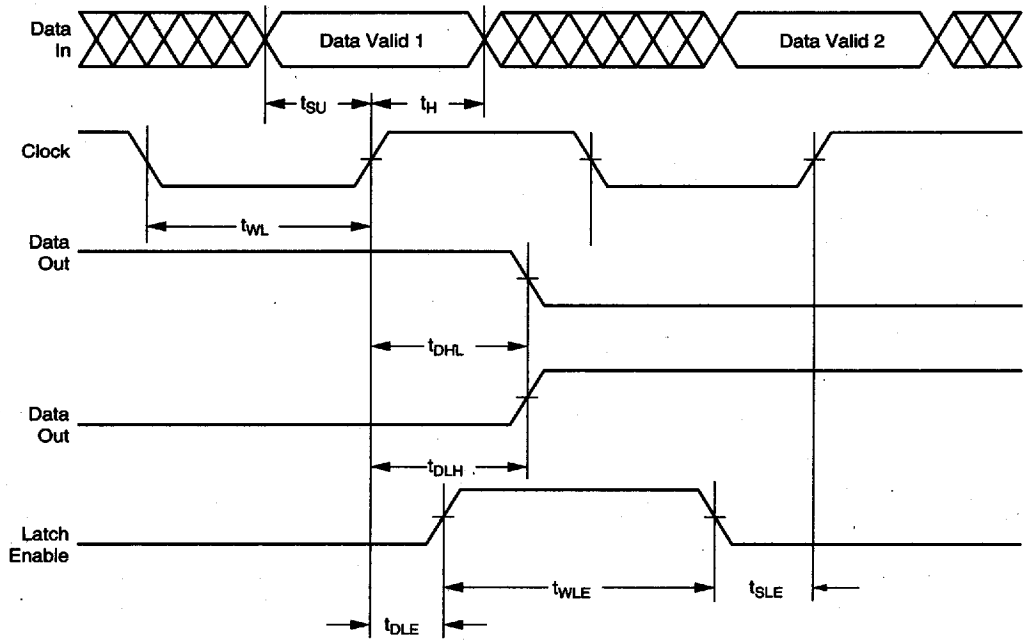
Typical HV04/06 Sink Current @ 25°C



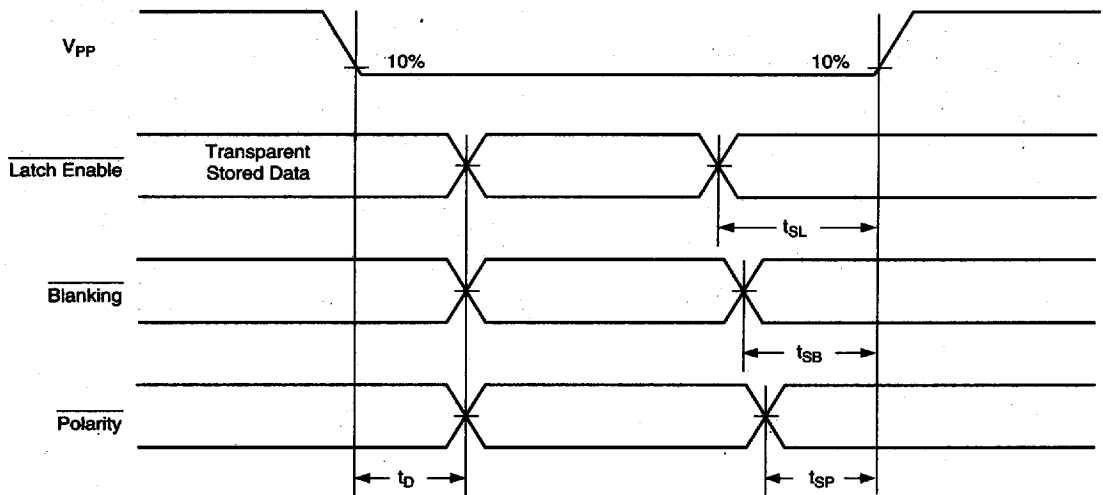
Typical HV04/06 Source Current @ 25°C



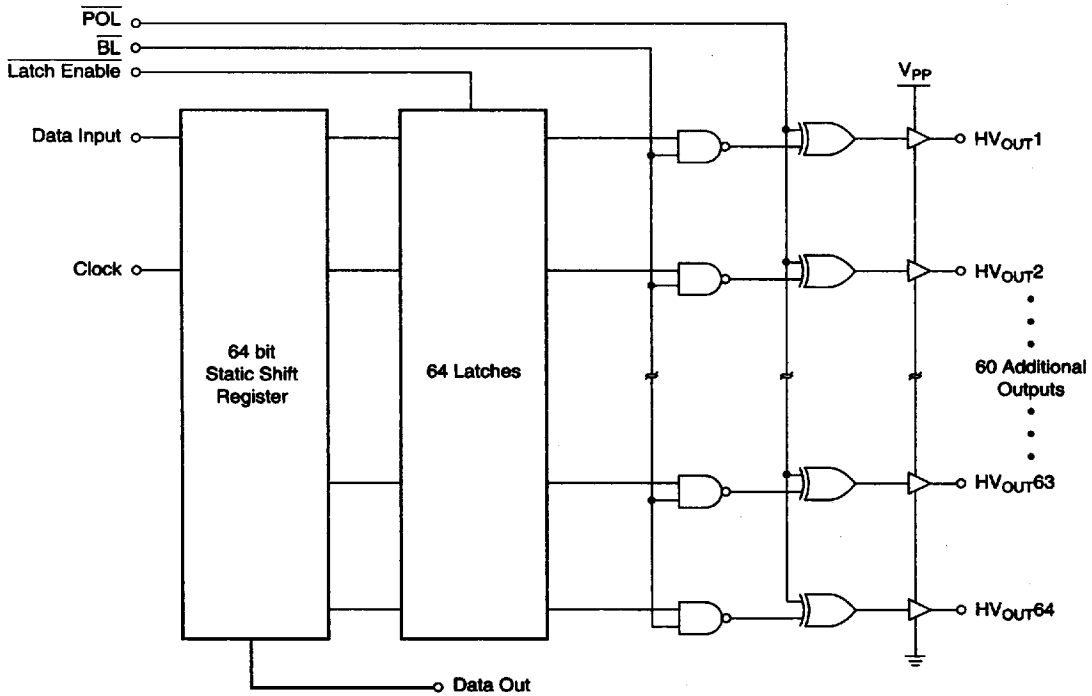
Switching Waveforms



Output Control Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	\overline{LE}	\overline{BL}	\overline{POL}	Shift Reg 1 2...64	HV Outputs 1 2...64		Data Out	
All on	X	X	X	L	L	* *...*	H	H...H	*	
All off	X	X	X	L	H	* *...*	L	L...L	*	
Invert mode	X	X	L	H	L	* *...*	\overline{H}	\overline{H} ... \overline{H}	*	
Load S/R	H or L	↑	L	H	H	H or L *...*	*	*...*	*	
Load Latches	X	H or L	H	H	H	* *...*	*	*...*	*	
	X	H or L	H	H	L	* *...*	\overline{H}	\overline{H} ... \overline{H}	*	
Transparent Latch mode	L	↑	H	H	H	L *...*	L	*...*	*	
	H	↑	H	H	H	H *...*	H	*...*	*	

Notes:
 H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
 * = dependent on previous stage's state before the last CLK or last LE high.

Pin Configurations
PG and DG Packages

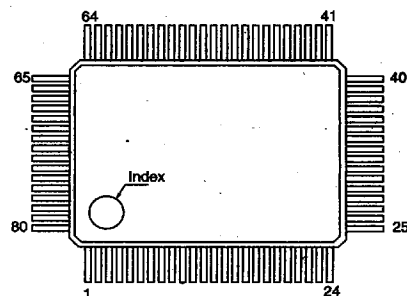
HV04

Pin	Function	Pin	Function
1	GND	41	GND
2	V _{PP}	42	V _{PP}
3	HV _{OUT} 59	43	HV _{OUT} 23
4	HV _{OUT} 60	44	HV _{OUT} 24
5	HV _{OUT} 61	45	HV _{OUT} 25
6	HV _{OUT} 62	46	HV _{OUT} 26
7	HV _{OUT} 63	47	HV _{OUT} 27
8	HV _{OUT} 64	48	HV _{OUT} 28
9	POL	49	HV _{OUT} 29
10	Data Out	50	HV _{OUT} 30
11	CLK	51	HV _{OUT} 31
12	GND	52	HV _{OUT} 32
13	V _{DD}	53	HV _{OUT} 33
14	LE	54	HV _{OUT} 34
15	Data In	55	HV _{OUT} 35
16	BL	56	HV _{OUT} 36
17	HV _{OUT} 1	57	HV _{OUT} 37
18	HV _{OUT} 2	58	HV _{OUT} 38
19	HV _{OUT} 3	59	HV _{OUT} 39
20	HV _{OUT} 4	60	HV _{OUT} 40
21	HV _{OUT} 5	61	HV _{OUT} 41
22	HV _{OUT} 6	62	HV _{OUT} 42
23	V _{PP}	63	V _{PP}
24	GND	64	GND
25	HV _{OUT} 7	65	HV _{OUT} 43
26	HV _{OUT} 8	66	HV _{OUT} 44
27	HV _{OUT} 9	67	HV _{OUT} 45
28	HV _{OUT} 10	68	HV _{OUT} 46
29	HV _{OUT} 11	69	HV _{OUT} 47
30	HV _{OUT} 12	70	HV _{OUT} 48
31	HV _{OUT} 13	71	HV _{OUT} 49
32	HV _{OUT} 14	72	HV _{OUT} 50
33	HV _{OUT} 15	73	HV _{OUT} 51
34	HV _{OUT} 16	74	HV _{OUT} 52
35	HV _{OUT} 17	75	HV _{OUT} 53
36	HV _{OUT} 18	76	HV _{OUT} 54
37	HV _{OUT} 19	77	HV _{OUT} 55
38	HV _{OUT} 20	78	HV _{OUT} 56
39	HV _{OUT} 21	79	HV _{OUT} 57
40	HV _{OUT} 22	80	HV _{OUT} 58

HV06

Pin	Function	Pin	Function
1	GND	41	GND
2	V _{PP}	42	V _{PP}
3	HV _{OUT} 6	43	HV _{OUT} 42
4	HV _{OUT} 5	44	HV _{OUT} 41
5	HV _{OUT} 4	45	HV _{OUT} 40
6	HV _{OUT} 3	46	HV _{OUT} 39
7	HV _{OUT} 2	47	HV _{OUT} 38
8	HV _{OUT} 1	48	HV _{OUT} 37
9	POL	49	HV _{OUT} 36
10	Data Out	50	HV _{OUT} 35
11	CLK	51	HV _{OUT} 34
12	GND	52	HV _{OUT} 33
13	V _{DD}	53	HV _{OUT} 32
14	LE	54	HV _{OUT} 31
15	Data In	55	HV _{OUT} 30
16	BL	56	HV _{OUT} 29
17	HV _{OUT} 64	57	HV _{OUT} 28
18	HV _{OUT} 63	58	HV _{OUT} 27
19	HV _{OUT} 62	59	HV _{OUT} 26
20	HV _{OUT} 61	60	HV _{OUT} 25
21	HV _{OUT} 60	61	HV _{OUT} 24
22	HV _{OUT} 59	62	HV _{OUT} 23
23	V _{PP}	63	V _{PP}
24	GND	64	GND
25	HV _{OUT} 58	65	HV _{OUT} 22
26	HV _{OUT} 57	66	HV _{OUT} 21
27	HV _{OUT} 56	67	HV _{OUT} 20
28	HV _{OUT} 55	68	HV _{OUT} 19
29	HV _{OUT} 54	69	HV _{OUT} 18
30	HV _{OUT} 53	70	HV _{OUT} 17
31	HV _{OUT} 52	71	HV _{OUT} 16
32	HV _{OUT} 51	72	HV _{OUT} 15
33	HV _{OUT} 50	73	HV _{OUT} 14
34	HV _{OUT} 49	74	HV _{OUT} 13
35	HV _{OUT} 48	75	HV _{OUT} 12
36	HV _{OUT} 47	76	HV _{OUT} 11
37	HV _{OUT} 46	77	HV _{OUT} 10
38	HV _{OUT} 45	78	HV _{OUT} 9
39	HV _{OUT} 44	79	HV _{OUT} 8
40	HV _{OUT} 43	80	HV _{OUT} 7

Package Outline



top view
80-pin Gullwing Package