LVDT/RVDT to digital converter ratiometric 14 bit series 178A100

FEATURES
- Built-in power oscillator
- Overrange output
- Reference frequency 400Hz to 5kHz
- 14-bit position output
- 50Hz bandwidth 400Hz models
- 140Hz bandwidth 1-5kHz models

APPLICATIONS
Avionic controls — Machine tool controls — Industrial Instrumentation — General purpose AC/Digital conversion

GENERAL DATA

The series 178A100 converters translate the outputs of LVDT and RVDT transducers into 14 bit offset binary digital code.

THEORY OF OPERATION

The 178A100 is a tracking converter employing a (Type II) servo loop which exhibits no velocity errors and only minor acceleration errors. The output automatically follows the input without the need of a convert command. A conversion is initiated by a change of input signal equivalent to 1 LSB of the output and is indicated by a Converter Busy (CB) pulse which brackets the output code change.

With an LVDT connected to give a null at center position, the output will track the input from digital "1 + all zeros" to digital "all ones" for in-phase condition, and digital "1 + all zeros" to digital "all zeros" for out-of-phase condition.

In the event the signal input exceeds the normal range, the overrange output is set to logic '1' and output data is invalid.

DIGITAL OUTPUT CODES

	MSB												LSB	PHASE
+FULL SCALE	1	1	1	1	1	1	1	1	1	1	1	1	1	IN
ZERO	1	0	0	0	0	0	0	0	0	0	0	0	0	
-FULL SCALE	0	0	0	0	0	0	0	0	0	0	0	0	0	OUT

Irrespective of the method of input connection the output codes will be offset binary.

LOGIC INPUTS/OUTPUTS

The 14 bit digital output is high speed CMOS logic capable of driving up to 3 TTL loads.

The Converter Busy pulse (CB) is a 2.0 usecond positive pulse which brackets data output code changes. The Inhibit input (INH) is used to lock the digital data in the output counters.

ELECTRICAL SPECIFICATIONS

Parameter	Value
Signal Inputs	
SH-SL & RH-RL	2.5 Vrms max. @ 200 Kohm differential 400–5kHz
Analog Outputs	
Reference Output (REF)[1]	2.5Vrms @ 5mA
Signal Output (SIG)[2]	2.5Vrms @ 5mA
Demodulator Output (D)	1.5mV/LSB
Velocity Output (VEL)	±10Vdc for max velocity
Inter LSB Output (E)	±6.0Vdc/LSB
Oscillator Output (OSC)	2.5–7Vrms @ 150mA rms max. 400-5kHz, short ckt & over temp. protection
Digital Outputs[3]	
Data (1–14)	14 bit offset binary
Converter Busy (CB)	2.0 usec positive pulse
Overrange (OVR)	Logic '1' = out of range
Direction (DIR)	Logic '0' = counting up
Accuracy[4]	
Gain Error	
@ x1 gain	±0.03% FS
@ x10 gain	±0.06% FS
Linearity	±0.024% FS
Differential linearity	±1 LSB max
Dynamic Characteristics	
Slew Rate	
50 Hz Bandwidth	150 LBS/ms
140 Hz Bandwidth	320 LSB/ms
Settling Time (½ F.S. step)	
50 Hz Bandwidth	160 ms
140 Hz Bandwidth	70 ms
Digital Inputs	
Inhibit (INH)[5]	Logic '0' inhibits
Power Supplies	
+15V	45 mA + oscillator load
−15V	45 mA + oscillator load
+5V	5 mA
Temperature Ranges	
Operating	
Standard	0°C to +70°C
ET Version	−55°C to +105°C
Storage	−55°C to +125°C
Dimensions	2.62″ x 3.12″ x 0.42″
Weight	4.0 oz.

NOTES:

1. REF is the output of the internal differential reference amplifier
2. SIG is the output of the internal differential signal amplifier and gain stage. In order to meet the converter accuracy the gain of the signal amplifier should be carefully chosen since the converter operates on the ratio of SIG and REF.
3. HCMOS output 3 TTL loads maximum except DIR output 1 CMOS load max.
4. Accuracy applies for:
   (a) ±10% reference and signal voltage variation
   (b) over operating temperature range
   (c) over operating frequency range
   (d) not greater than 3° phase error between reference and signal inputs
5. CMOS input with 51 Kohm pull-up resistor

The CB output or the INH input can be used to interface to a computer. The converter will ignore an inhibit command applied during the CB time. There are two methods of interfacing with a computer: (1) synchronously and (2) asynchronously. A simple method of synchronous loading is to (a) set INH to logic '0', (2) wait 3 useconds, (c) transfer the data, and (d) reset INH to logic '1'. Asynchronous loading is accomplished by transferring data on the negative going edge of the CB pulse.

The Direction output (DIR) indicates the direction in which the 14 bit digital output is counting. Logic '0' indicates counting up and logic '1' indicates counting down. This logic level is only valid during the CB pulse. Do not load this output with other than CMOS loads.

An Overrange output (OVR) is provided, when at logic '1' indicates the SIG output has exceeded the REF output and the converter is out of range and the output data is invalid.

REFERENCE INPUT AMPLITUDE

In order to optimize converter performance the reference input RH-RL must be maintained so the REF output is 2.5Vrms ±10%. This output may be scaled downwards by placing matched resistors in series with RH-RL. The values for these resistors can be calulated as follows:

$$R = 40E - 100$$

Where: R = value of series resistors in Kohms
E = reference input voltage

Note: The resistors should be matched to within ±0.02% and have a tempco match of 10 ppm.

CONNECTING THE CONVERTER

The power lines, which must not be reversed, should be connected to the +15V, −15V and +5V pins with the common connected to the GND pin. Because the converter contains a power oscillator and has a high gain input stage it is recommended that 1.0μF 50V tantalum capacitors be placed from the ±15V supplies to GND.

The digital output is taken from pins 1 thru 14, where pin 1 is the MSB.

For connections to the reference (RH-RL) and signal inputs (SH-SL) refer to TB-6, LVDT to digital interface.

SIGNAL INPUT GAIN

Since the transformation ratio of an LVDT or RVDT from excitation voltage to signal voltage varies from device to device, provisions for gain scaling have been included. The gain can be selected to ensure that the full scale output of the converter represents the maximum stroke position of the transducer.

The gain setting is accomplished by means of the G1 and G2 pins. A jumper between these two pins gives a preset gain of x10, no connection gives a present gain of x1.

Intermediate gains are accomplished by connecting a resistor between G1 and G2 with a value according to the following equation:

$$G = \frac{9K}{Rg + 1K} + 1$$

Where: Rg is the value of the external resistor

The internal resistor temperature coefficient is ±10PPM with a ±2PPM tempco match.

In order to obtain maximum resolution, the gain should be selected so that the voltage at the SIG output equals the voltage at the REF output with maximum stroke position of the transducer. Another method of accomplishing this is to adjust the gain until all ones or all zeros are present at the digital output with maximum stroke position of the transducer.

POWER OSCILLATOR

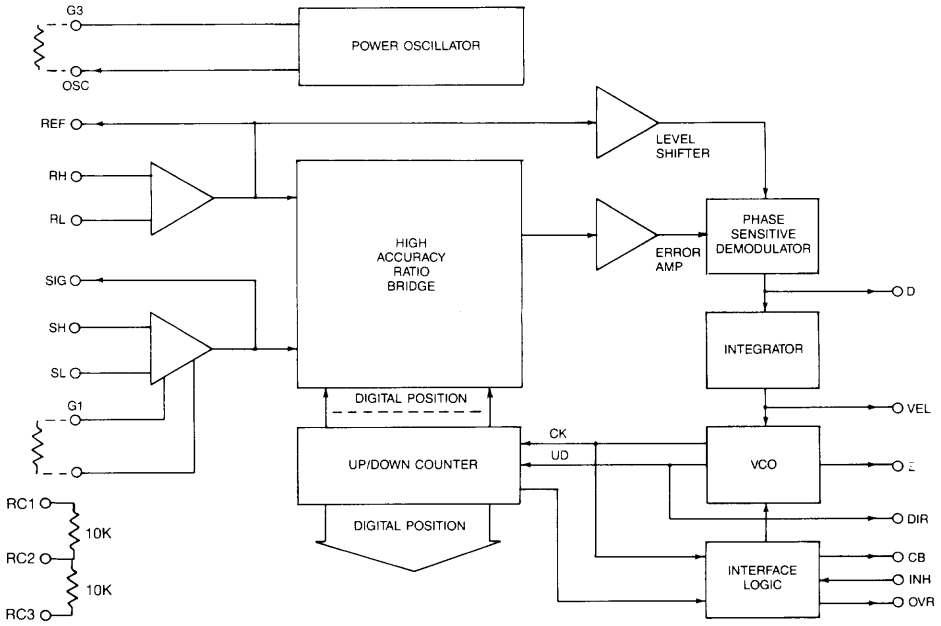
The 178A100 contains an internal power oscillator for the LVDT or RVDT excitation drive. The OSC output voltage can be programmed from 2.5Vrms to 7.0Vrms by means of an external resistor connected between G3 and OSC. With no resistor connection the output amplitude will be 7.0Vrms ±5%. A jumper between the two pins gives an amplitude of 2.5Vrms ±5%.

The value of this resistor can be calculated as follows:

$$R = \frac{8.45V - 21.125}{7 - V}$$

Where: R = resistor in Kohms
V = desired output voltage

BLOCK DIAGRAM
LVDT/DIGITAL CONVERTER

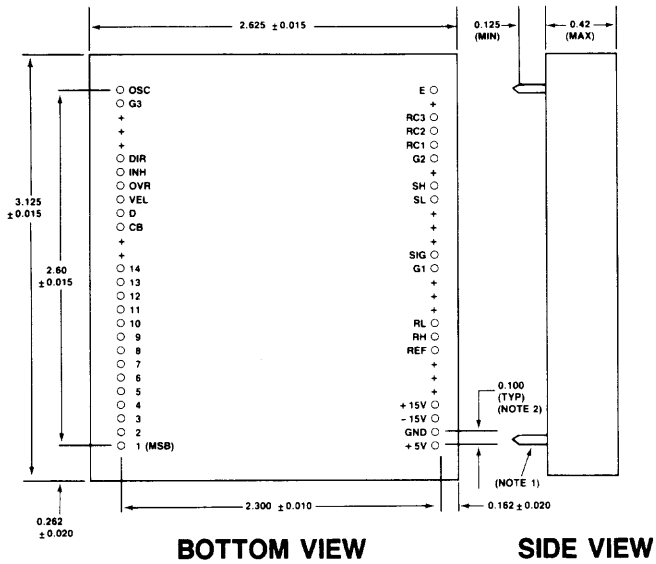


ORDERING INFORMATION

178A Suffix	Operating Frequency	Internal Oscillator
100	400Hz	Yes
101	1.0kHz	Yes
102	2.6kHz	Yes
103	5.0kHz	Yes
104	400Hz-5.0kHz	No
105	1.0kHz-5.0kHz	No

Standard temperature range (0° to 70°C), add suffix ET to part number for extended temperature range. (−55° to +105°C).

MECHANICAL OUTLINE



NOTES

1. Rigid 0.025 diameter pins for solder-in or plug-in applications.
2. Noncumulative.
3. Dimensions are in inches.
4. G3 and OSC pins deleted on models without internal oscillator.

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