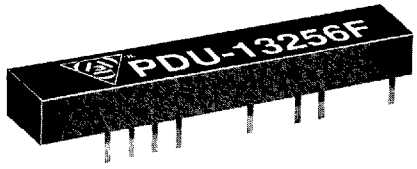
Digitally Programmable Delay Units

SERIES: PDU-13256F
(8-Bit) TTL Interfaced

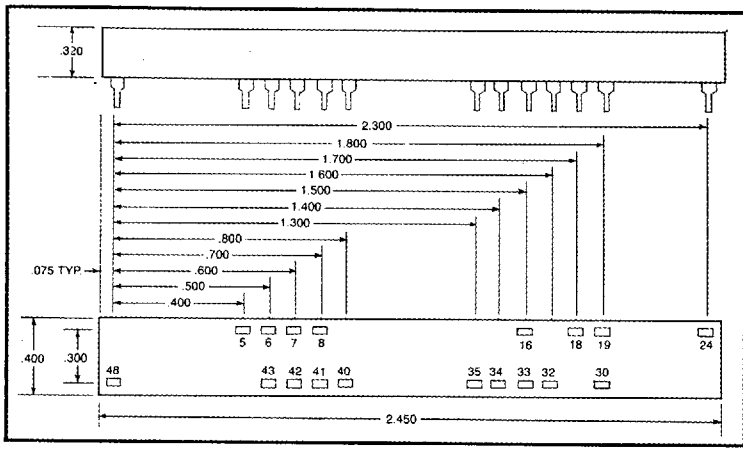
data delay devices, inc.

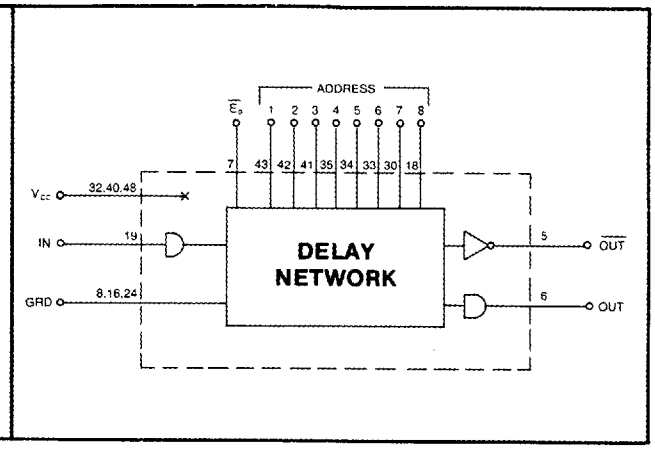


Features:
- Input & output TTL buffered
- 8-BIT TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting
- Completely interfaced
- Compact & low profile

Specifications:
- **Delay variation:** Monotonic in one direction.
- **Programmed delay tolerance:** ±5% or 2 ns whichever is greater.
- **Inherent delay (TDO):** 15 ns on pin 6, 18 ns on pin 5 } typical
- **Propagation delay:**
  Address to output (TSUA) 12 ns typ.
  Enable to output (TSUE) 12 ns typ.
- **Power dissipation:** .95 w max.
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperature:** 0-70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

Test Conditions:
- **Input pulse-width:** ≥150% of Max. delay.
- **Input pulse spacing:** ≥3 times of Max. delay.
- **Input pulse voltage:** TTL logic.
- **Measurements taken @** Ta = 25°C; Vcc = 5V.





TRUTH TABLE

Address (Bit No.)								Enable ($\overline{E_0}$)	Delay Out
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	0	1	0	T_1
0	0	0	0	0	0	1	0	0	T_2
0	0	0	0	0	0	1	1	0	T_3
0	0	0	0	0	1	0	0	0	T_4
0	0	0	0	0	1	1	1	0	T_7
0	0	0	0	1	0	0	0	0	T_8
0	0	0	0	1	1	1	1	0	T_{15}
0	0	0	1	0	0	0	0	0	T_{16}
0	0	0	1	1	1	1	1	0	T_{31}
0	0	1	0	0	0	0	0	0	T_{32}
0	0	1	1	1	1	1	1	0	T_{63}
0	1	0	0	0	0	0	0	0	T_{64}
0	1	1	1	1	1	1	1	0	T_{127}
1	0	0	0	0	0	0	0	0	T_{128}
1	1	1	1	1	1	1	1	0	T_{255}
ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	1

0 = Logic 0 1 = Logic 1 ϕ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{255}$ multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-13256F-.5	.5 ± .3	127.5
PDU-13256F-1	1 ± .5	255
PDU-13256F-2	2 ± .5	510
PDU-13256F-3	3 ± 1.0	765
PDU-13256F-4	4 ± 1.0	1,020
PDU-13256F-5	5 ± 1.5	1,275
PDU-13256F-6	6 ± 1.5	1,530
PDU-13256F-7	7 ± 1.5	1,785
PDU-13256F-8	8 ± 2.0	2,040
PDU-13256F-9	9 ± 2.0	2,295
PDU-13256F-10	10 ± 2.0	2,550

NOTE: 1. For the sake of simplicity all 256 programmable steps are not shown in this truth table.
2. After Bit 6, the incremental delay tolerance is 5% of programmed delay.

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