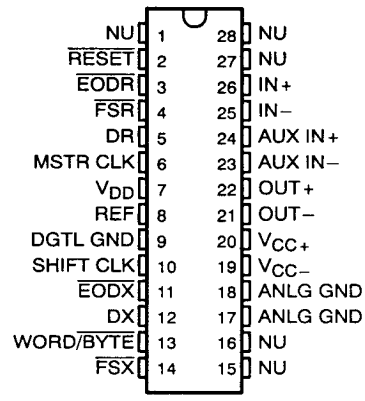
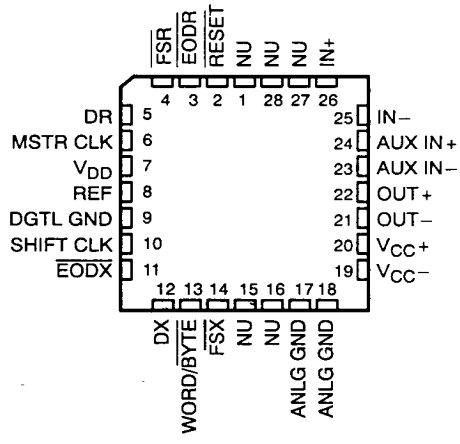
D3495, MAY 1990

- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Variable ADC and DAC Sampling Rate up to 19200 Samples Per Second**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Serial Port for Direct Interface to SMJ320E14, SMJ32020, SMJ320C25, and SMJ320C30 Digital Processors**
- **Synchronous or Asynchronous ADC and DAC Conversion Rates With Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Serial Port Interface to SN54299 Serial-to-Parallel Shift Register for Parallel Interface to SMJ320C10, SMJ320C15, SMJ320E15 or Other Digital Processors**
- **Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NU – Nonusable; no external connection should be made to these pins. See Table 2.

description

The TLC32044M is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This voice-band analog interface circuit integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of master clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this integrated circuit include speech encryption for digital transmission, speech recognition/storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the SMJ320E14, SMJ32020, SMJ320C25, and SMJ320C30 digital signal processors, are provided. Also, when the transmit and receive sections of the analog interface circuit (AIC) are

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description (continued)

operating synchronously, it will interface to two SN54299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the SMJ320C10, SMJ320C15, SMJ320E15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the integrated circuit can be selected and adjusted coincidentally with signal processing via software control.

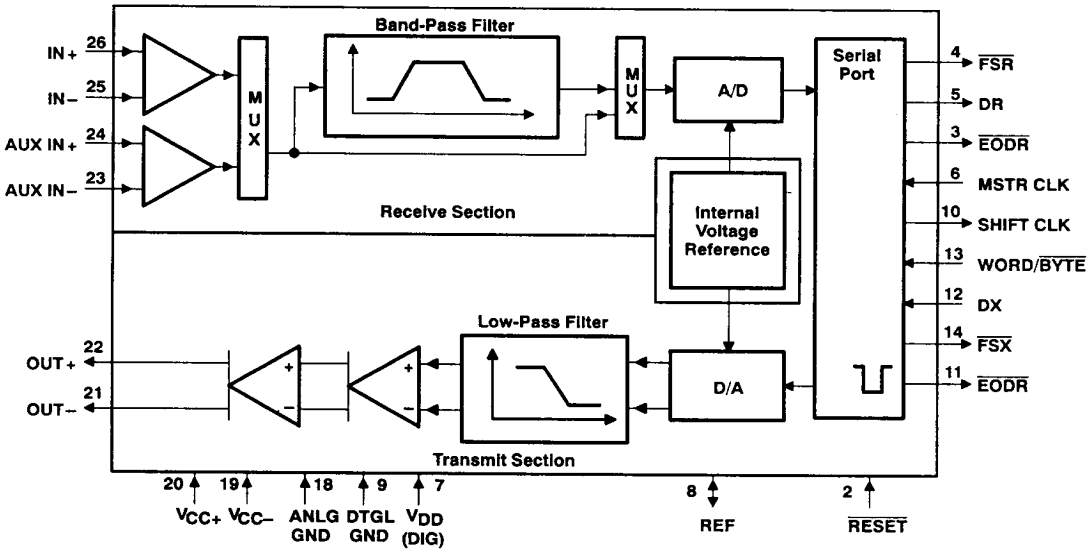
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the integrated circuit. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample and hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sinx)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32044M is characterized for operation from –55°C to 125°C.

functional block diagram



TEXAS INSTRUMENTS
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Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the band-pass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs will be used (see the AIC DX data word format section).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the SMJ320 serial port. This transmission of bits from the AIC to the SMJ320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the SMJ320. This serial transmission from the SMJ320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	End of data receive. (See the WORD/$\overline{\text{BYTE}}$ pin description and serial port timing diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the SMJ320 serial port. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the SMJ320 serial port and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second. $\overline{\text{EODR}}$ does not occur after secondary communication.
$\overline{\text{EODX}}$	11	O	End of data transmit. See the WORD/$\overline{\text{BYTE}}$ pin description and serial port timing diagram. During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the SMJ320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the SMJ320 serial port to the AIC and is kept low until the second byte has been transmitted. The DSP can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{\text{FSR}}$	4	O	Frame sync receive. In the serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the SMJ320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{\text{FSR}}$ goes low. (See Serial Port Timing and Internal Timing Configuration diagrams.) $\overline{\text{FSR}}$ does not occur after secondary communication.
$\overline{\text{FSX}}$	14	O	Frame sync transmit. When this pin goes low, the SMJ320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, $\overline{\text{FSX}}$ is held low during bit transmission (see the Serial Port Timing and Internal Timing Configuration diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN–	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The master clock signal is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The internal timing configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the internal timing configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT–	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. Also an external voltage reference can be applied to this pin.
$\overline{\text{RESET}}$	2	I	A reset function is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', will be reset to 1. The control register bits will be reset as follows (see the AIC DX data word format section). d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.

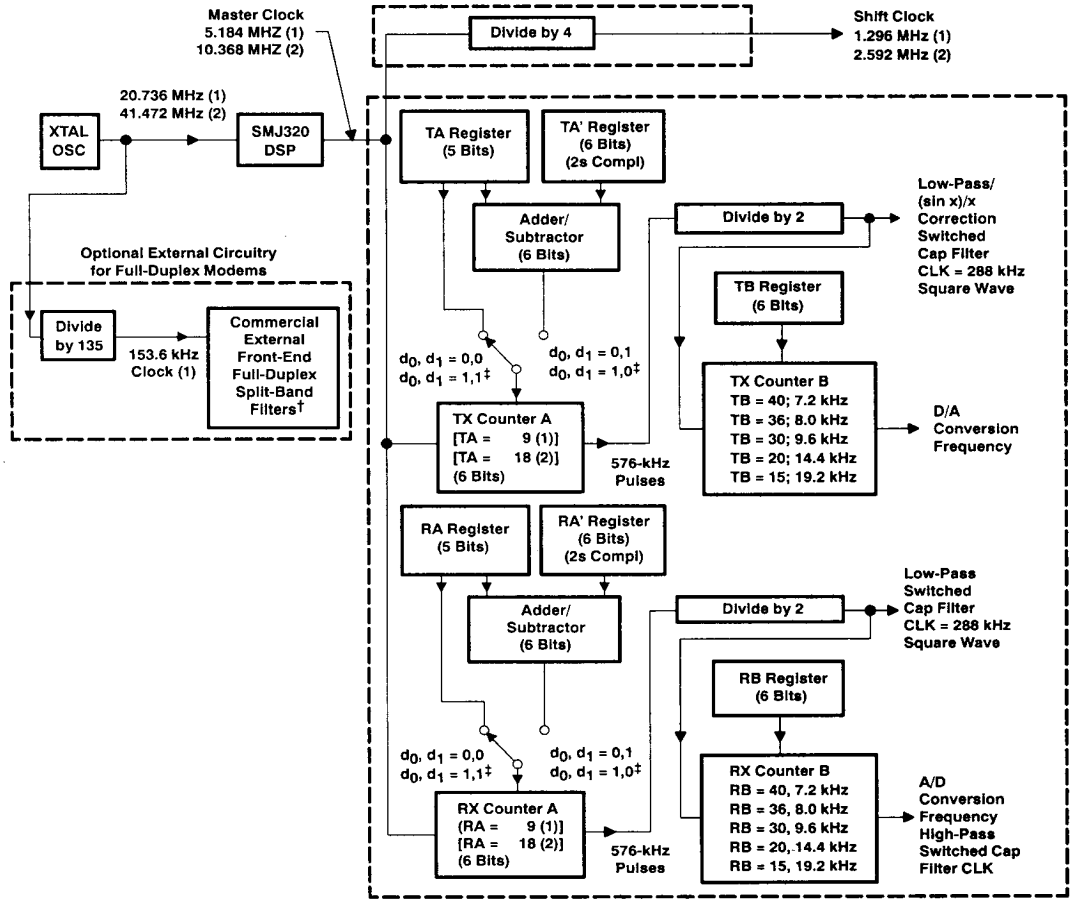
Terminal Functions (Continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
SHIFT CLK	10	O	The shift clock signal is obtained by dividing the master clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{\text{BYTE}}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagrams).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, −5 V ±5%
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the control register, is used to establish one of four serial modes. These four modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX data word format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the DSP and communications in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is brought low. 4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ emits a positive frame-sync pulse that is four shift clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is brought high. 7. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought high. H Serial port directly interfaces with the serial port of the SMJ32020, SMJ320C25, or SMJ320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought high. 4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the band-pass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA', and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the DSP and communicates in two 8-bit bytes 1. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought low. 4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ emits positive frame-sync pulse that are four shift-clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is brought high. 7. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ is brought high.

Terminal Functions (Continued)

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$ (continued)	13	I	H Serial port directly interfaces with the serial port of the SMJ32020, SMJ320C25, or SMJ320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high. 4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN54299 serial-to-parallel shift registers. Interfacing the AIC to the SN54299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



† Split-band filtering can alternatively be performed after the analog input function via software in the SMJ320.
‡ These control bits are described in the AIC DX data word format section.

NOTE: Frequency 1 (20.736 MHz) is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2 (41.472 MHz) is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

explanation of internal timing configuration

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D Path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D Path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX Counter A and TX Counter B, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency scaled by the ratios of the clock frequency to 288 kHz. Thus to obtain the specified filter response, the combination of master clock frequency and TX Counter A and RX Counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX Counter B to establish the D/A conversion timing.

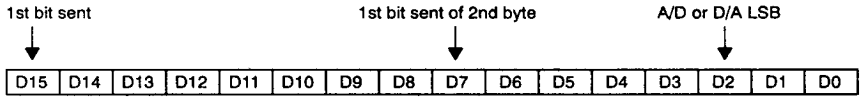
The transfer function of the band-pass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section will meet the band-pass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section will meet the band-pass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section will be frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the master clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description) then both the low-pass and band-pass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS
Primary DX serial communication protocol																
← d15 (MSB) through d2 go to the D/A converter register													→	0	0	The TX and RX Counter As are loaded with the TA and RA register values. The TX and RX Counter Bs are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register													→	0	1	The TX and Counter As are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter Bs are loaded with the TB and RB register values. Counter Bs are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register													→	1	0	The TX and Counter As are loaded with the TA - TA' and RA - RA' register values. The TX and RX Counter Bs are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register													→	1	1	The TX and Counter As are loaded with the TA and RA register values. The TX and RX Counter Bs are loaded with the TB and RB register values. After a delay of four shift-clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{\text{FSX}}$ will remain high for four shift-clock cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. in this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{\text{FSR}}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA' register → | x | ← to RA' register → | 0 1	d14 and d7 are 2s complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x x d7 d6 d5 d4 d3 d2 1 1 |← Control Register →|	d2 = 0/1 deletes/inserts the band-pass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN- pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184-MHz master clock input signal. The AIC, except the control register, will be initialized as follows (see AIC DX data word format section):

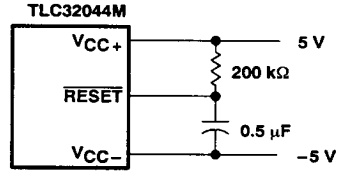
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA'	1
TB	24
RA	9
RA'	1
RB	24

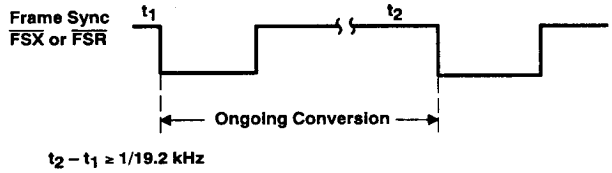
The control register bits will be reset as follows (see AIC DX data word format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions table and AIC DX data word format section).

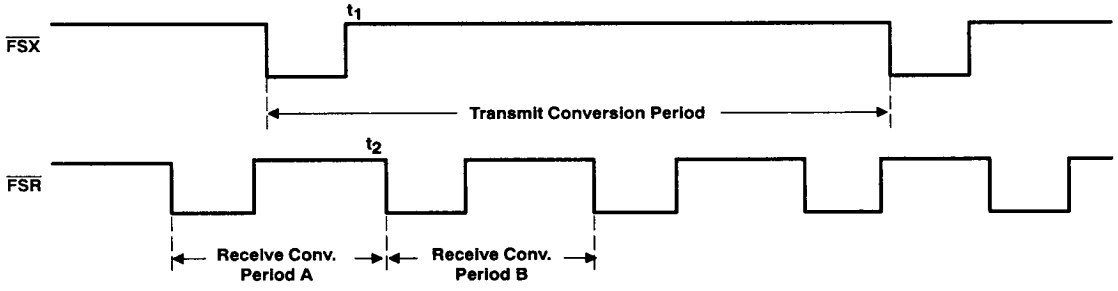
The circuit shown below will provide a reset on power up. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.





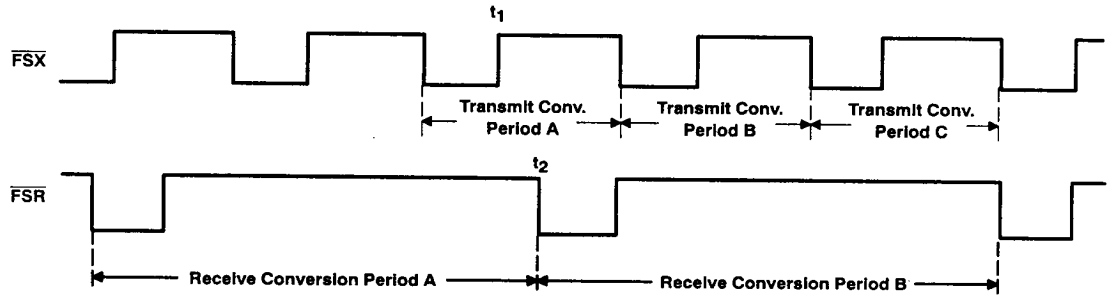
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t_1 and t_2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



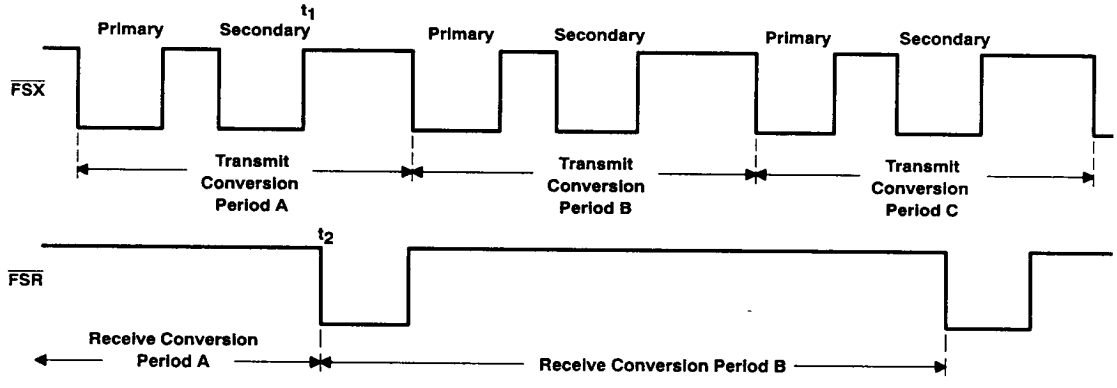
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the following figure. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t_1 and t_2. If there is not sufficient time between t_1 and t_2, Receive Conversion Period B will be adjusted. The receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation – more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX data word format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA', and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period will be disregarded (see diagram below).



test modes†

The following paragraph provides information that explains how the TLC32044M may be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications; however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) pins are left unconnected. These NU pins are used by the factory to speed up testing of the TLC32044M Analog Interface Circuit (AIC). When the device is used in normal (non-test-mode) operation, the NU pin (pin 1) has an internal pull down to 5 V. Externally connecting 0 V or 5 V to pin 1 puts the device in test-mode operation. Selecting one of the possible test modes is accomplished by placing a particular voltage on certain pins. A description of these modes is provided in Table 1 and Figures 1 and 2.

Table 1. List of Test Modes

TEST PINS	D/A PATH TEST (PIN 1 TO 5 V) TEST FUNCTION	A/D PATH TEST (PIN 1 TO 0 V) TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.	The band-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.
11	No change from normal operation. The $\overline{\text{EODX}}$ signal is brought out to pin 11.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The $\overline{\text{EODR}}$ signal is brought out.
27 and 28	There are no test output signals provided on these pins.	The outputs of the A/D path low-pass or band-pass filter (depending upon control bit d2 – see AIC DX data word format section) are brought out to these pins. If the high-pass section is inserted, the output will have a (six)/s droop. The slope of the droop will be determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of band-pass or low-pass filter test for receive section). These outputs will drive small (30-pF) loads.
	D/A PATH LOW-PASS FILTER TEST; PIN 13 (WORD/$\overline{\text{BYTE}}$) –5 V	
	TEST FUNCTION	
15 and 16	The inputs of the D/A path low-pass filter are brought out to pins 15 and 16. The D/A input to this filter is removed. If the (sin x)/x correction filter is inserted, the OUT+ and OUT– signals will have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V.	

† In the test mode, the AIC responds to the setting of pin 13 to 5 V, as if pin 13 were set to 0 V. Thus the byte mode is selected for communicating between the DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, pin 13 must be connected to 5 V, which initiates byte-mode communications.

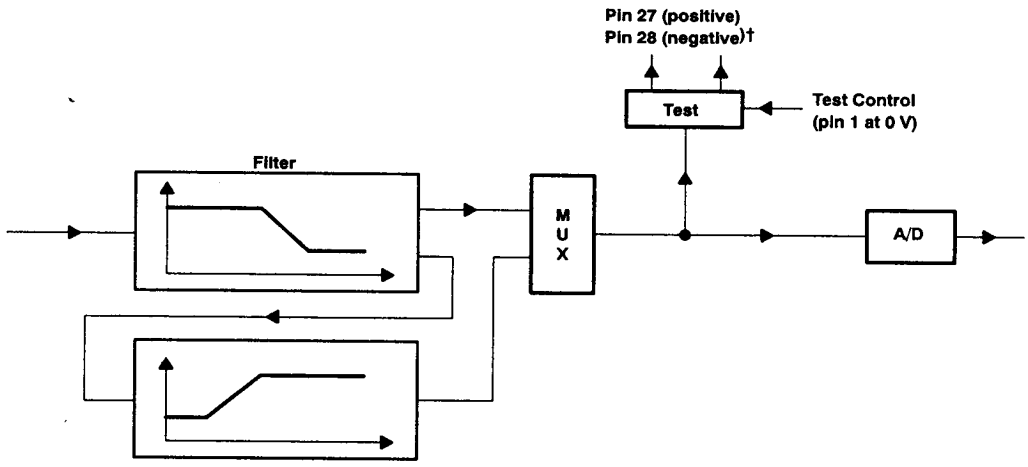


Figure 1. Band-Pass or Low-Pass Filter Test for Receiver Section

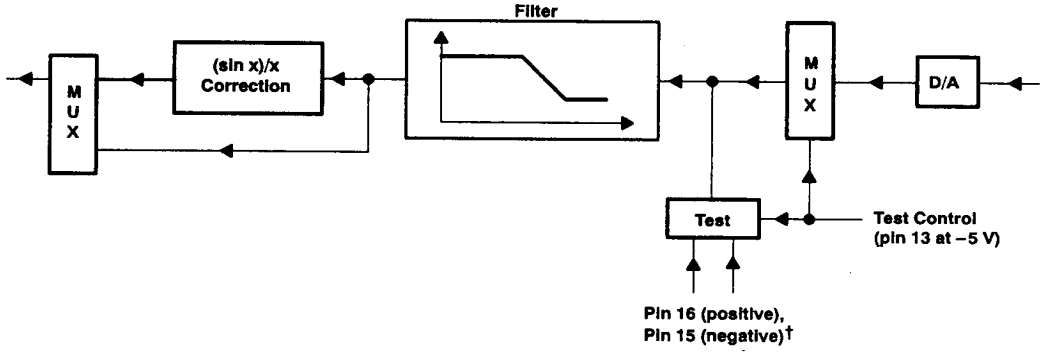


Figure 2. Low-Pass Filter Test for Transmit Section

† All analog signal paths have differential architecture and hence have positive and negative components.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) ..... −0.3 V to 15 V
Supply voltage range, V_{DD} ..... −0.3 V to 15 V
Output voltage range, V_O ..... −0.3 V to 15 V
Input voltage range, V_I ..... −0.3 V to 15 V
Digital ground voltage range ..... −0.3 V to 15 V
Operating free-air temperature range ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)	−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)	4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND		0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)	2		4	V
High-level input voltage, V_{IH}	2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	V
Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended) (see Note 4)	±3			V
Load resistance at OUT+ and/or OUT−, R_L	300			Ω
Load capacitance at OUT+ and/or OUT−, C_L			100	pF
MSTR CLK frequency (see Note 5)	0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 6)			±1.5	V
A/D or D/A conversion rate			20	kHz
Operating free-air temperature, T_A	−55		125	°C

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. This applies when $R_L \geq 300\ \Omega$ and offset voltage = 0.
5. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
6. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 4.75 V, I_{OH} = −300 µA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 4.75 V, I_{OL} = 2 mA			0.9	V
I_{CC+}	Supply current from V_{CC+}				40	mA
I_{CC-}	Supply current from V_{CC-}				−40	mA
I_{DD}	Supply current from V_{DD}	$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage		2.9		3.3	V
α_{Vref}	Temperature coefficient of internal reference voltage			200		ppm/°C
r_o	Output resistance at REF			100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	85	mV
CMRR	Common–mode rejection ratio at IN+, IN–, or AUX IN+, AUX IN–	See Note 7	35	55		dB
r_i	Input resistance at IN+, IN– or AUX IN+, AUX IN–, REF			100		kΩ

NOTE 7: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT– (single ended relative to ANLG GND)			15	75	mV
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT– (differential output)	RL ≥ 300 Ω	±6			V

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	Single ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref},	62	70		dB
	Differential	Single-ended tested at 25°C, See Note 8	62	70		
Attenuation of third and higher harmonics of A/D input signal	Single ended	V_{in} = −0.5 dB to −24 dB referred to V_{ref},	57	65		dB
	Differential	Single-ended tested at 25°C, See Note 8	57	65		
Attenuation of second harmonic of D/A input signal	Single ended	V_{in} = −0 dB to −24 dB referred to V_{ref},		70		dB
	Differential	See Note 8	62	70		
Attenuation of third and higher harmonics of D/A input signal	Single ended	V_{in} = −0 dB to −24 dB referred to V_{ref},		65		dB
	Differential	See Note 8	57	65		

† All typical values are at T_A = 25°C.

NOTE 8: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance fo the DAC is 300 Ω.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted) (continued)

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 8)	A_V = 1†		A_V = 2†		A_V = 4†		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_I = −6 dB to −0.5 dB	58		>58‡		>58‡		dB
	V_I = −12 dB to −6 dB	58		58		>58‡		
	V_I = −18 dB to −12 dB	56		58		58		
	V_I = −24 dB to −18 dB	50		56		58		
	V_I = −30 dB to −24 dB	44		50		56		
	V_I = −36 dB to −30 dB	38		44		50		
	V_I = −42 dB to −36 dB	32		38		44		
	V_I = −48 dB to −42 dB	26		32		38		
	V_I = −54 dB to −48 dB	20		26		32		

† A_V is the programmable gain of the input amplifier.
‡ A value > 58 is overrance and signal clipping occurs over range.

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 8)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_I = −6 dB to 0 dB	58		dB
	V_I = −12 dB to −6 dB	58		
	V_I = −18 dB to −12 dB	56		
	V_I = −24 dB to −18 dB	50		
	V_I = −30 dB to −24 dB	44		
	V_I = −36 dB to −30 dB	38		
	V_I = −42 dB to −36 dB	32		
	V_I = −48 dB to −42 dB	26		
	V_I = −54 dB to −48 dB	20		

NOTE 8: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 300 Ω.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and band-pass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	With (sin x)/x	DX input = 00000000000000, constant input code		575	μV rms
	Without (sin x)/x		325	450	μV rms
			18		dBrnc0
Receive noise (see Note 9)		Inputs grounded, gain = 1	300	500	μV rms
			18		dBrnc0

§ All typical values are at T_A = 25°C.
NOTE 9: This noise is computed by statistically evaluating the digital output of the A/D converter.

timing requirements

serial port recommended input signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	100	192	ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	42%	58%	
	$\overline{\text{RESET}}$ pulse duration (see Note 10)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	28		ns
$t_{h(DX)}$	DX hold time before SCLK↓	$t_{c(SCLK)}/4$		ns

NOTE 10: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port – AIC output signals

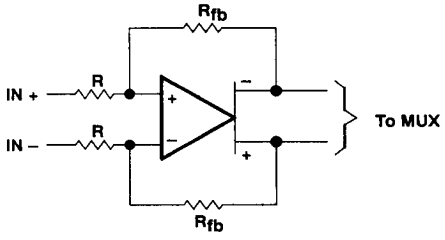
PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	400			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50		ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50		ns
	Shift clock (SCLK) duty cycle		50		ns
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}$↓			260	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR}}/\overline{\text{FSX}}$↑			260	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			316	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↓ in WORD mode			280	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↑ in WORD mode			280	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		15		ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		15		ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↓ in $\overline{\text{BYTE}}$ mode		100		ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}/\overline{\text{EODR}}$↑ in $\overline{\text{BYTE}}$ mode		100		ns
$t_{d(MH-SL)}$	Delay from MSTR CLK ↑ to SCLK↓		65		ns
$t_{d(MH-SH)}$	Delay from MSTR CLK ↑ to SCLK↓		65		ns

† Typical values are T_A = 25°C.

Table 2. Gain Control Table
(Analog Input Signal Required for Full-Scale A/D Conversion)

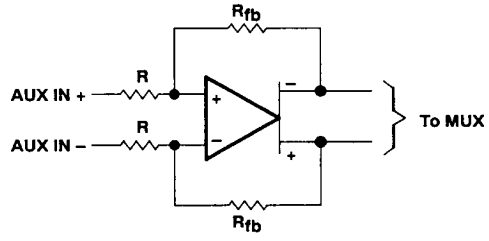
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT†	A/D CONVERSION RESULT
	d6	d7		
Differential configuration Analog input = IN+ – IN–	1 0	1 0	±6 V	Full scale
= AUX IN+ – AUX IN–	1	0	±3 V	Full scale
	0	1	±1.5 V	Full scale
Single-ended configuration Analog input = IN+ – ANLG GND	1 0	1 0	±3 V	Half scale
= AUX IN+ – ANLG GND	1	0	±3 V	Full scale
	0	1	±1.5 V	Full scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

Figure 3. IN+ and IN– Gain Control Circuitry



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

Figure 4. AUX IN+ and AUX IN– Gain Control Circuitry

(sin x)/x correction section

The AIC does not have (sin x)/x correction circuitry after the digital-to-analog converter. (sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown on the next page, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the SMJ320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300 – 3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

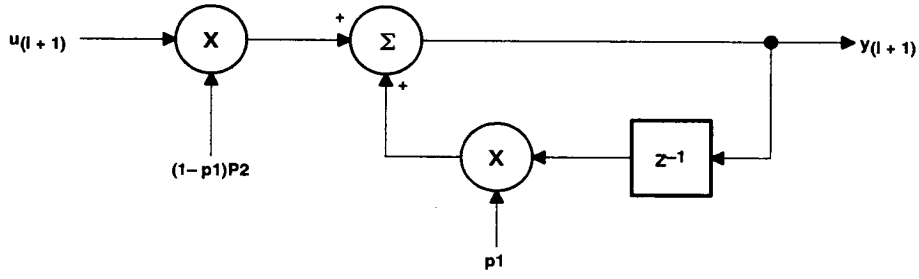
Table 3. (sin x)/x Roll-Off

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	−2.64
8000	−2.11
9600	−1.44
14400	−0.63
19200	−0.35

Note that the actual AIC (sin x)/x roll-off will be slightly less than the above figure because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$Y_i + 1 = p2(1 - p1)\ (u_i + 1) + p1\ Y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H\ (f)|^2 = \frac{p2^2\ (1 - p1)^2}{1 - 2p1\ \cos(2\ \pi\ f/f_s) + p1^2}$$

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

Table 4. Optimum P Values

f (Hz)	ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0.0999	ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	−0.099	−0.043
600	−0.089	−0.043
900	−0.054	0
1200	−0.002	0
1500	0.041	0
1800	0.079	0.0.43
2100	0.100	0.043
2400	0.091	0.043
2700	−0.043	0
3000	−0.102	−0.043

SMJ320 software requirements

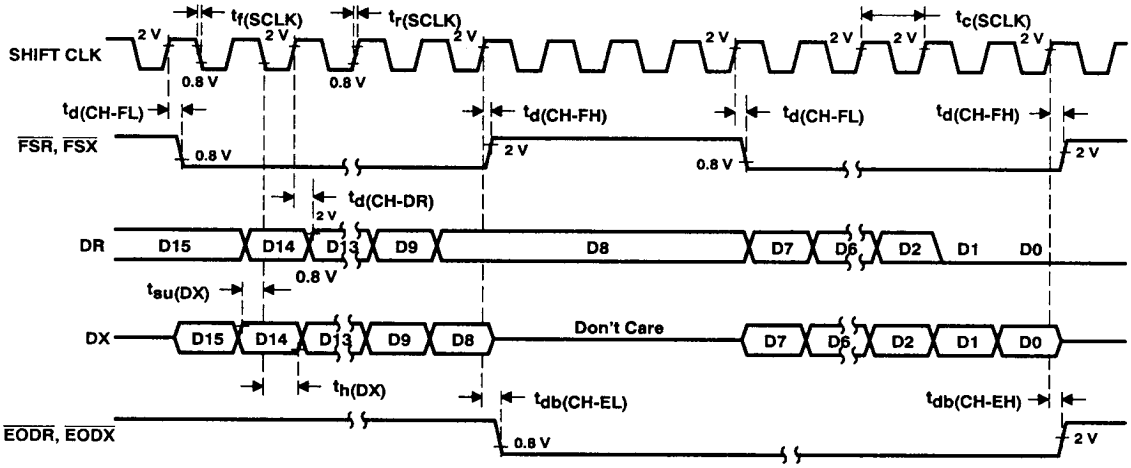
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

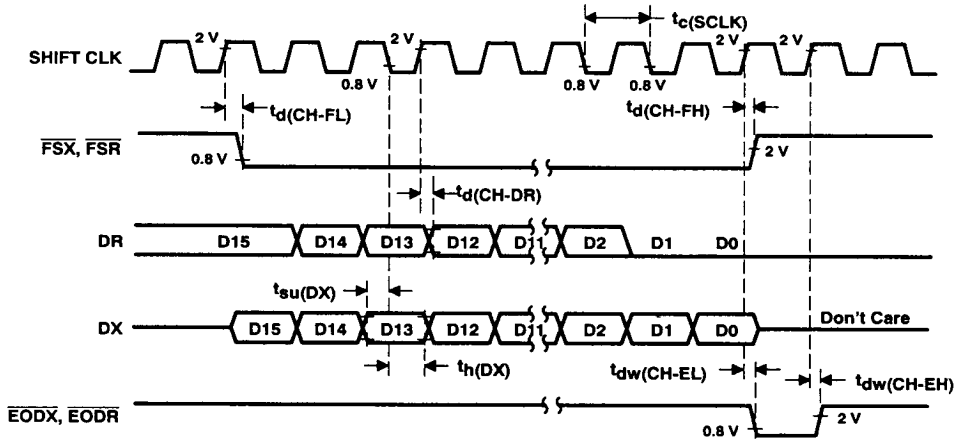
where k1 equals p1 (from the preceding page), k2 equals (1 – p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the SMJ320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

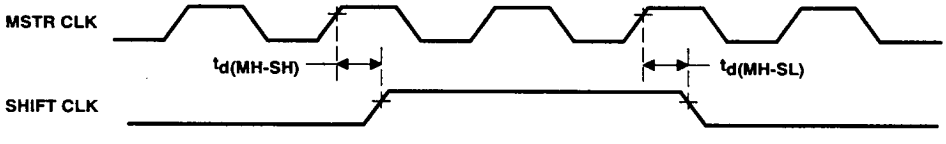
PARAMETER MEASUREMENT INFORMATION



(a) BYTE-MODE TIMING



(b) WORD-MODE TIMING



(c) SHIFT-CLOCK TIMING

Figure 5. Serial Port Timing

PARAMETER MEASUREMENT INFORMATION

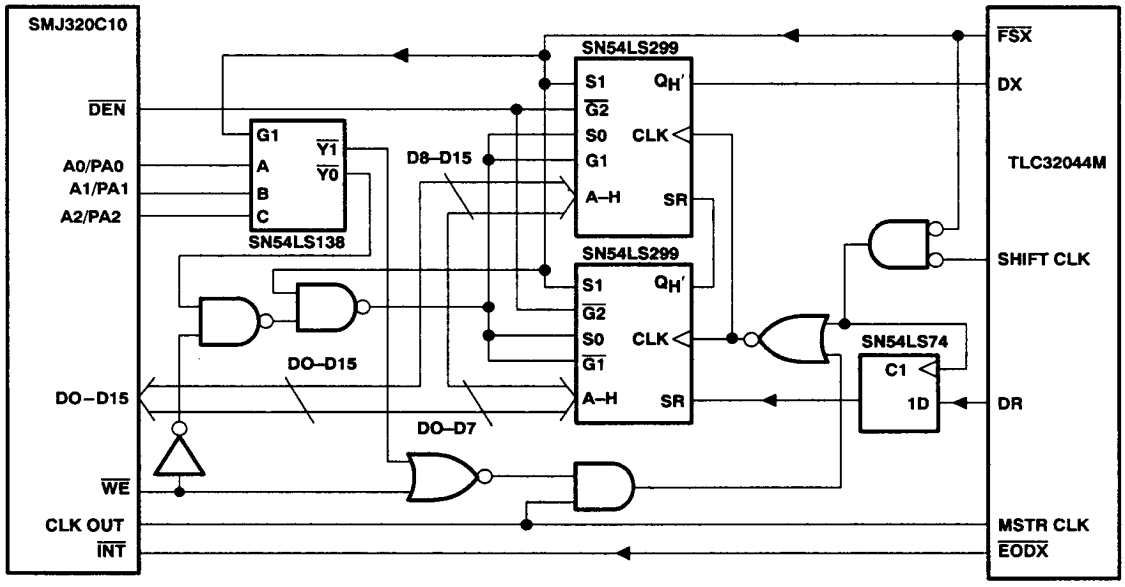


Figure 6. SMJ320C10/SMJ320C15/SMJ320E15-TLC32044M Interface Circuit

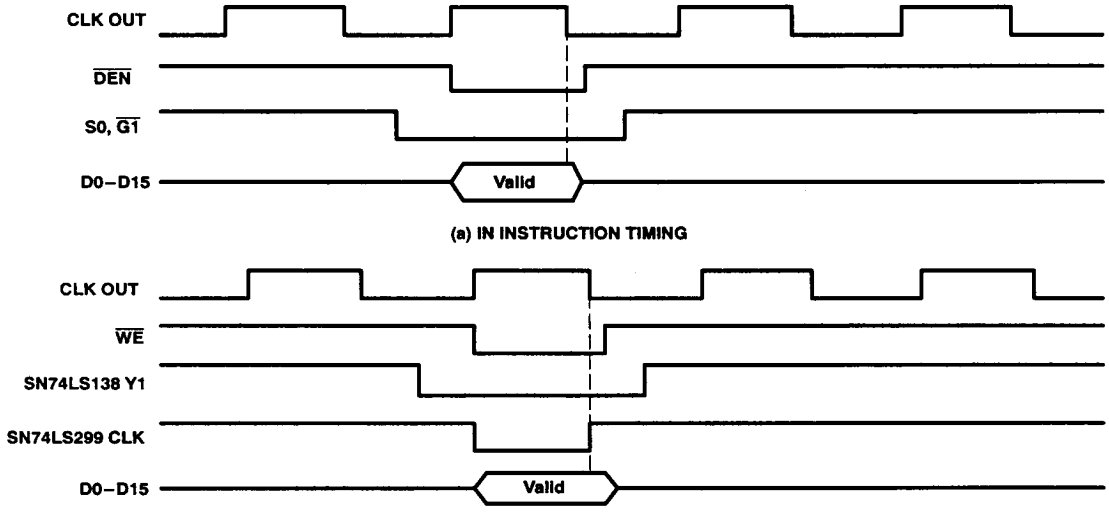


Figure 7. SMJ320C10/SMJ320C15/SMJ320E15-TLC32044M Interface Timing

TYPICAL CHARACTERISTICS

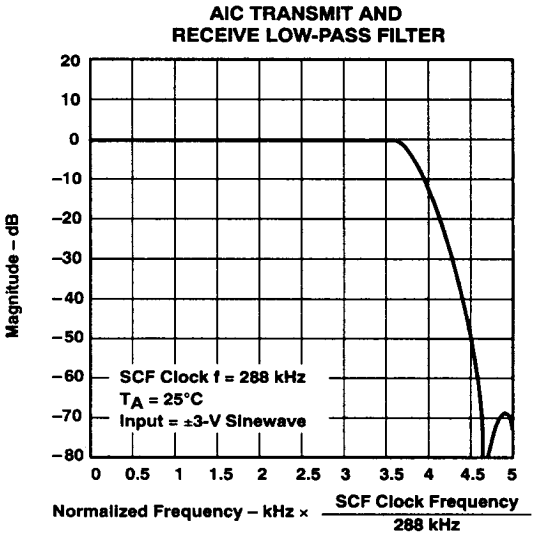


Figure 8

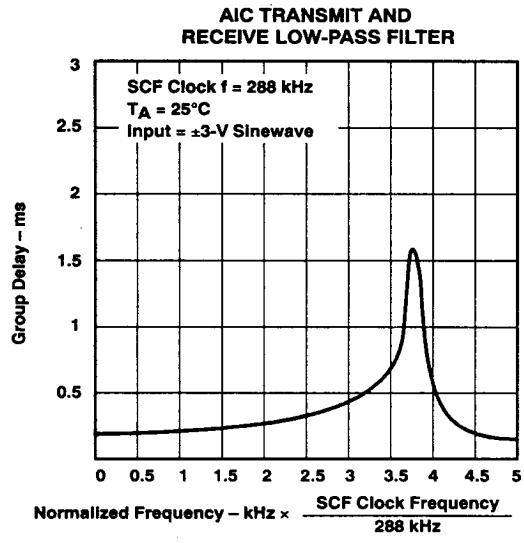


Figure 9

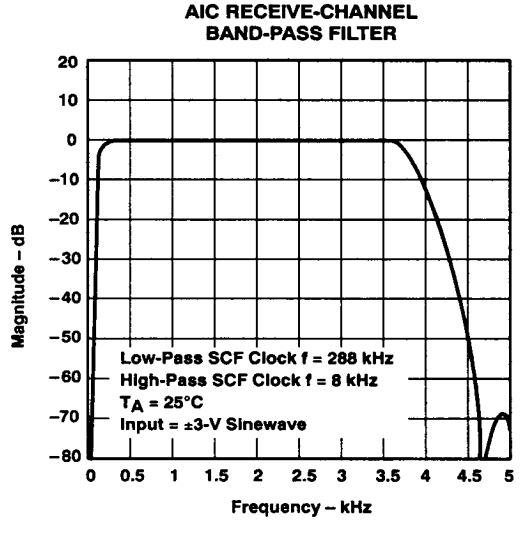


Figure 10

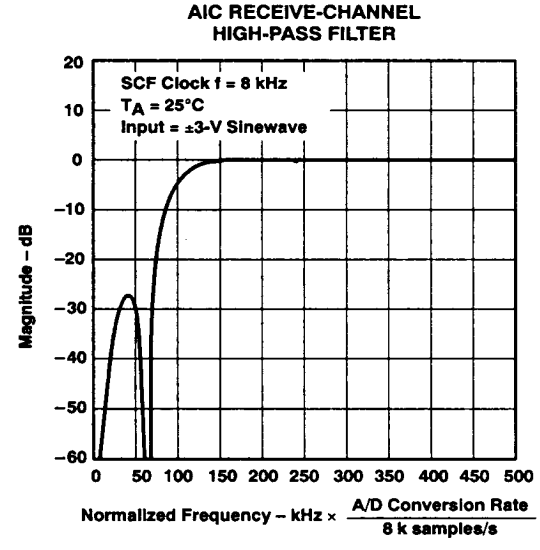


Figure 11

TYPICAL CHARACTERISTICS

AIC RECEIVE-CHANNEL
BAND-PASS FILTER

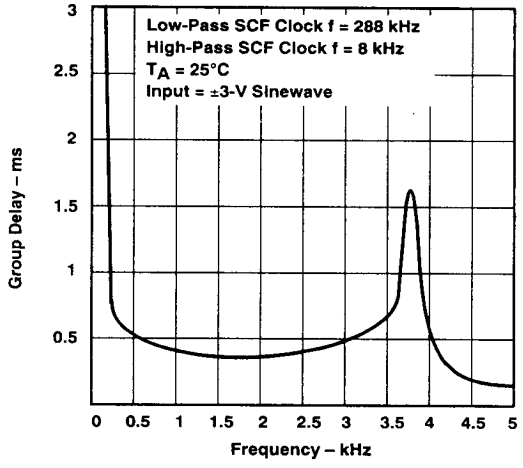


Figure 12

AIC (sin x)/x CORRECTION FILTER

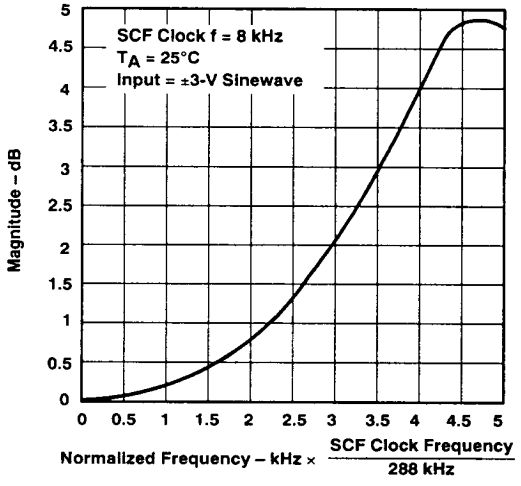


Figure 13

AIC (sin x)/x CORRECTION FILTER

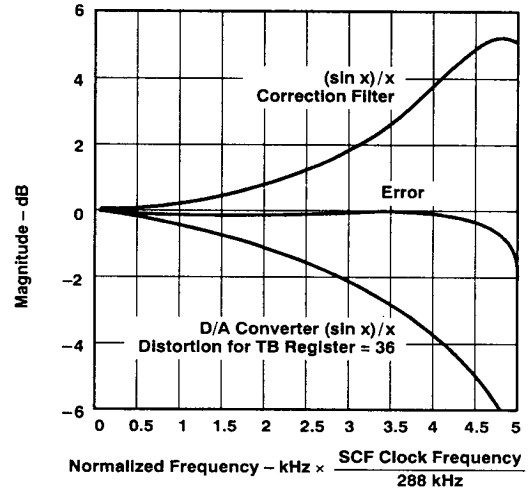


Figure 14

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

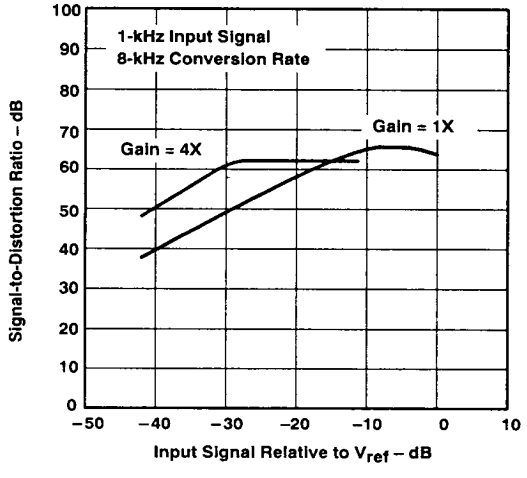


Figure 15

TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)

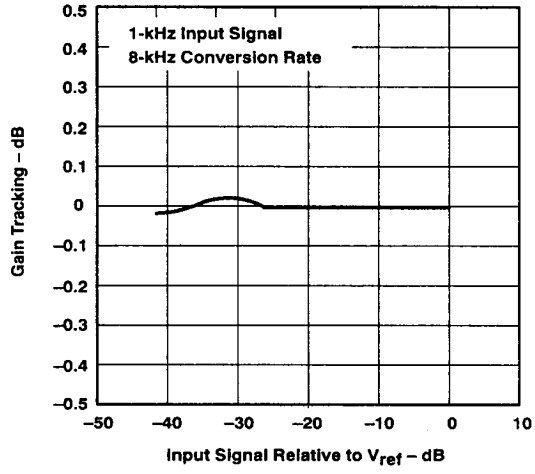


Figure 16

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL LEVEL

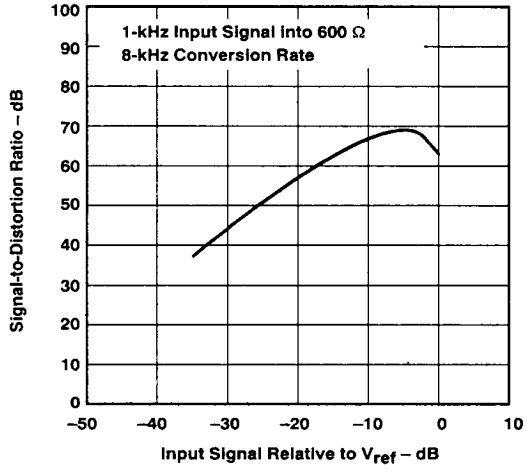


Figure 17

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL LEVEL)

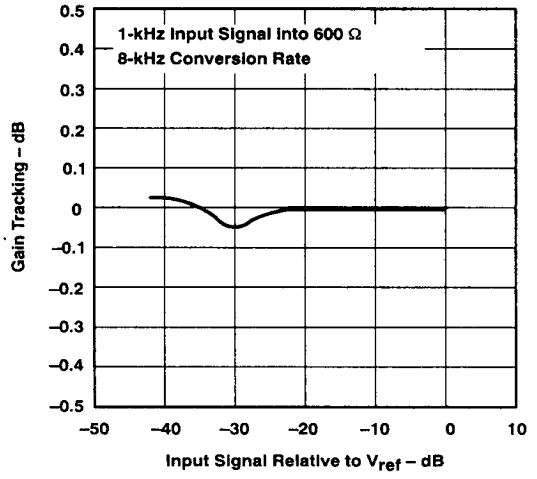


Figure 18

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

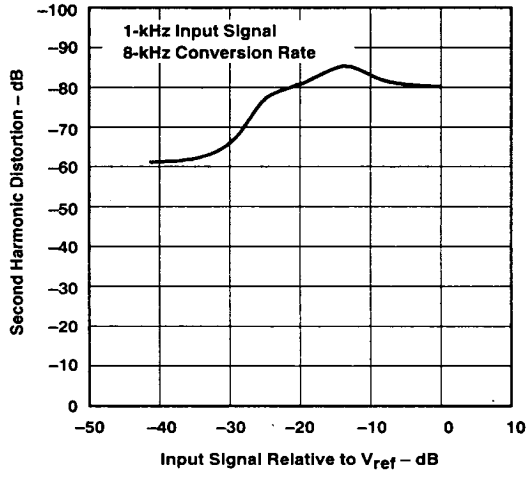


Figure 19

TYPICAL CHARACTERISTICS

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

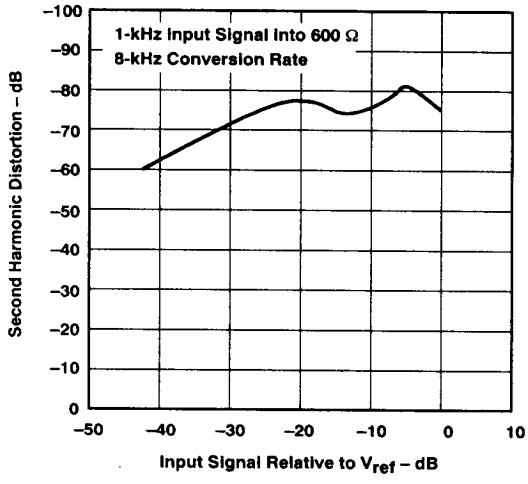


Figure 20

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

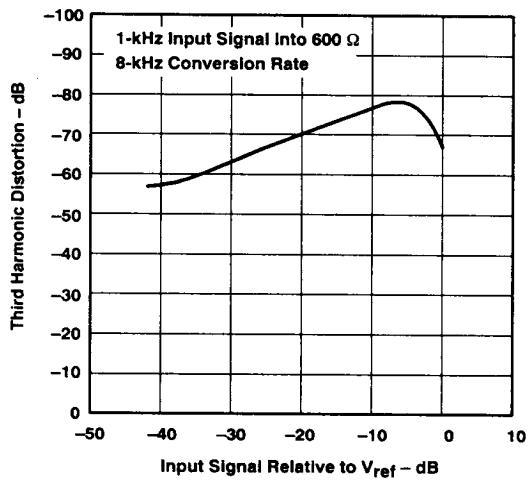


Figure 21

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

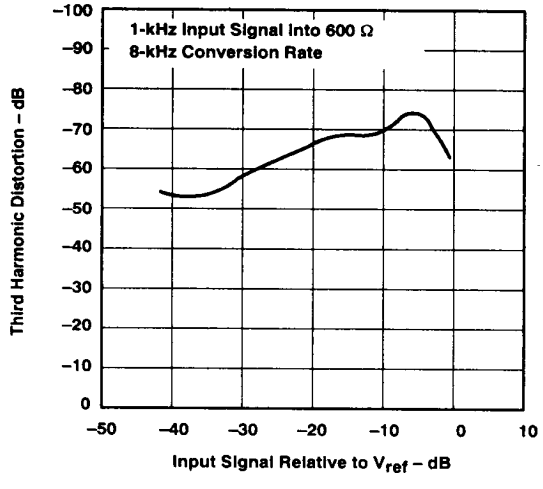


Figure 22

APPLICATION INFORMATION

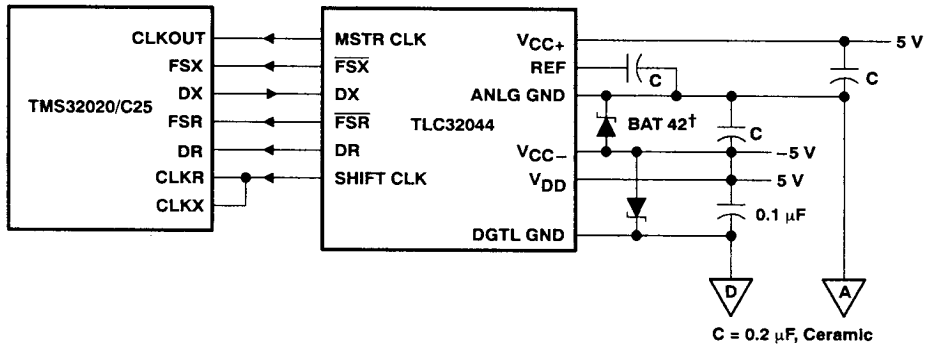
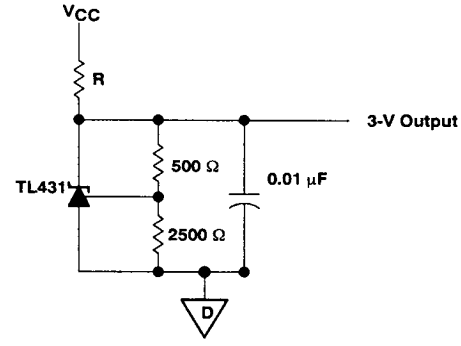


Figure 23. AIC Interface to the SMJ32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors



For: V_{CC} = 12 V, R = 7200 W
V_{CC} = 10 V, R = 5600 W
V_{CC} = 5 V, R = 1600 W

Figure 24. External Reference Circuit for TLC32044

PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D band-pass filter, A/D band-pass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency scaled by the ratio of the A/D sample rate to 8 kHz.

The A/D conversion rate is then attained by frequency dividing the 288-kHz band-pass switched-capacitor filter clock with the RX Counter B. Thus unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample and hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x)/x filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

PRINCIPLES OF OPERATION

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (band-pass filter and ADC) are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Terminal Functions table.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample and hold that is realized with a switched-capacitor ladder.

system frequency response correction

(Sin x)/x correction for the D/A converter's zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see internal timing configuration section) equals 36, the correction results of Figures 11 and 12 will be obtained.

(Sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ±0.1-dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven SMJ320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x correction section for more details).

serial port

The serial port has four possible modes that are described in detail in the Terminal Functions table. These modes are briefly described below and in the description for pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the DSP in two 8-bit bytes.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the SMJ32020, SMJ320C25, and the SMJ320C30.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the DSP in two 8-bit bytes.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the SMJ32020, SMJ320C25, SMJ320C30, or two SN54299 serial-to-parallel shift registers, which can then interface in parallel to the SMJ320C10, SMJ320C15, SMJ320E15, to any other digital signal processor or to external FIFO circuitry.

PRINCIPLES OF OPERATION

operation of TLC32044M with internal voltage reference

The internal reference of the TLC32044M eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32044M with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function will initialize all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX data word format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. Thus the DAC bits (d15 to d2), which are transmitted to DX, can be compared with the ADC bits (d15 to d2), which are received from DR. An ideal comparison would be that the bits on DR equal the bits on DX. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC DX data word format section).