

P54/74FCT157T/AT/CT P54/74FCT158T/AT/CT DATA SELECTOR/MULTIPLEXER



FEATURES

- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-C speed at 4.3ns max. (Com'I)
FCT-A speed at 5.0ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'I), 32 mA (MII)
15 mA Source Current (Com'I), 12 mA (MII)
- Manufactured in 0.7 micron PACE Technology™



DESCRIPTION

The 'FCT157T and 'FCT158T are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data Select input (S). The Enable input ($\bar{E}$) is active-low. When $\bar{E}$ is HIGH, all of the inputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 'FCT157T and 'FCT158T. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

These devices are logic implementation of a 4-pole, 2

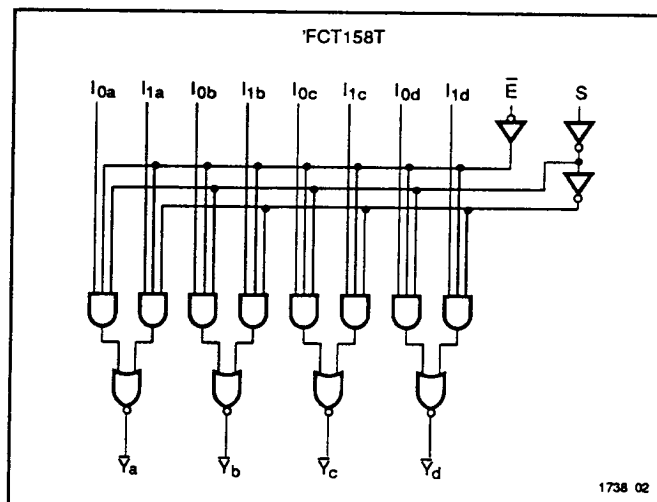
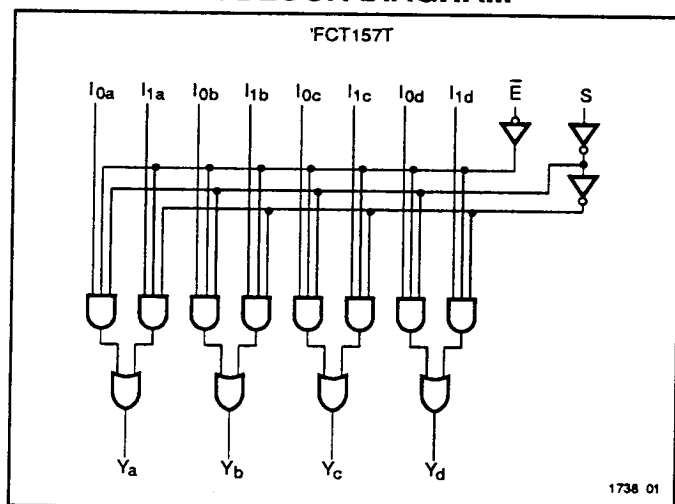
position switch where the position of the switch is determined by the logic levels supplied to the Select input. The outputs of the 'FCT157T are Non-Inverting whereas the 'FCT158T has Inverting outputs.

The 'FCT157T/158T is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. Pace Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.



FUNCTIONAL BLOCK DIAGRAM

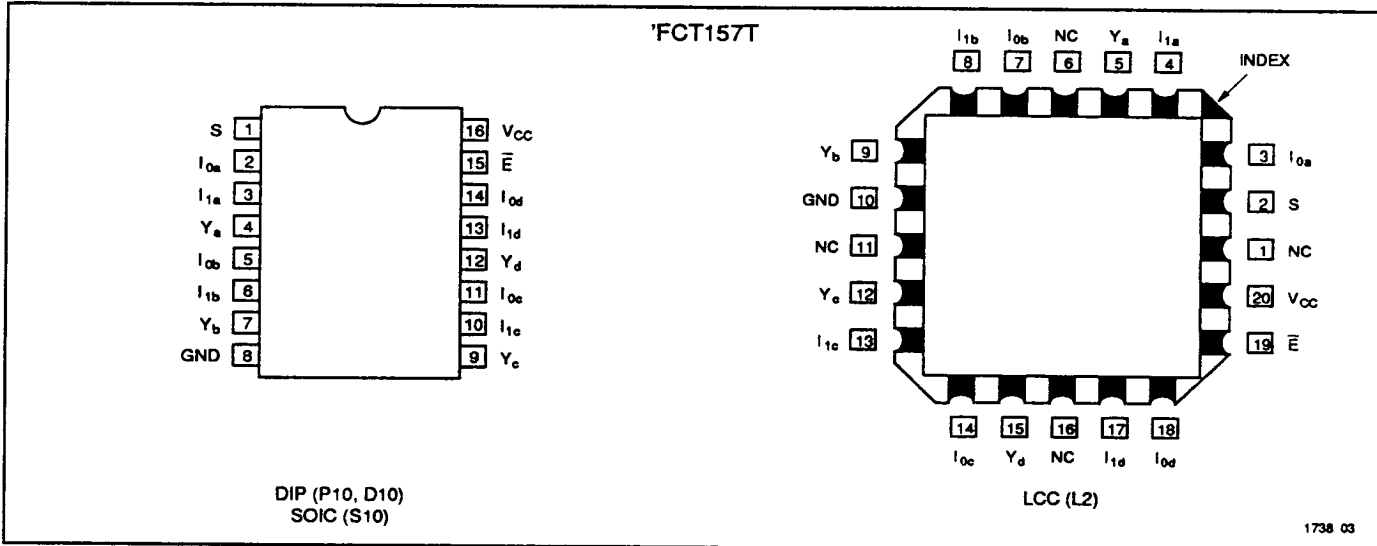


Means Quality, Service and Speed

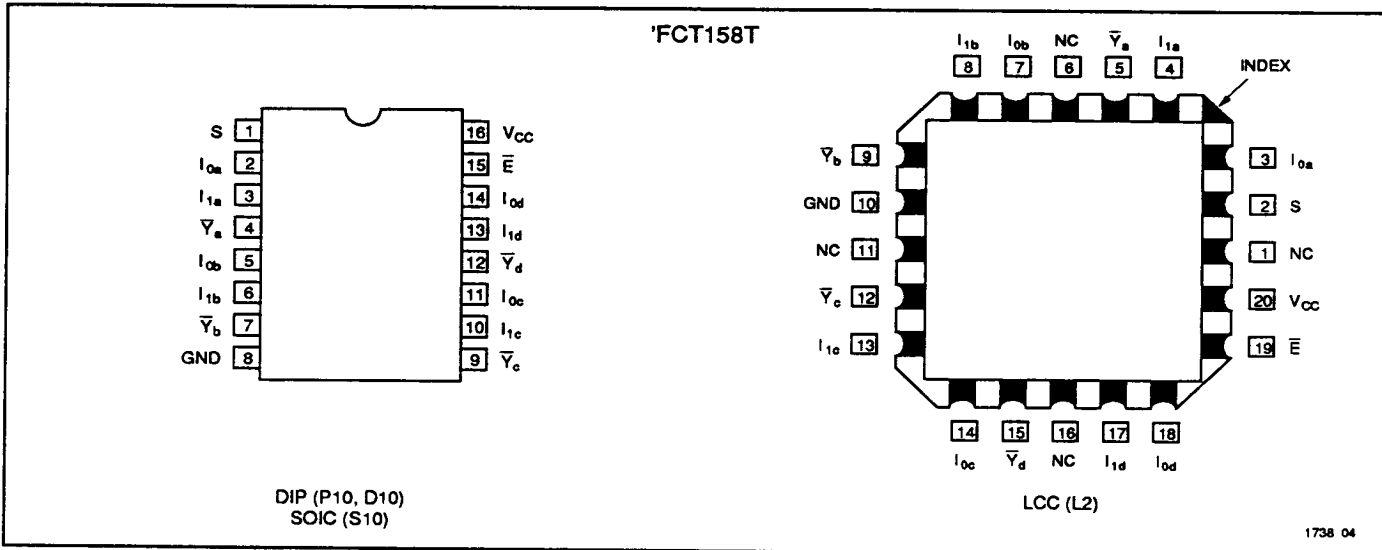
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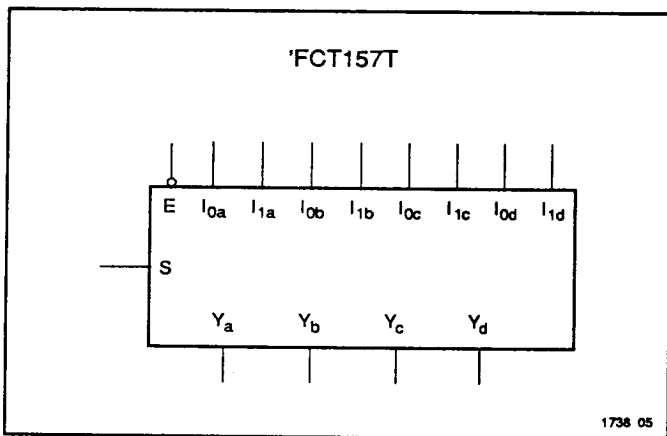
PIN CONFIGURATIONS



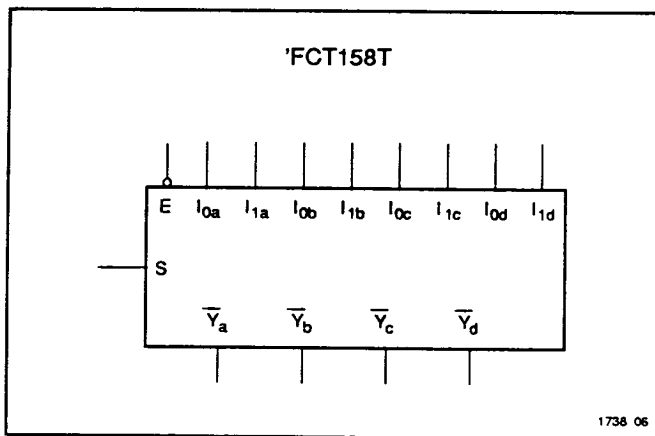
PIN CONFIGURATIONS



LOGIC SYMBOL



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	–65 to +150	°C
T _A	Ambient Temperature Under Bias	–65 to +135	°C
V _{CC}	V _{CC} Potential to Ground	–0.5 to +7.0	V
P _T	Power Dissipation	0.5	W

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I _{OUTPUT}	Current Applied to Output	120	mA
V _{IN}	Input Voltage	–0.5 to +7.0	V
V _{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V _{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ ¹	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		
V _{IL}	Input LOW Voltage				0.8	V		
V _H	Hysteresis			0.2		V		All inputs
V _{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I _{IN} = –18mA
V _{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I _{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I _{OH} = –15mA
V _{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I _{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I _{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I _{OL} = 64mA
I _I	Input HIGH Current				20	μA	MAX	V _{IN} = V _{CC}
I _{IH}	Input HIGH Current				5	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current				–5	μA	MAX	V _{IN} = 0.5V
I _{OZH}	Off State I _{OUT} HIGH-Level Output Current				10	μA	MAX	V _{OUT} = 2.7V
I _{OZL}	Off State I _{OUT} LOW-Level Output Current				–10	μA	MAX	V _{OUT} = 0.5V
I _{OS}	Output Short Circuit Current ²		–60	–120	–225	mA	MAX	V _{OUT} = 0.0V
I _{OFF}	Power-off Disable				100	μA	0V	V _{OUT} = 4.5V
C _{IN}	Input Capacitance ³			5	10	pF	MAX	All inputs
C _{OUT}	Output Capacitance ³			9	12	pF	MAX	All outputs
I _{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	V _{IN} ≤ 0.2V, V _{IN} ≥ V _{CC} – 0.2V

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Notes:

- Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

- operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ. ¹	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	1.7	4.0	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1 = 10\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1 = 10\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		1.7	4.0 ⁴	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.7	8.0 ⁴	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

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Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 $I_{CC} = \text{Quiescent Current with CMOS input levels}$

 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $(V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_0 = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_1 = \text{Input Frequency}$
 $N_1 = \text{Number of Inputs at } f_1$

All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE — 'FCT157T

Enable	Select Inputs	Data Inputs		Output
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

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H = High voltage level

L = Low voltage level

X = Don't care

FUNCTION TABLE — 'FCT158T

Enable	Select Inputs	Data Inputs		Output
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	X	L	H
L	L	X	H	L
L	H	L	X	H
L	H	H	X	L

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PIN DESCRIPTIONS

Pin Names	Description
S	Common Select Input
$\bar{E}$	Enable Input (Active LOW)
$I_{0A} - I_{0D}$	Data Inputs from Source 0
$I_{1A} - I_{1D}$	Data Inputs from Source 1
$Y_A - Y_D$	Non-Inverted Output
$\bar{Y}_A - \bar{Y}_D$	Inverted Output

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AC CHARACTERISTICS ('FCT157T)

Symbol	Parameter	'FCT157T				'FCT157AT				'FCT157CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_n to Y	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}$ to Y	1.5	12.0	1.5	10.5	1.5	7.4	1.5	6.0	1.5	5.9	1.5	4.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	1.5	6.0	1.5	5.2	ns	1, 3

Note: Minimum limits are guaranteed but not tested on Propagation Delays.

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AC CHARACTERISTICS ('FCT158T)

Symbol	Parameter	'FCT158T				'FCT158AT				'FCT158CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Propagation Delay I _n to Y	1.5	7.5	1.5	6.5	1.5	6.3	1.5	5.5	1.5	5.5	1.5	4.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}$ to Y	1.5	12.5	1.5	11.0	1.5	7.9	1.5	6.5	1.5	6.4	1.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.5	12.5	1.5	11.0	1.5	8.6	1.5	7.5	1.5	6.5	1.5	5.7	ns	1, 2

Note: Minimum limits are guaranteed but not tested on Propagation Delays.

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ORDERING INFORMATION

<u>PxxFCT</u> Temp. Class	<u>xxxx</u> Device type	<u>x</u> Package	<u>x</u> Processing		
				Blank	Commercial
				M	Military Temperature
				B	MIL-STD-883, Class B
				P	Plastic DIP
				D	CERDIP
				S	Small Outline IC
				L	Leadless Chip Carrier
				157 T	Quad 2-Input Data Selector (Non-Inverted)
				158 T	Quad 2-Input Data Selector (Inverted)
				157 AT	Fast Quad 2-Input Data Selector (Non-Inverted)
				158 AT	Fast Quad 2-Input Data Selector (Inverted)
				157 CT	Ultra Fast Quad 2-Input Data Selector (Non-Inverted)
				158 CT	Ultra Fast Quad 2-Input Data Selector (Inverted)
				74	Commercial
				54	Military

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